

Supporting Information:

AC-Impedance Spectroscopic Analysis on the Charge Transport in CVD-Grown Graphene Devices with Chemically Modified Substrates

Bok Ki Min,^{†,‡} Seong K. Kim[†], Seong Ho Kim[†], Min-A Kang[†], Suttinart Noothongkaew[†], Edmund M. Mills[§], Wooseok Song[†], Sung Myung[†], Jongsun Lim[†], Sangtae Kim[§], and Ki-Seok An^{†}*

[†]Thin Film Materials Research Center, Korea Research Institute of Chemical Technology (KRICT), Yuseong, Daejeon 305-600, Republic of Korea

[‡]Department of Physics, Sungkyunkwan University, 2066 Seobu-ro, Jangan-gu, Suwon-si, Gyeonggi-do 440-746, Republic of Korea

[§]Department of Chemical Engineering and Materials Science, University of California, Davis, California 95616-5294, United States

*E-mail: ksan@kRICT.re.kr.

EXPERIMENTAL DETAIL

Synthesis of graphene

Graphene was synthesized on a 25- μm -thick Cu foils (Sigma-Aldrich) by thermal chemical vapor deposition (TCVD). The Cu foil was put into a quartz tube and pre-annealed under 2 Torr H_2 (100 sccm) at 1050 $^{\circ}\text{C}$ for 30 min, after which a mixture of CH_4 (2 sccm) and H_2 (100 sccm) was introduced for 20 min to synthesize graphene films. The sample was cooled to room temperature. The synthesized graphene films were then transferred onto heavily p-doped silicon (100) substrates with 300-nm-thick SiO_2 insulating layers by the poly(methyl methacrylate) (PMMA) assisted wet transfer method. The substrates were cleaned beforehand in deionized water containing detergent, acetone, and isopropanol by ultrasonication. Then, the residues on the SiO_2 surface were removed by O_2 plasma with a RF power of 200 W for 10 min. The PMMA layer was removed by immersing in acetone bath. The absence of PMMA residues on graphene was confirmed using XPS analysis (Figure S1).

SAMs treatment and characterization

Hexamethyldisilazane (HMDS) and octyltrichlorosilane (OTS) were used as SAM molecules on SiO_2 surface. These materials were purchased from Sigma Aldrich. OTS was fabricated on cleaned SiO_2/Si substrates following the procedure reported in the literature.¹ A HMDS was formed by spin-coating with a rotation speed of 4000 rpm for 30 s followed by annealing at 125 $^{\circ}\text{C}$ for 10 min under ambient conditions. The graphene samples on the various SAMs treated SiO_2 were characterized using Raman spectroscopy and X-ray photoelectron spectroscopy (XPS). The Raman spectra were obtained using a Raman spectrometer (Renishaw) with excitation wavelength of 514 nm to confirm the successful synthesis of graphene and to determine the

effect of SAMs treatment to graphene layer. The compatibility of SAMs on SiO₂ was investigated using XPS. The XPS analysis was performed using conventional monochromatic Al K α (1486.7 eV) radiation with a normal emission geometry and vacuum pressure of 10⁻⁸ mbar during the analysis. The C 1s core level spectra were acquired with pass energy of 50 eV, energy step of 0.1 eV, dwell time of 50 ms, and spot size of 400 μ m. There is no charging effect for C 1s binding energy (~284.7 eV).

Device fabrication

To fabricate the device, graphene grown using TCVD was transferred on the silicon substrates with a 300 nm-thick SiO₂. The transferred graphene was patterned using aluminum (Al) as the sacrificial layer that was deposited by thermal evaporation with the thickness of 20 nm. The exposed graphene was removed using O₂ plasma with a RF power of 200 W for 5 min, after which Al was wet-etched by aqueous iron chloride (FeCl₃) solution, and then the substrates were carefully rinsed with deionized water. Cr/Au electrodes were deposited by thermal evaporation through a sheet mask. With patterned graphene, the residual capacitive components from neighboring cells can be avoided.

Electrical characterization

All room temperature impedance measurements were performed using an Agilent 4294a impedance analyzer. Measurements were conducted over the frequency range of 10² to 10⁷ Hz with ac amplitude of 50 mV. The variable temperature measurements were performed in vacuum (~10⁻⁶ Torr) with a MS-tech vacuum probe station. Liquid nitrogen and a heating stage were used to control the temperature. The impedance spectra were fitted employing the Zview software.

Transmission line method (TLM) was performed using an Agilent 4200 semiconductor analyzer to determine the contact resistance between the graphene and electrodes.

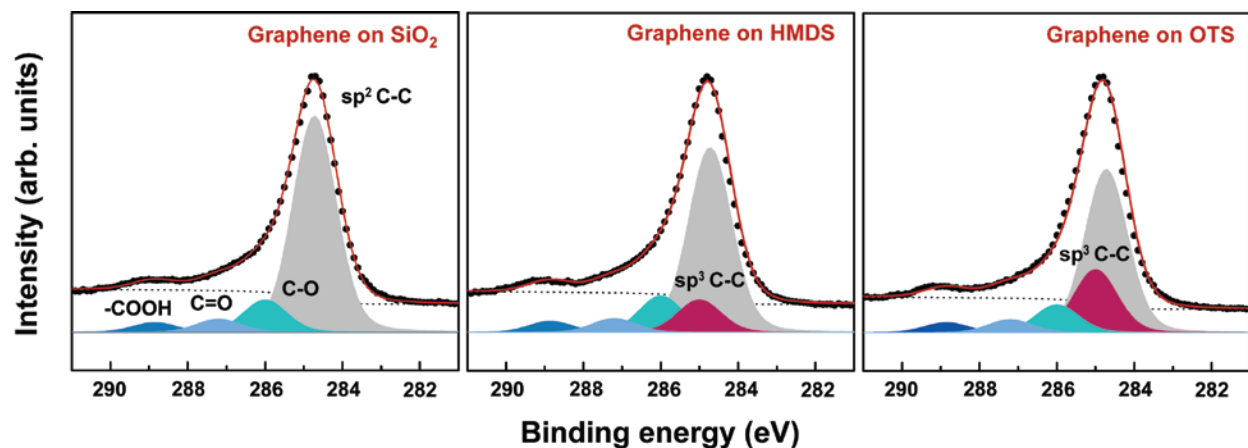


Figure S1. XPS spectra of the C 1s core level for the graphene on untreated, HMDS, and OTS treated SiO₂.

For the graphene on bare SiO₂, the C 1s core level was consistently fitted by three components which are the main contribution of the sp² carbon atoms in graphene at 284.7 eV and the defect sites in the form of the carbon-oxygen bonding configuration such as C-O (BE = 286 eV), C=O (BE = 287.3 eV), and COOH (BE = 289 eV). Upon SAMs treatment, the sp³ hydrocarbon peak at 285 eV was added. The intensity of this peak was increased as introducing the SAMs with long alkyl chains. In addition, the FWHM values of the total C 1s line increase as SAMs treatment with long alkyl chains. These results imply that the sp² carbon atoms in graphene and the sp³ hydrocarbon from SAMs mainly contribute to the total C 1s line without any disruption of the sp² framework.

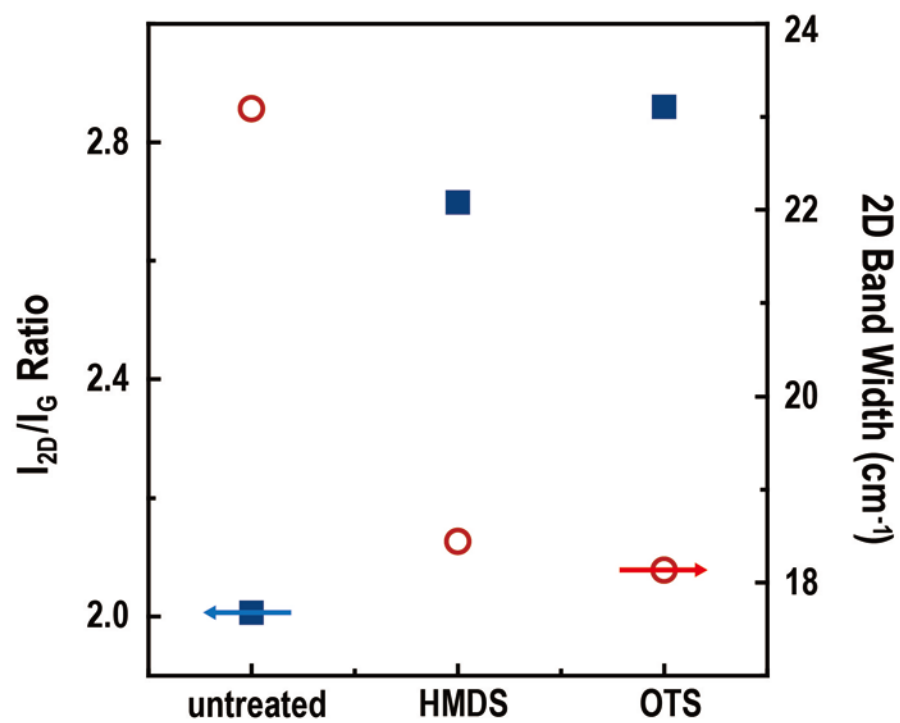


Figure S2. The intensity ratio between the 2D- and G-band (left-y axis) and the width of 2D-band of the graphene on untreated, HMDS treated, and OTS treated SiO₂.

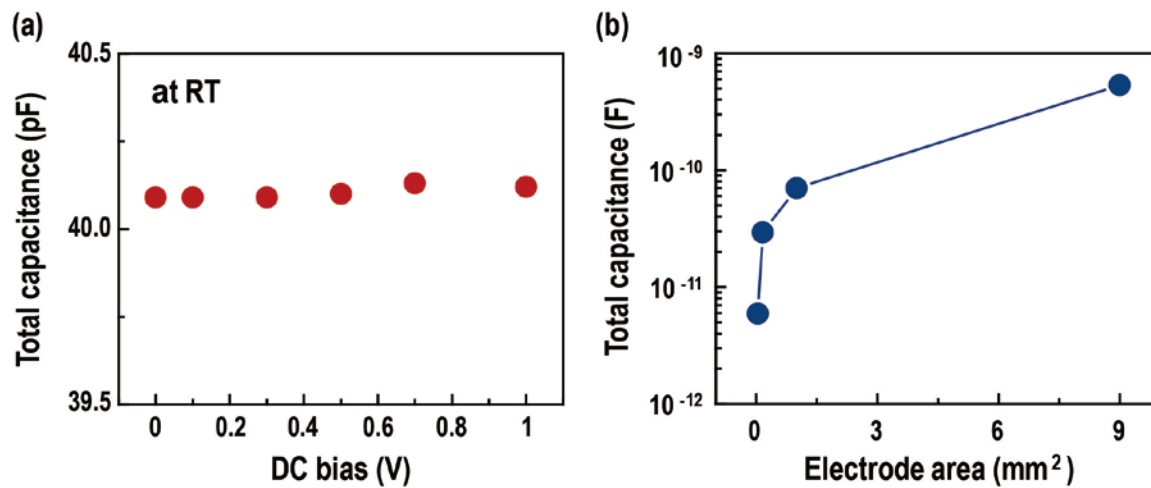


Figure S3. The fitting results of the total capacitance obtained from IS measurement with (a) applied dc bias at room temperature and (b) the area of contact electrodes.

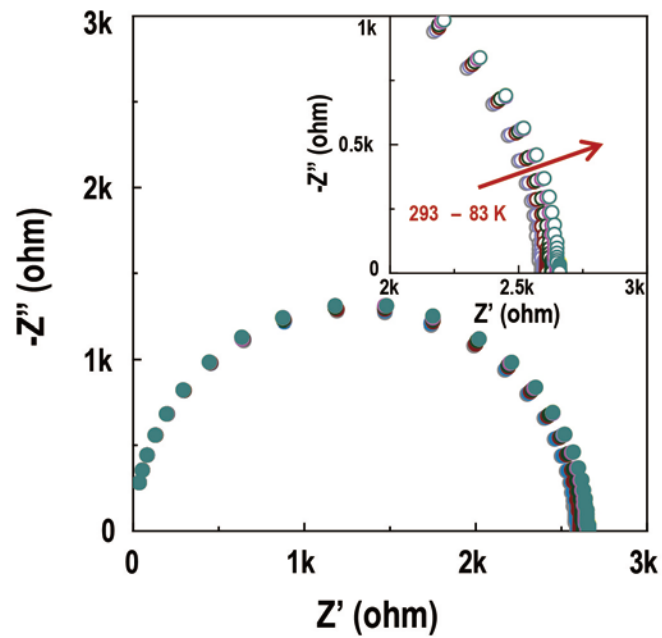


Figure S4. Nyquist plots from the graphene devices as a function of temperature in the range of 83 – 293 K. The inset shows the plots in the low frequency region.

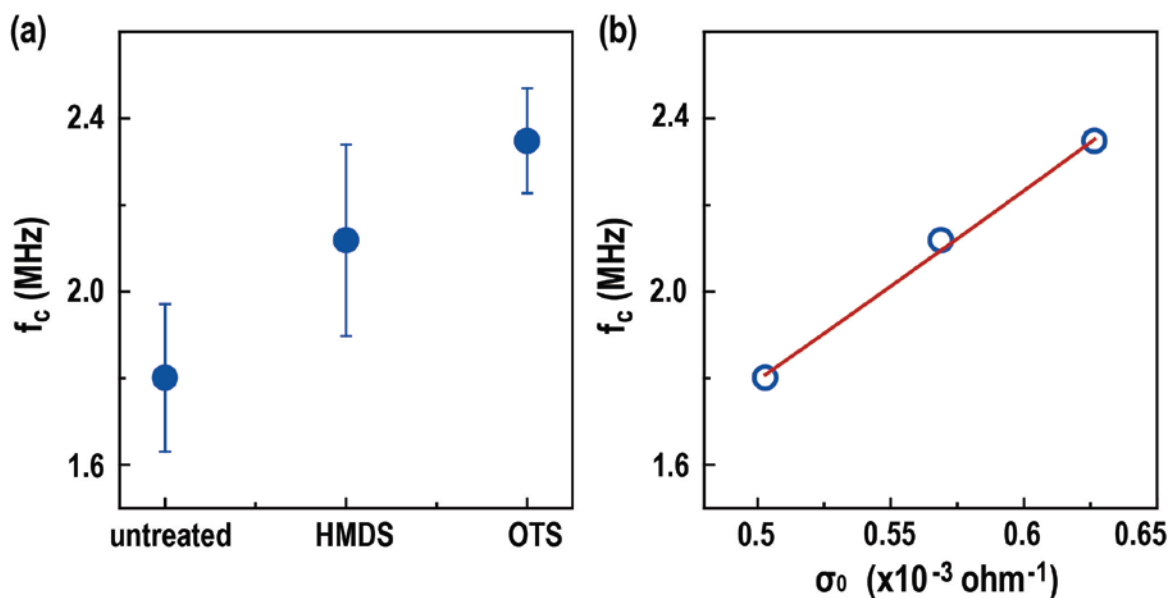


Figure S5. (a) Shift of the characteristic frequency f_c with different SiO₂ surface treatment. (b) The linear relation between the characteristic frequency f_c and the dc-conductance σ_0 .

REFERENCES

- [1] Kim, D. H.; Lee, H. S.; Yang, H.; Yang, L.; Cho, K. Tunable Crystal Nanostructures of Pentacene Thin Films on Gate Dielectrics Possessing Surface-Ordered Control. *Adv. Funct. Mater.* **2008**, 18, 1363-1370.