# Sulfidative Purification of Carbon Nanotubes Integrated in Transistors

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## Supporting Information

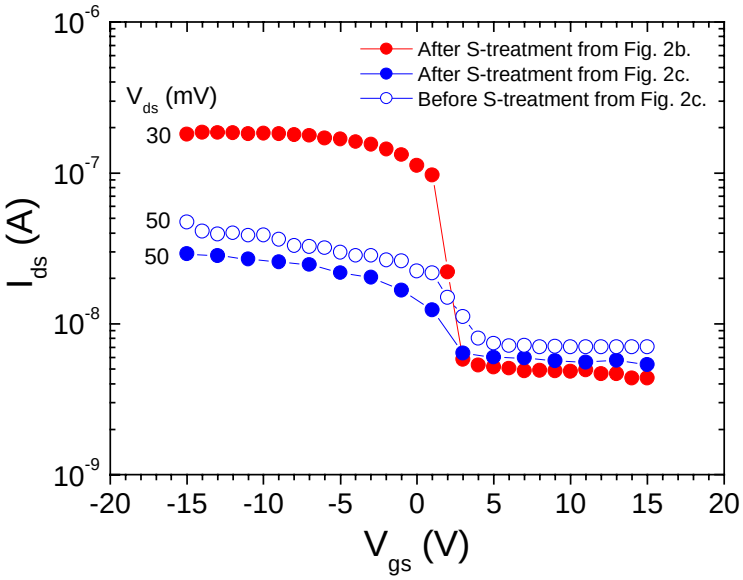


***Figure S1.*** $I_{ds}$ - $V_{gs}$ curves in a log scale before (open circles) and after (solid circles) sulfur treatment. Red and blue curves are re-plotted from Figure 2b and 2c, respectively. The transistor with high off-state current before the sulfur treatment turns on and off at 3V after treatment as shown with red circles in which the on-state and off-state currents are on the order of ~ $10^{-7}$ A and ~ $10^{-9}$ A, respectively. The normally operating transistor before the sulfur treatment shows nearly the same on-/off-state current ratio after the treatment (blue circles). Note that the small on/off ratios are attributed to the large diameter (~ 2 nm) of the nanotube integrated in the transistor [Ref S1].

**CNT-FET Fabrication Procedure**

Single-crystal Si substrate (*p*-type), with a resistivity of 0.005 ~ 0.01 Ωcm, were cleaned and coated with 300 nm of thermal $SiO_2$. Nanotubes were dispersed from a 1,2-dichloroethane solution by spinning onto the substrates after mild sonication. The concentration of the solution was adjusted to yield approximately one nanotube in an area of $5 \times 5$ $\mu m^2$. The spin-coating was performed with a rotation speed of 2000 rpm for 30 sec and subsequently 4000 rpm for 10sec. Alignment marks consisting of a metal dot array with ~ 1 μm spacing were fabricated to identify the location of a nanotube. A suitable nanotube was selected by using a scanning probe microcope. Once a suitable nanotube was found, its position was determined relative to the alignment marks. After generating patterns for metal contacts by electron-beam lithography, Pd electrodes of 100 nm were defined by lift-off process.

**Reference**

S1. Rakitin, A.; Papadopoulos, C.; Xu, J.M. *Phys. Rev. B* **2000**, *61*, 5793.