Supporting Information

Theoretical Study of Triboelectric-Potential Gated/Driven Metal-Oxide-Semiconductor Field-Effect-Transistor

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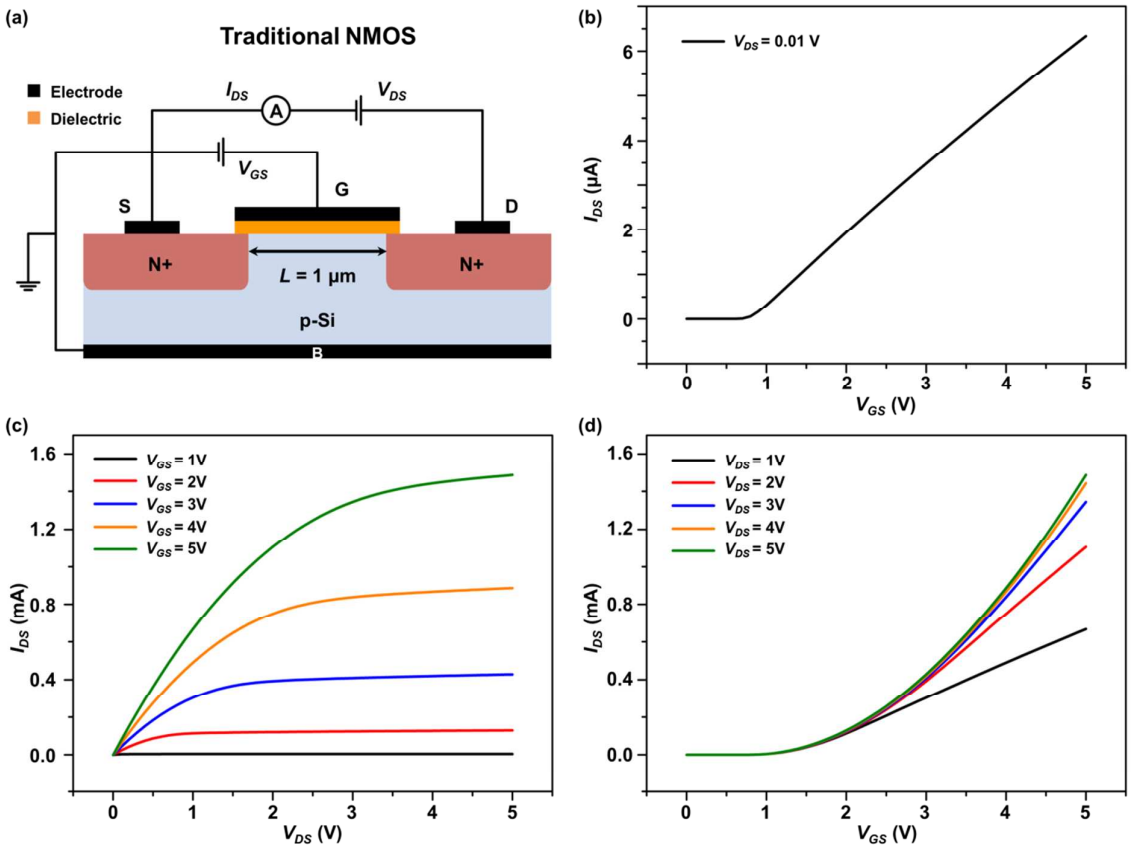

Figure S1. Traditional NMOS used in the simulation. (a) Schematic illustration of simulated traditional NMOS. (b-d) *I-V* characteristics of the traditional NMOS. I_{DS}-V_{DS} characteristic with a small V_{DS} bias of 0.01 V indicates the threshold voltage is 0.8 V.

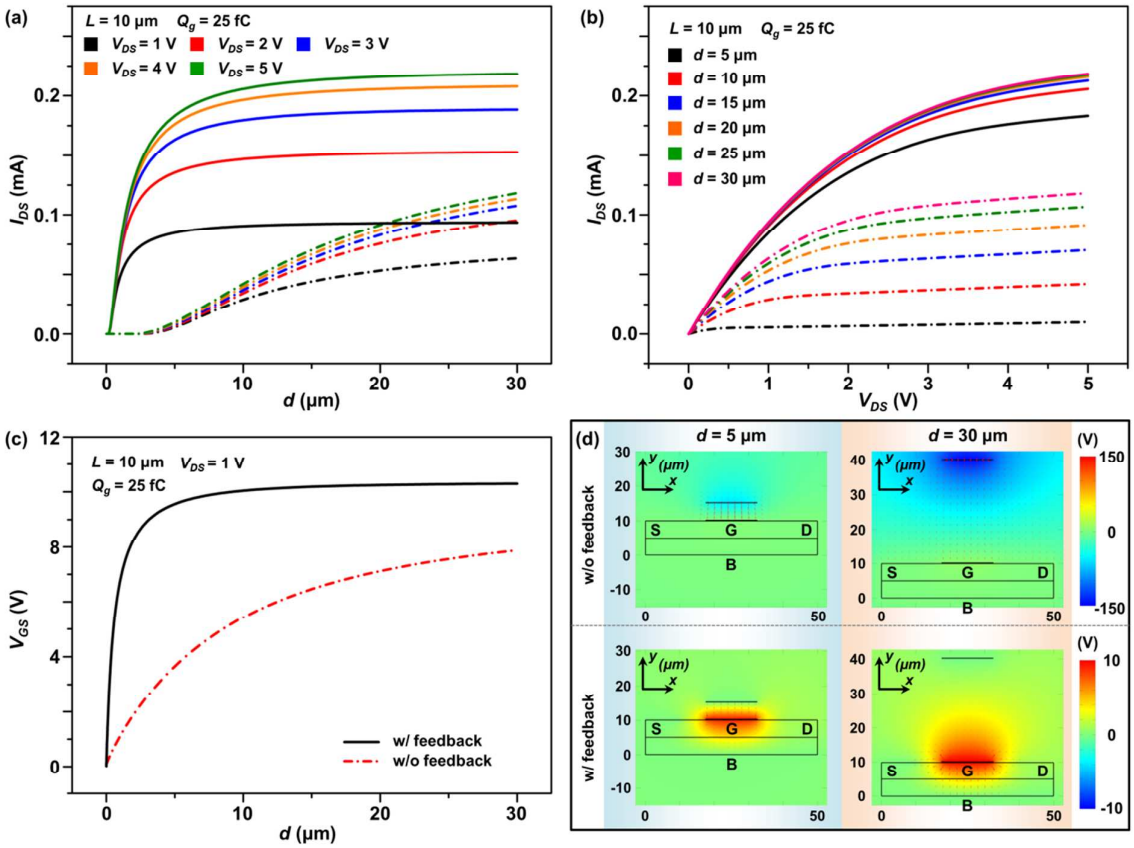

Figure S2. TPG NMOS with conduction channel length L of 10 μm and Q_g of 25 fC. (a) I_{DS}-d characteristic with different V_{DS} varying from 1 to 5 V. (b) I_{DS}-V_{DS} characteristic with different d varying from 5 to 30 μm. (c) V_{GS}-d characteristic with V_{DS} of 1 V. (d) Electric potential and electric field distribution with V_{DS} of 1 V under different d values: 5 and 30 μm.

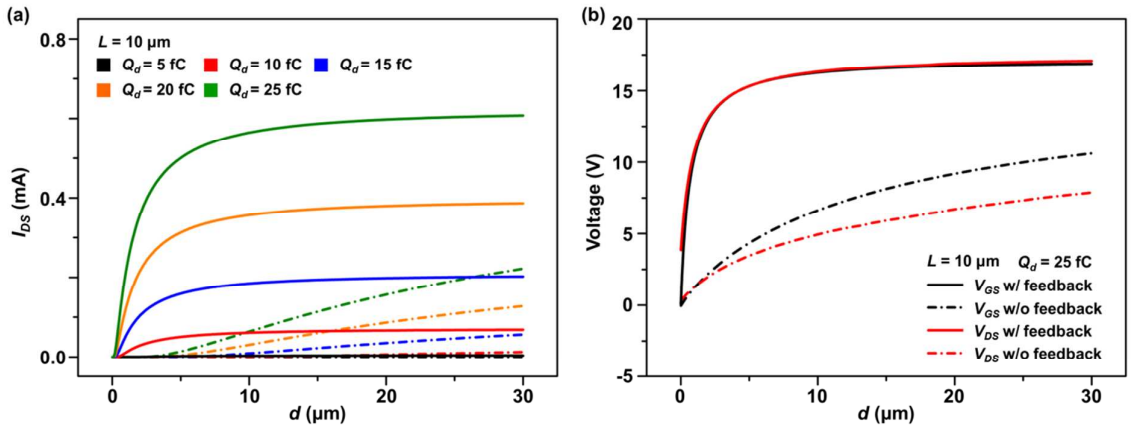

Figure S3. TPD NMOS with conduction channel length L of 10 μm. (a) I_{DS}-d characteristic with different Q_d varying from 5 to 25 fC. (b) V_{GS}/V_{DS}-d characteristics with Q_d of 25 fC.

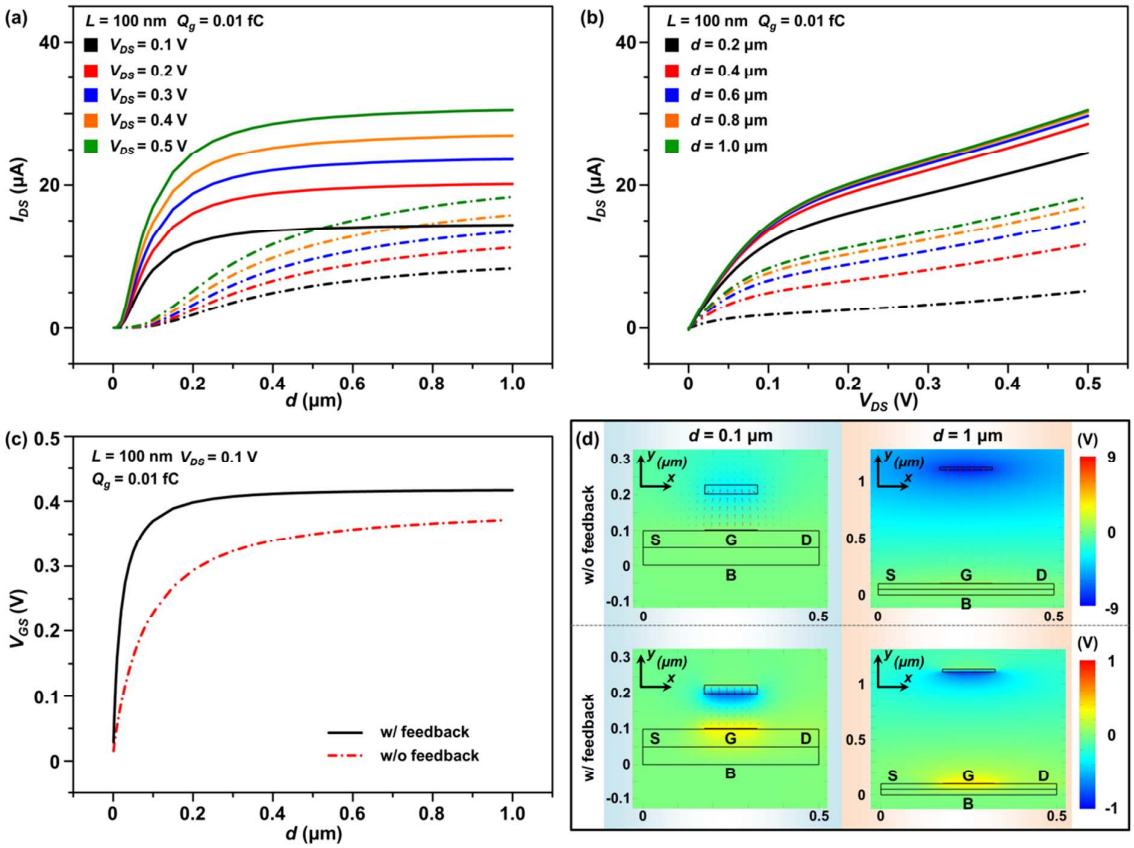

Figure S4. TPG NMOS with conduction channel length L of 100 nm and Q_g of 0.01 fC. (a) I_{DS}-d characteristic with different V_{DS} varying from 0.1 to 0.5 V. (b) I_{DS}-V_{DS} characteristic with different d varying from 0.2 to 1.0 μm. (c) V_{GS}-d characteristic with V_{DS} of 0.1 V. (d) Electric potential and electric field distribution with V_{DS} of 0.1 V under different d values: 0.1 and 1 μm.

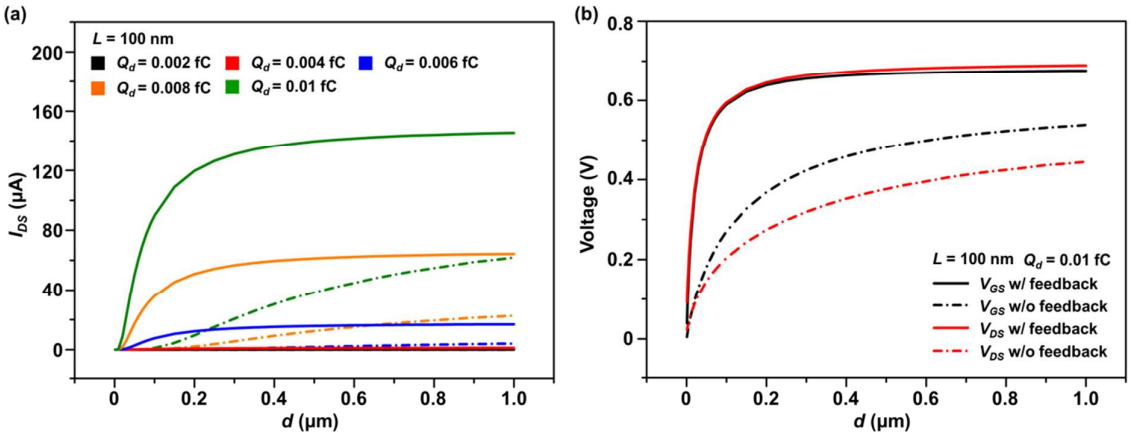

Figure S5. TPD NMOS with conduction channel length L of 100 nm. (a) I_{DS}-d characteristic with different Q_d varying from 0.002 to 0.01 fC. (b) V_{GS}/V_{DS}-d characteristics with Q_d of 0.01 fC.

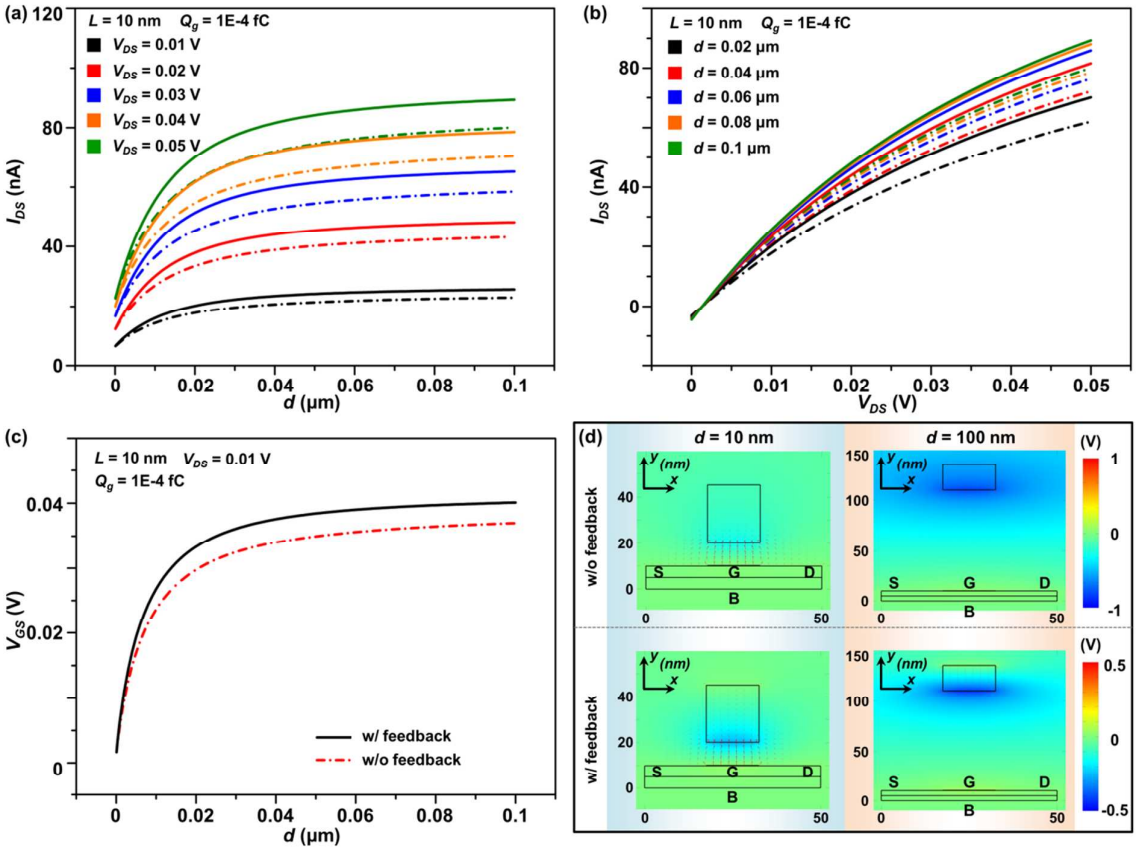

Figure S6. TPG NMOS with conduction channel length L of 10 nm and Q_g of 1E-4 fC. (a) I_{DS}-d characteristic with different V_{DS} varying from 0.01 to 0.05 V. (b) I_{DS}-V_{DS} characteristic with different d varying from 0.02 to 0.1 μm. (c) V_{GS}-d characteristic with V_{DS} of 0.01 V. (d) Electric potential and electric field distribution with V_{DS} of 0.01 V under different d values: 10 and 100 nm.

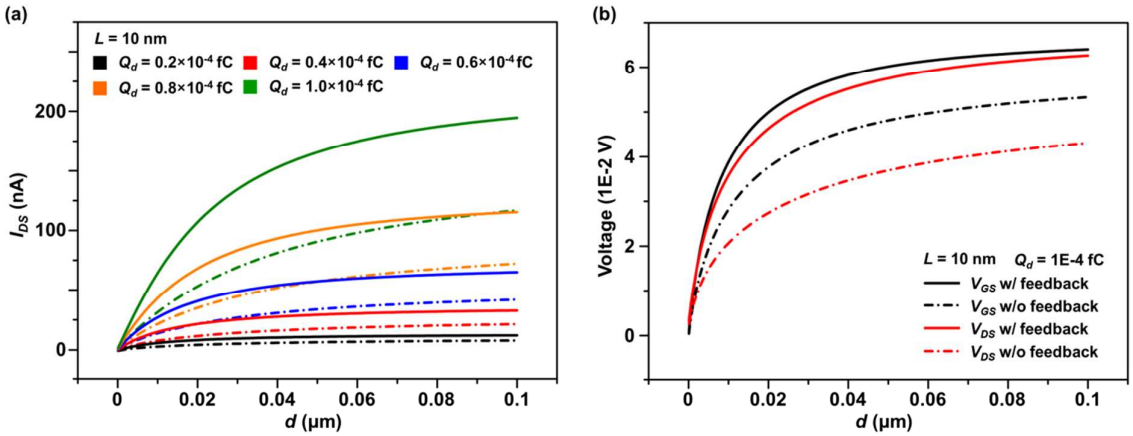

Figure S7. TPD NMOS with conduction channel length L of 10 nm. (a) I_{DS}-d characteristic with different Q_d varying from 0.2E-4 to 1.0E-4 fC. (b) V_{GS}/V_{DS}-d characteristics with Q_d of 1.0E-4 fC.

Supporting Information Note 1

Electrostatic discharge (ESD) is a major concern in advanced MOSFET devices. Triboelectric contact electrification is invariably prone to ESD events. Since our tribotronic transistors utilize triboelectric contact electrification and electrostatic induction to produce an electrostatically induced gate-source voltage V_{GS} acting as the gate voltage, it is definitely important to concern the electrostatic discharge (ESD) problem. In our tribotronic transistors, the major concern relating to ESD is the electrostatically induced voltages (V_{GS} in TPG NMOS, V_{GS} and V_{DS} in TPD NMOS), which are mainly dependent on the triboelectric charge amount Q and the separation distance d.

First, it is of great importance to control the electrostatically induced voltages being capable of driving the transistors but not causing ESD. The main concern is the effective control of the triboelectric contact electrification process, which determines the triboelectric charge amount Q. According to the simulated results shown in Figure S8, for both TPG and TPD NMOS operated at "w/o feedback" and "w/ feedback" modes, the I_{DS} as well as V_{GS} finally saturates to a maximum value ($I_{DS,max}$ and $V_{GS,max}$) when separation distance d is as large as 1 mm. The $V_{GS,max}$ is independent of the separation distance d and is determined by the triboelectric gate charge Q_g. Therefore, the minimum triboelectric gate charge $Q_{g,min}$ needed to drive the tribotronic transistors is determined by the condition $V_{GS,max} = V_{th}$. Here we only discuss the tribotronic transistors operated at "w/ feedback" mode since their $I_{DS,max}$ is larger than that of the transistors operated at "w/o feedback" mode. As illustrated in Figure S9a, the transferred charge Q equals the gate charge Q_g when the d is infinite, and then the charge distribution model can be simplified to the right part of Figure S9a. Under this condition, the

V_{GS} is the maximum $V_{GS,max}$ and its relation with the gate charge Q_g can be easily derived as follow:

$$Q_g = CV_{GS,max}$$

where $C = \frac{C_{GD}C_{Si}}{C_{GD}+C_{Si}}$ is the capacitance between the two electrodes, C_{GD} and C_{Si} are the capacitances of the gate dielectric and the silicon, respectively. Thus, the minimum gate charge $Q_{g,min}$ is:

$$Q_{g,min} = \frac{C_{GD}C_{Si}}{C_{GD}+C_{Si}}V_{th}$$

where V_{th} is the threshold voltage of transistors, which is 0.8 V in our simulation model. Then the $Q_{g,min}$ and corresponding triboelectric gate surface charge density $\sigma_{g,min}$ are derived as ~0.12 fC and ~80 μC m^{-2}.

The triboelectric surface charge density can be tuned/controlled by choosing appropriate mobile polymer materials according to the triboelectric series.[1] Moreover, surface functionalization[2] and modification[3] are two alternatives to control the triboelectric surface charge density. By these methods, we can carefully control the triboelectric gate surface charge density σ_g to produce V_{GS} over V_{th} for driving tribotronic transistors, but not to produce too large V_{GS} resulting in ESD problem.

Second, if the triboelectric gate surface charge density σ_g is too large beyond our expectation in practice and damages the tribotronic transistors, we can also design the tribotronic transistors with stacked gate dielectrics, as shown in Figure S9b. By stacking a thick (from tens of nanometers to even a few microns) high-κ dielectric over the conventional gate dielectric, only a small fraction of the total voltage caused by the triboelectric gate charge Q_g is applied across the conventional gate dielectric, while the rest is applied across

the high-κ dielectric. In this manner, ESD problems can also be prevented.

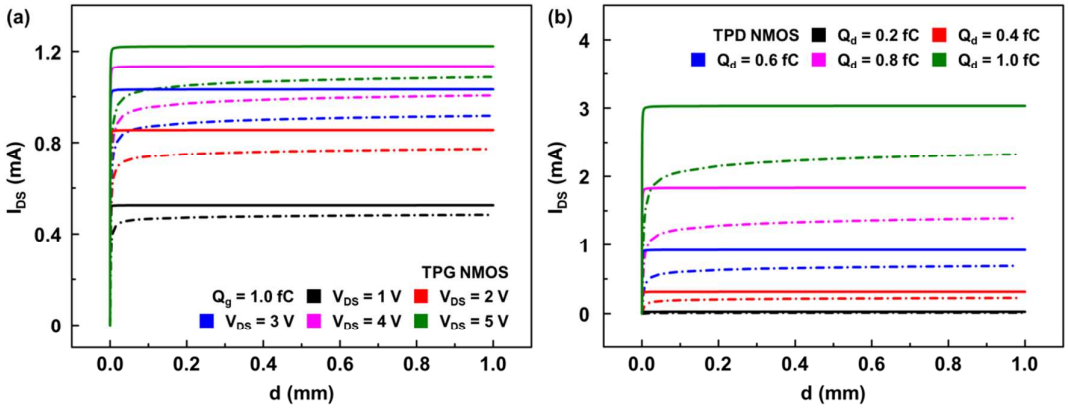

Figure S8. (a) I_{DS}-d characteristic of triboelectric-potential gated (TPG) NMOS with Q_g = 1.0 fC and V_{DS} bias from 1 to 5 V. (b) I_{DS}-d characteristic of self-powered triboelectric-potential driven (TPD) NMOS with Q_d from 0.2 to 1.0 fC. Conduction channel length L = 1 μm. Solid lines and dash dot lines correspond to the "with feedback" (w/ feedback) mode and the "without feedback" (w/o feedback) mode, respectively.

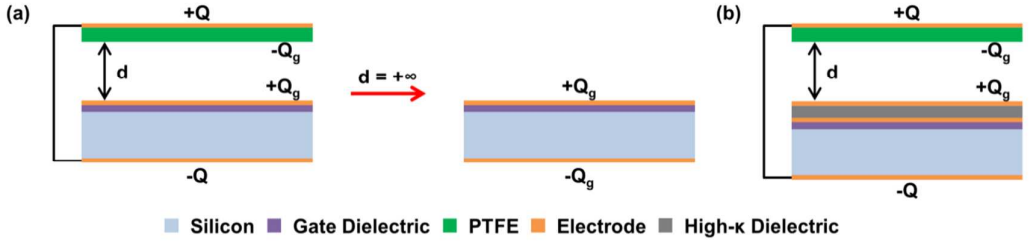

Figure S9. (a) Charge distribution in tribotronic transistors operated at "w/ feedback" mode. (b) Tribotronic transistors with stacked gate dielectric.

Supporting Information Note 2

We have simulated the triboelectric-potential gated (TPG) NMOS and the self-powered triboelectric-potential driven (TPD) NMOS with carrier mobility degradation by taking the effects of phonons, impurities, surface scattering and high electric field velocity saturation on carrier mobility into consideration.

In practice, the mobility is typically computed using analytic functions with or without a rigorous physical motivation and designed to fit the experimental data to a good degree of accuracy. Often, mobility models are designed to address one particular effect and require other mobility models as a basis. As an example, high electric field effects are often incorporated into a model by defining the high electric field mobility as a function of the mobility due to phonon and impurity scattering. Here, we combine phonon, impurity, surface scattering and high electric field mobility models in the following manner:

$$\mu_{tot} = \mu_E\big(\mu_S(\mu_{PI})\big) \tag{1}$$

where μ_{tot} is the total mobility, μ_E, the mobility due to high electric field effects, is a function of μ_S (the mobility due to surface scattering), which in turn is a function of μ_{PI} (the mobility due to phonon and impurity scattering).

The empirical mobility model derived by N.D. Arora et al.[4] is employed to include both phonon and impurity scattering. The electron ($\mu_{n,PI}$) and hole ($\mu_{p,PI}$) mobilities are determined by the equations:

$$\begin{cases} \mu_{n,PI} = \mu_{min,n} + \dfrac{\mu_{0,n}}{1+\left(\frac{N}{N_{0,n}}\right)^{\alpha}} \\ \mu_{p,PI} = \mu_{min,p} + \dfrac{\mu_{0,p}}{1+\left(\frac{N}{N_{0,p}}\right)^{\alpha}} \end{cases} \tag{2}$$

$$\begin{cases} \mu_{min,n} = \mu_{min,n}^{ref}\left(\frac{T}{T_{ref}}\right)^{\beta_1} \\ \mu_{min,p} = \mu_{min,p}^{ref}\left(\frac{T}{T_{ref}}\right)^{\beta_1} \end{cases} \tag{3}$$

$$\begin{cases} \mu_{0,n} = \mu_{0,n}^{ref}\left(\frac{T}{T_{ref}}\right)^{\beta_2} \\ \mu_{0,p} = \mu_{0,p}^{ref}\left(\frac{T}{T_{ref}}\right)^{\beta_2} \end{cases} \tag{4}$$

$$\begin{cases} N_{0,n} = N_{0,n}^{ref}\left(\frac{T}{T_{ref}}\right)^{\beta_3} \\ N_{0,p} = N_{0,p}^{ref}\left(\frac{T}{T_{ref}}\right)^{\beta_3} \end{cases} \tag{5}$$

$$\alpha = \alpha_0^{ref}\left(\frac{T}{T_{ref}}\right)^{\beta_4} \tag{6}$$

$$N = N_a^- + N_d^+ \tag{7}$$

where T is the lattice temperature, N_a^- is the ionized acceptor concentration, and N_d^+ is the ionized donor concentration. All the other parameters are the silicon material properties, which are taken from Ref. 4.

Then, the surface scattering mobility (μ_S) resulting from surface acoustic phonons and from surface roughness is combined with the phonon and impurity mobility (μ_{PI}). The electron ($\mu_{n,S}$) and hole ($\mu_{p,S}$) mobilities are determined by the following equations:[5]

$$\begin{cases} \frac{1}{\mu_{n,S}} = \frac{1}{\mu_{n,PI}} + \frac{1}{\mu_{n,ac}} + \frac{1}{\mu_{n,sr}} \\ \frac{1}{\mu_{p,S}} = \frac{1}{\mu_{p,PI}} + \frac{1}{\mu_{p,ac}} + \frac{1}{\mu_{p,sr}} \end{cases} \tag{8}$$

$$\begin{cases} \mu_{n,ac} = \frac{\mu_{n,1}}{\left(\frac{E_{\perp,n}}{E_{ref}}\right)} + \frac{\mu_{n,2}\left(\frac{N}{N_{ref}}\right)^{\alpha_n}}{\left(\frac{E_{\perp,n}}{E_{ref}}\right)^{1/3}\left(\frac{T}{T_{ref}}\right)} \\ \mu_{p,ac} = \frac{\mu_{p,1}}{\left(\frac{E_{\perp,p}}{E_{ref}}\right)} + \frac{\mu_{p,2}\left(\frac{N}{N_{ref}}\right)^{\alpha_p}}{\left(\frac{E_{\perp,p}}{E_{ref}}\right)^{1/3}\left(\frac{T}{T_{ref}}\right)} \end{cases} \tag{9}$$

$$\begin{cases} \mu_{n,sr} = \frac{\delta_n}{E_{\perp,n}^2} \\ \mu_{p,sr} = \frac{\delta_p}{E_{\perp,p}^2} \end{cases} \tag{10}$$

$$N = N_a^- + N_d^+ \tag{11}$$

where T is the lattice temperature, N_a^- is the ionized acceptor concentration, and N_d^+ is the ionized donor concentration, $E_{\perp,n}$ is the component of the electric field perpendicular to the electron current, and $E_{\perp,p}$ is the component of the electric field perpendicular to the hole current. All the other parameters are the silicon material properties, which are taken from Ref. 5.

At last, the high electric field mobility (μ_E) is included by utilizing the surface scattering mobility (μ_S) as the basis. The electron ($\mu_{n,E}$) and hole ($\mu_{p,E}$) mobilities are determined by the following equations:[6]

$$\begin{cases} \mu_{n,E} = \dfrac{\mu_{n,S}}{\left(1+\left(\dfrac{\mu_{n,S}F_n}{v_{n,sat}}\right)^{\alpha_n}\right)^{1/\alpha_n}} \\ \mu_{p,E} = \dfrac{\mu_{p,S}}{\left(1+\left(\dfrac{\mu_{p,S}F_p}{v_{p,sat}}\right)^{\alpha_p}\right)^{1/\alpha_p}} \end{cases} \tag{12}$$

$$\begin{cases} \alpha_n = \alpha_{n,0}\left(\dfrac{T}{T_{ref}}\right)^{\beta_{n,1}} \\ \alpha_p = \alpha_{p,0}\left(\dfrac{T}{T_{ref}}\right)^{\beta_{p,1}} \end{cases} \tag{13}$$

$$\begin{cases} v_{n,sat} = v_{n,0}\left(\dfrac{T}{T_{ref}}\right)^{\beta_{n,2}} \\ v_{p,sat} = v_{p,0}\left(\dfrac{T}{T_{ref}}\right)^{\beta_{p,2}} \end{cases} \tag{14}$$

where T is the lattice temperature, $F_n = E_{\parallel,n}$ and $F_p = E_{\parallel,p}$ currently are the driving forces for electrons and holes, $E_{\parallel,n}$ is the component of the electric field parallel to the electron current, and $E_{\parallel,p}$ is the component of the electric field parallel to the hole current. All the other parameters are the silicon material properties, which are taken from Ref. 6.

By linking different mobility models together as described above, we use the electron ($\mu_n = \mu_{n,E}$) and hole ($\mu_p = \mu_{p,E}$) mobilities, which contain all the contributions from the phonon, impurity, surface scattering and high electric field, in the simulation. Mobility models generally model the processes that remove or limit the momentum of carriers;

therefore a reduction in the drain-source current I_{DS} is expected when they are included in the simulation. Figure S10 and S11 show the results with constant mobility (solid lines) and with the added mobility models (dash dot lines) of TPG NMOS (Figure S10) and TPD NMOS (Figure S11), respectively. Obviously, for both TPG NMOS and TPD NMOS operated at "w/o feedback" mode and "w/ feedback" mode, the I_{DS} is significantly reduced; while the I_{DS}-V_{DS} and the I_{DS}-d relationships are still the same.

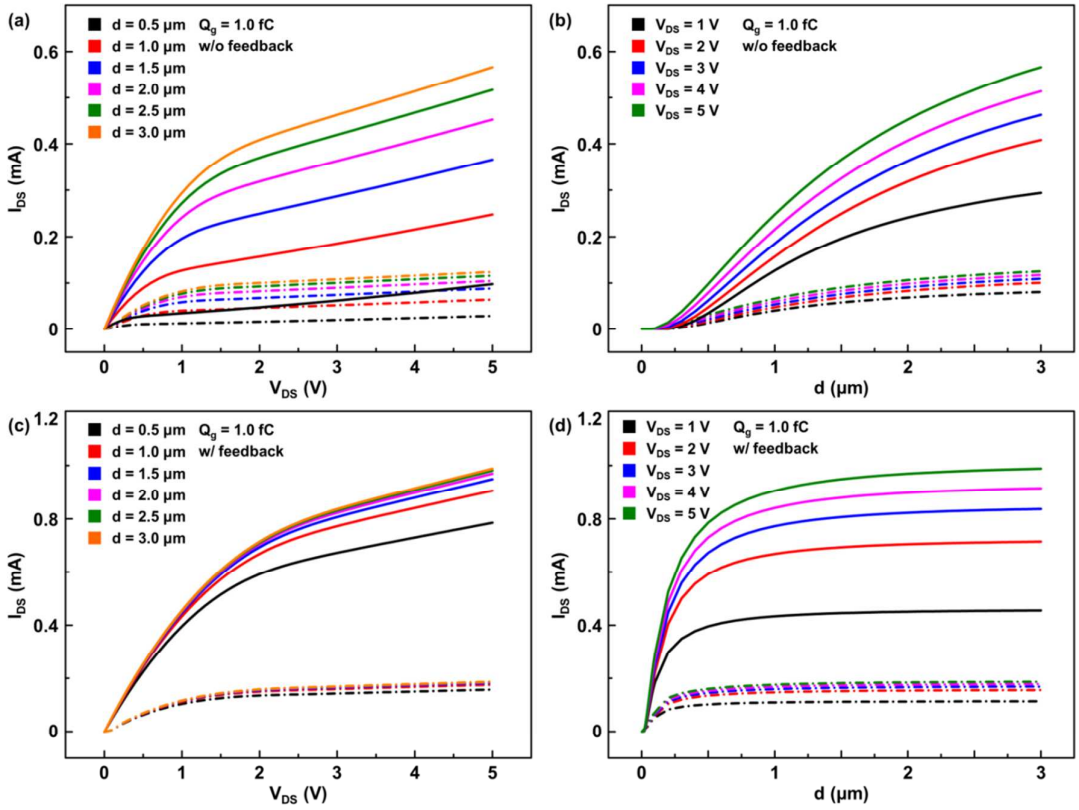

Figure S10. Characteristics of triboelectric-potential gated (TPG) NMOS with gate charge Q_g = 1.0 fC. I_{DS}-V_{DS} characteristics of TPG NMOS with separation distance d from 0.5 to 3.0 μm under (a) "w/o feedback" mode and (c) "w/ feedback" mode, respectively. I_{DS}-d characteristics of TPG NMOS with drain-source voltage V_{DS} from 1 to 5 V under (b) "w/o feedback" mode and (d) "w/ feedback" mode, respectively. Conduction channel length L = 1 μm. Solid lines and dash dot lines correspond to the simulated results without and with

considering the mobility models, respectively.

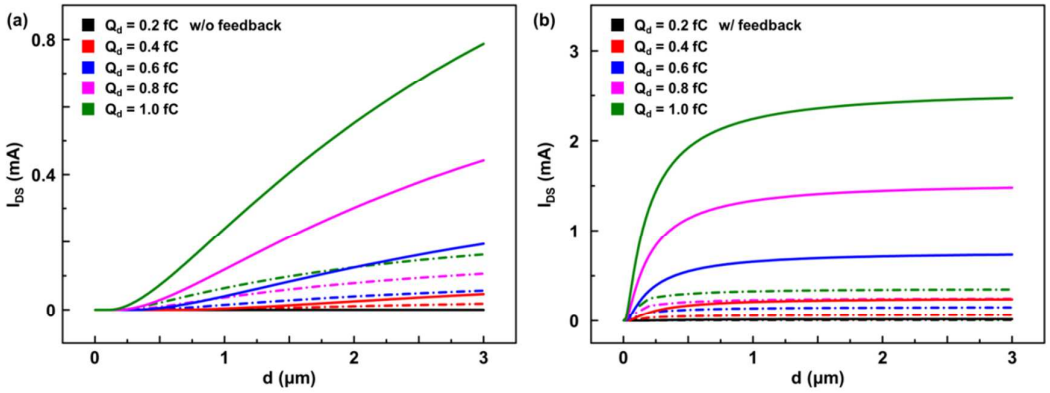

Figure S11. Characteristics of self-powered triboelectric-potential driven (TPD) NMOS with drain charge Q_d from 0.2 to 1.0 fC. I_{DS}-d characteristics of self-powered TPD NMOS under (a) "w/o feedback" mode and (b) "w/ feedback" mode, respectively. Conduction channel length L = 1 μm. Solid lines and dash dot lines correspond to the simulated results without and with considering the mobility models, respectively.

References

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