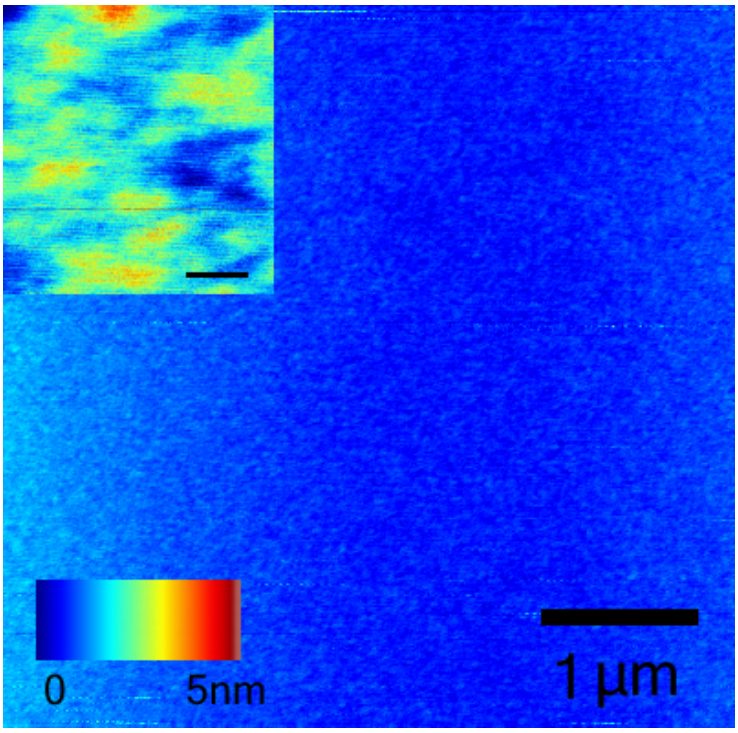


**Figure S1** Tapping-mode atomic force microscopy (AFM) image of the silicon substrate covered by the SAM. The layer is very smooth and pinhole free across large areas. **Inset** Zoom. The scale bar here is 20 nm, and the colour scale ranges from 0 to 0.5 nm.

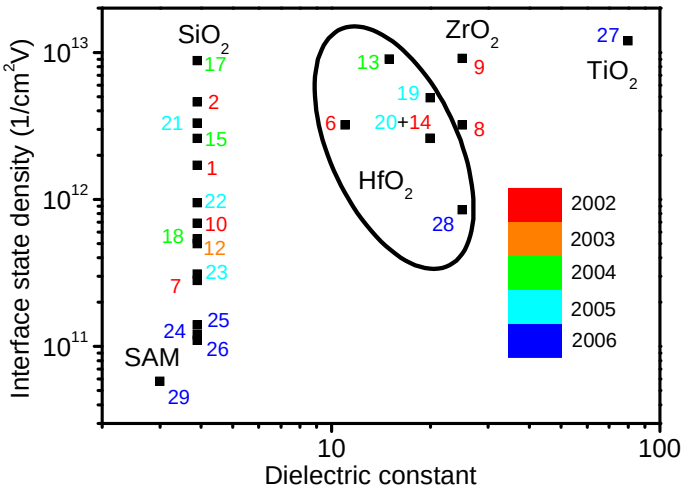


**Figure S2** Comparison of the interface state density of gate insulator materials with different dielectric constants. The interface state density N was calculated from the subthreshold swing S at room temperature and the capacitance per unit area C of the gate dielectric by the formula $N = (\log(e)*q*S/k_BT-1)*C/q$ with q as the electron charge, $k_B$ Boltzmann's constant and T as the temperature. The color scale indicates the respective year of the publication. It can be clearly observed that for materials of lower dielectric constant the interface state density is also lower. Furthermore a trend towards a lower interface state density over the years due to higher quality dielectrics is visible.

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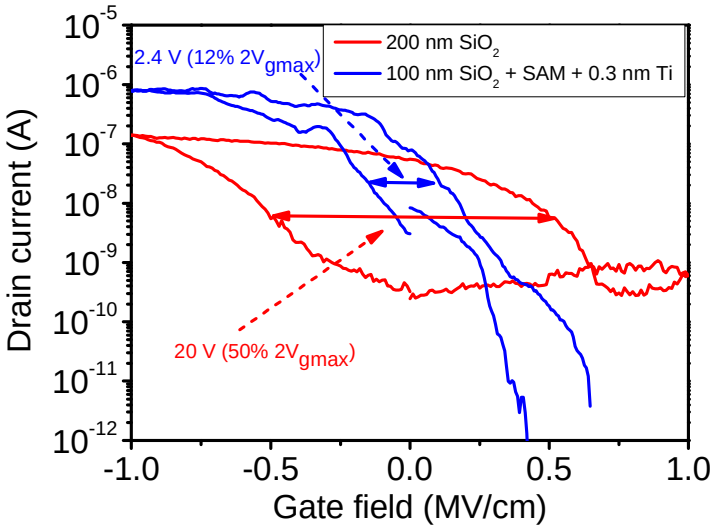


**Figure S3** Transfer curve of two devices: In red a SWCNT FET with a 200 nm $SiO_2$ dielectric. In blue a SWCNT FET with a 100 nm $SiO_2$ and a SAM on top. The hysteresis in this case is only 12% of the gate voltage window (determined by the difference between the minimum and maximum gate voltage) at a gate voltage sweep rate of 0.38 V/s (3.8 x $10^4$ V/cm s).