Supporting Information

Insights into the interfacial properties of low-voltage CuPc field-effect transistor

Yaorong Su[‡], Ming Ouyang[†], Pengyi Liu[†], Zhi Luo[§], Weiguang Xie[†*], and Jianbin Xu[‡*]

[†] Department of Physics, Siyuan Laboratory, Jinan University, Guangzhou, Guangdong, 510632, PR China

[‡] Department of Electronic Engineering and Materials Science and Technology Research Centre, The Chinese University of Hong Kong, Shatin, Hong Kong SAR, PR China

[§] Department of Electronic Engineering, Jinan University, Guangzhou, Guangdong, 510632, PR China

Experimental details:

Titanium oxide (TiO_x) sol was prepared by dissolving titanium (IV) isopropoxide (TIP) ($Ti(OC_3H_7)_4$, 99.99%, Aldrich) into a mixture of methanol and acetic acid in a volume ratio of about 1 : 30 : 1 (TIP : methanol : acetic acid), then sealed and vigorously stirred for 24 h before use. Aluminum oxide (Al_2O_y) sol was prepared by dissolving aluminum nitrate nonahydrate ($Al(NO_3)_3 \cdot 9H_2O$, 99.99%, Aldrich) into 2-methoxylethanol in a concentration of about 0.5 mol/L and then stirred for 12 h before use.

Before deposition of the dielectric layer, heavily n-doped Si wafers (n^{++}-Si) (acting as substrates and gate electrodes) were cleaned by acetone, isopropanol and ethanol ultrasonically for 10 min in each round, and then blown dry with N_2 gas and used immediately for the following dielectric layer deposition. The TiO_x layer was prepared by spin-coating the as-prepared TiO_x sol onto the cleaned n^{++}-Si substrates at 5000 r/min for 40 s, followed by baking at 200 ± 5 °C for 5 min to ensure the hydrolyzation and decomposition of the precursor. The thickness of the single TiO_x layer is about 12 nm as estimated by AFM depth profile. Subsequently, the Al_2O_y layer was deposited by spin-coating the previous Al_2O_y sol onto the cooled TiO_x-coated substrates and then

*Author to whom correspondence should be addressed, Weiguang Xie, email: weiguangxie@gmail.com; Jianbin Xu, email: jbxu@ee.cuhk.edu.hk;

baked at the same condition as that of TiO_x. As a result, the bilayer Al_2O_y/TiO_x dielectric system was obtained, and the thickness of the bilayer system is estimated to be about 45 nm through AFM depth profile.

In-situ KPFM characterization

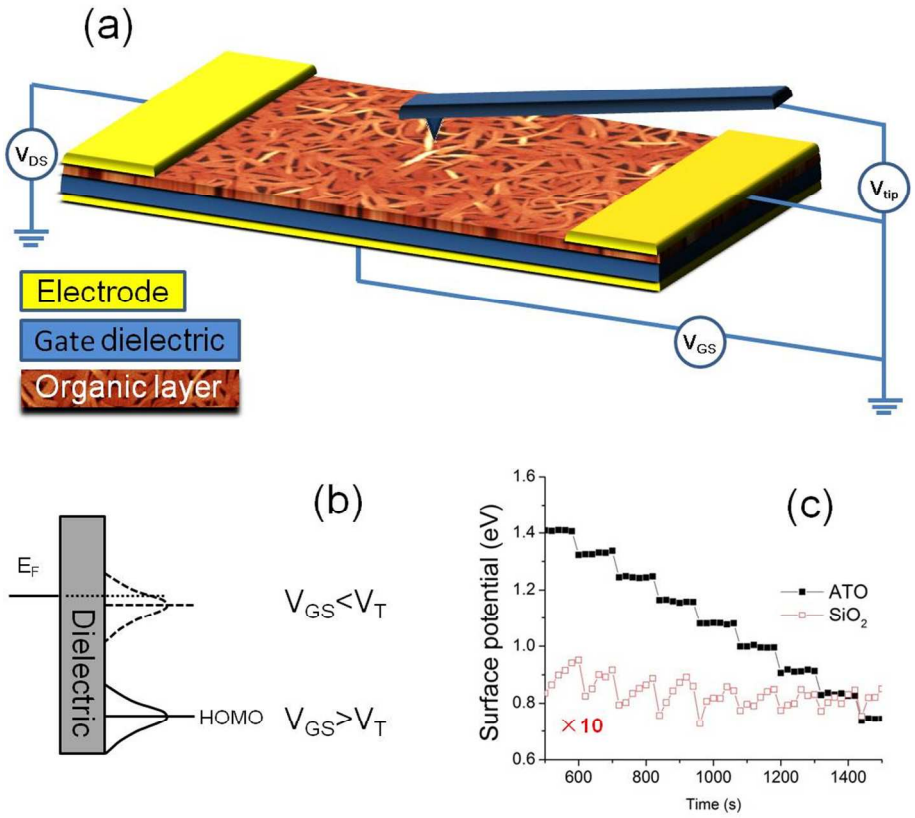


Figure S1 (a) Schematic setup of KPFM measurement on OFET; (b) HOMO shifting diagram at the interface; the solid line shows the HOMO position at $V_{GS}>V_T$; the dash line shows the HOMO position at $V_{GS}<V_T$; (c) Gate bias dependent surface potential curves, the gate bias changes every 120 second.

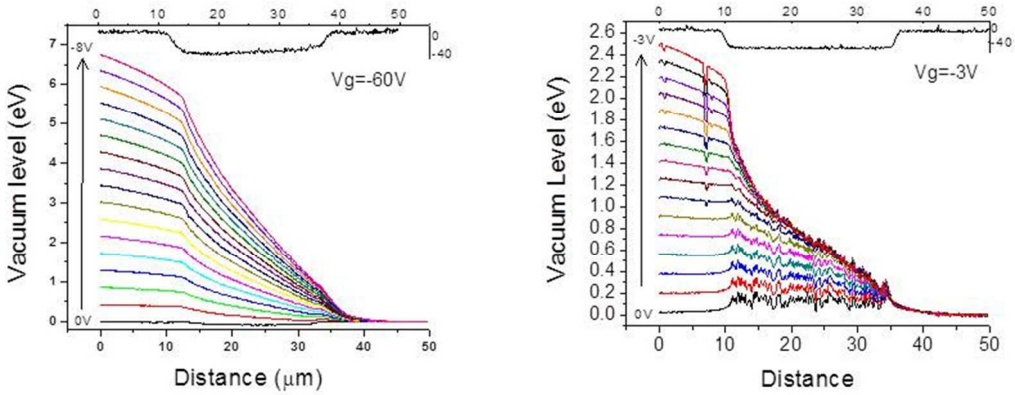
Figure S1 shows the schematic setup of KPFM measurement on the CuPc OFET. When measuring the channel resistance, a fix V_{GS} is applied and the V_{DS} is ramped step by step, during which the KPFM tip scans the surface from the source electrode to the drain electrode. The morphology and surface potential line profiles are recorded simultaneously. The I_{DS}-V_{GS} characteristic is also measured and used to calculate the resistance.

During DOS measurement, the source and drain electrodes are connected to the earth and the V_{DS} is altered. When a negative V_{GS} is applied, the interfacial HOMO band should be elevated. When the film is thin enough (<10 nm), the band bending effect inside the film can be ignored so that the surface potential change reflects the change of interfacial band shifting (Figure S1(b)). The interfacial density of states can be calculated using equation:

$$g(qV_L(x)) = \frac{C_{ox}}{d_{org}q^2}\left(\frac{d(V_{GS-}V_T)}{dV_L(x)} - 1\right)$$

where the $V_L(x)$ is vacuum level of the CuPc at the channel position x that measured by KPFM. C_{ox} is the capacitance density of the dielectric. For SiO_2, it is 11 nF/cm^2, and for ATO, it is 250 nF/cm^2. The parameter d_{org} is the thickness of the organic semiconductor, and q is the electron charge. V_{GS} is the gate bias and the V_T is the threshold voltage that can be measured from the transfer curve. For the detail theoretical description, please refer to Ref. [1, 2].

In our experiment, the KPFM scanning speed is reduced to 0.1 Hz to ensure high energy resolution and to avoid collision of the tip. In Figure S1 (c), the jump of surface potential is induced by the step addition of V_{GS}. The surface potential of CuPc on ATO substrate keeps constant if the V_{GS} is not changed. In the case of CuPc on SiO_2, the change of V_{GS} induces smaller modulation to the surface potential. Especially, pinning effect is observed, where the change of V_{GS} cause the sudden decrease of surface potential immediately, but then reversed slowly to the initial value. The observation indicates generation of trap states due to the gate bias stress [3]. The time scale of the measurement is in the order of 10^2 s, so the results reflect the steady states of the device.



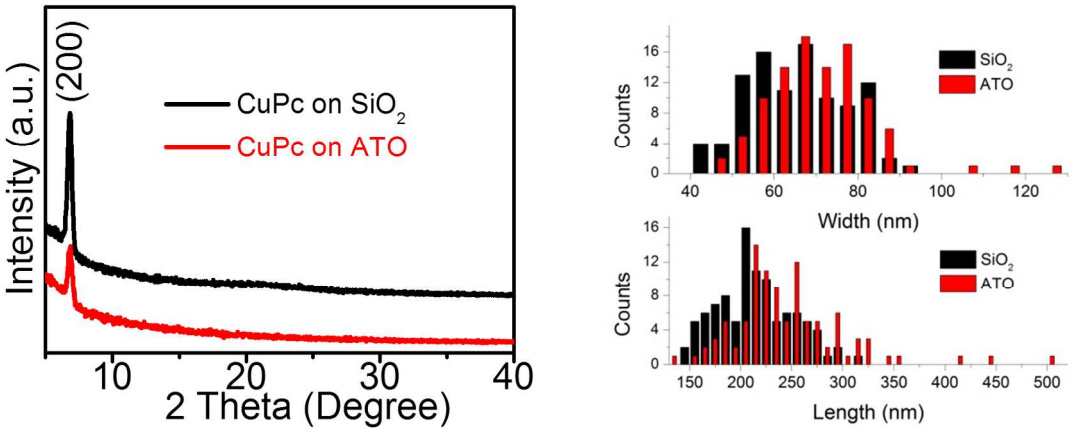
(a) (b)

Figure S2 Surface potential profiles along the channel of 5-nm-thick CuPc/SiO_2 (a) and CuPc/ATO (b) devices respectively.

Surface potential profiles along the channel at different V_{DS} are shown in Figure S2. Transition from linear to saturation range can be observed in CuPc/ATO device. The pinch-off effect at the drain electrode is clear at V_{DS}<-1.5V, when the applied bias manily drop at the drain electrode. The electrical field in the channel and the mobility no longer change. Due to the limitation of the KPFM, a maximum V_{DS}=-8V is used in measurement of the CuPc/SiO_2 device. The pinch-off effect at the drain electrode is not clear.

Near the source electrode, the potential drop along the channel changes linearly with increasing V_{DS}. The electrical field and mobility are calculated from this area.

Structure characterization



(a) (b)

Figure S3. (a) XRD patterns of 25 nm CuPc film on the two types of dielectrics; (b) size of the CuPc crystal domains at the interface.

Figure S3 (a) shows the XRD patterns of 25-nm-thick CuPc thin films deposited on SiO_2 and ATO at substrates. A single sharp reflection peak at 2θ of 6.9° assigned to the (200) plane of α-phase CuPc can be observed from both patterns. The interface domain sizes are statistically estimated from AFM topography of the 5-nm-thick films. For each film, 100 domains are taken for the estimation. Figure S3 (b) shows that the domain width and length of CuPc on ATO substrate is slightly bigger than that on SiO_2 substrate.

Transfer curvess of CuPc/ODPA/ATO OFET

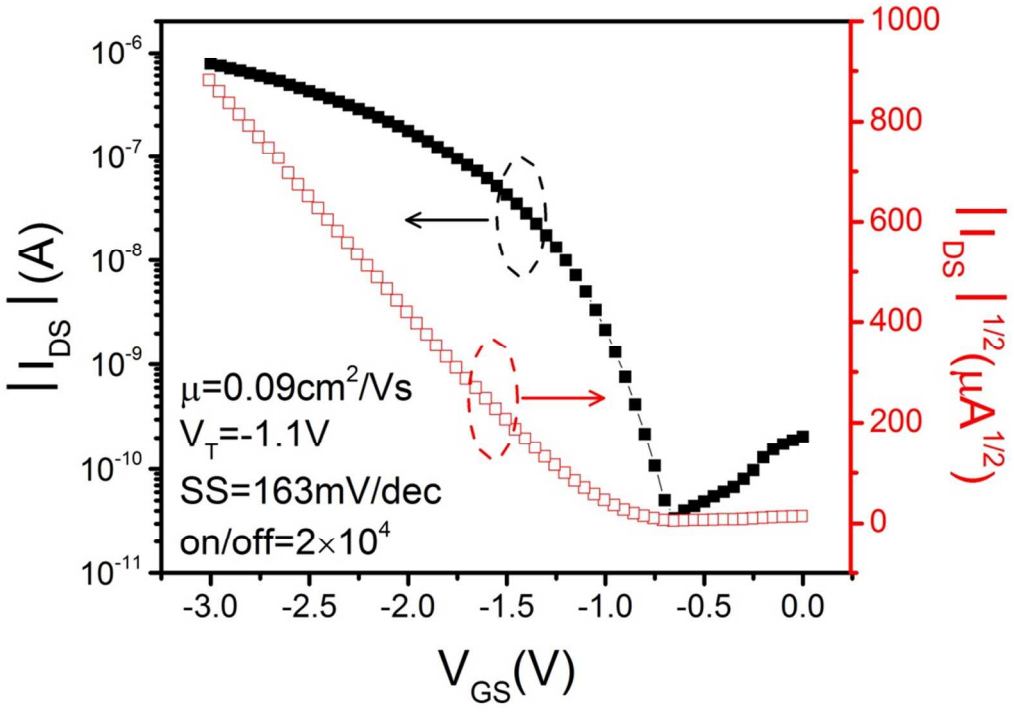


Figure S4 Transfer curvess of 25-nm-thick CuPc/ODPA/ATO OFET in ambient condition

References

(1) Tal, O.; Rosenwaks, Y.; *J. Phys. Chem. B* **2006,** *110*, 25521.

(2) Tal, O.; Rosenwaks, Y.; Preezant, Y.; Tessler, N.; Chan, C. K.; Kahn, A.; *Phys. Rev. Lett.* **2005,** *95*, 256405.

(3) Goldmann, C.; Gundlach, D. J.; Batlogg, B.; *Appl. Phys. Lett.* **2006,** *88*, 063501.