

Interfacial Charge Transfer and Gate Induced Hysteresis in Monochalcogenide InSe/GaSe Heterostructures

Supporting Information

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1. Additional data for charge transfer experiment

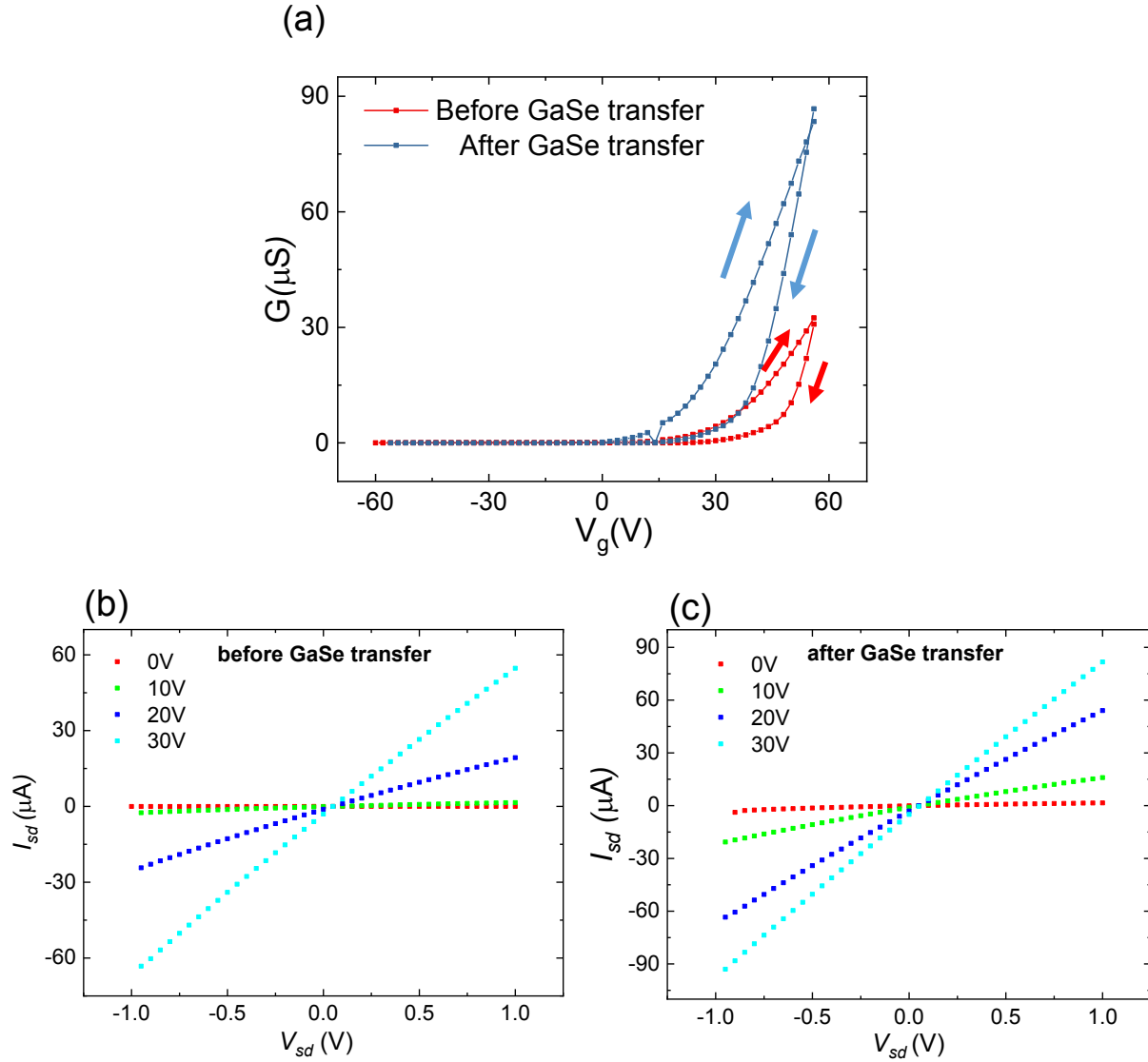


FIGURE S1 (a) Gate-transfer curves (V_g scanning rate = 13.33 V/s) before and after GaSe transfer for an additional sample (InSe sample 2) – sample structure and experiment is the same as described in Figure 2 in main text. Arrows indicate V_g scanning directions. (b),(c) I-V characteristics of an InSe FET device (InSe Sample 1 – Figure 2 in main text) before and after GaSe transfer and anneal, respectively. Applied V_g values are indicated in the plots.

2. Gate-transfer characteristics of bare InSe and GaSe devices

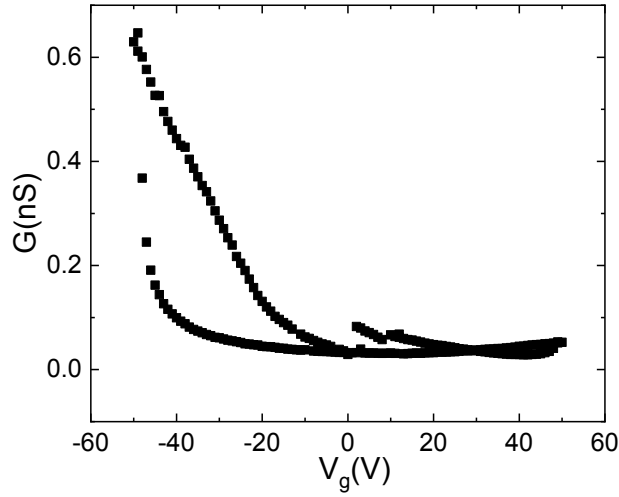


FIGURE S2 Room temperature gate-transfer characteristics at $V_{sd}=1V$ for a bare GaSe device on 300 nm SiO_2 substrate (V_g scanning rate = 13.33 V/s).

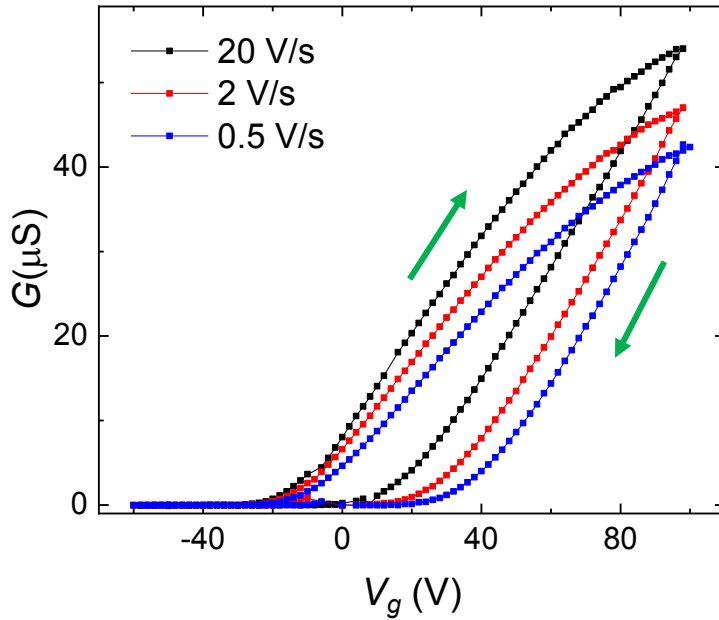


FIGURE S3 Room-temperature gate-transfer characteristics at $V_{sd} = 0.1V$ for bare few-layer (20 nm thick) InSe FET at different scanning rates, measured in vacuum of 50 mTorr (Arrows indicate V_g scanning directions). These measurements were done on devices fabricated and annealed under the same conditions as described for the InSe/GaSe heterostructures in main text.

It is to be noted that, in Figure S3, we have used a wider range of scanning rates than in the main text to clearly indicate the scanning rate dependence. The scanning rate dependence observed here is more than 10 times weaker than in Fig.3(c) in main text.

3. I-V characteristics of InSe-GaSe heterostructures

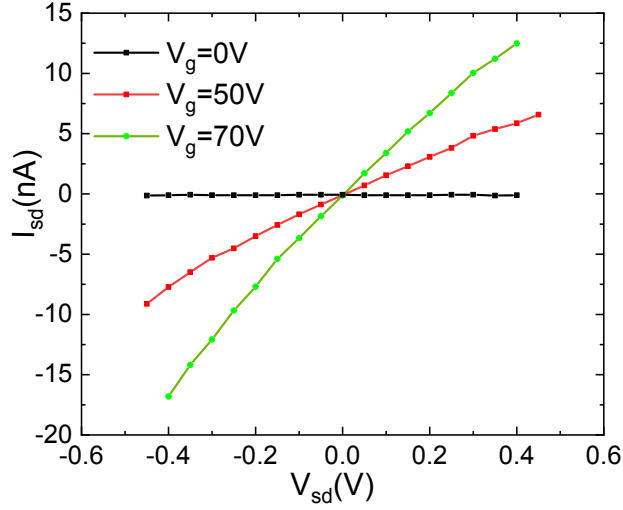
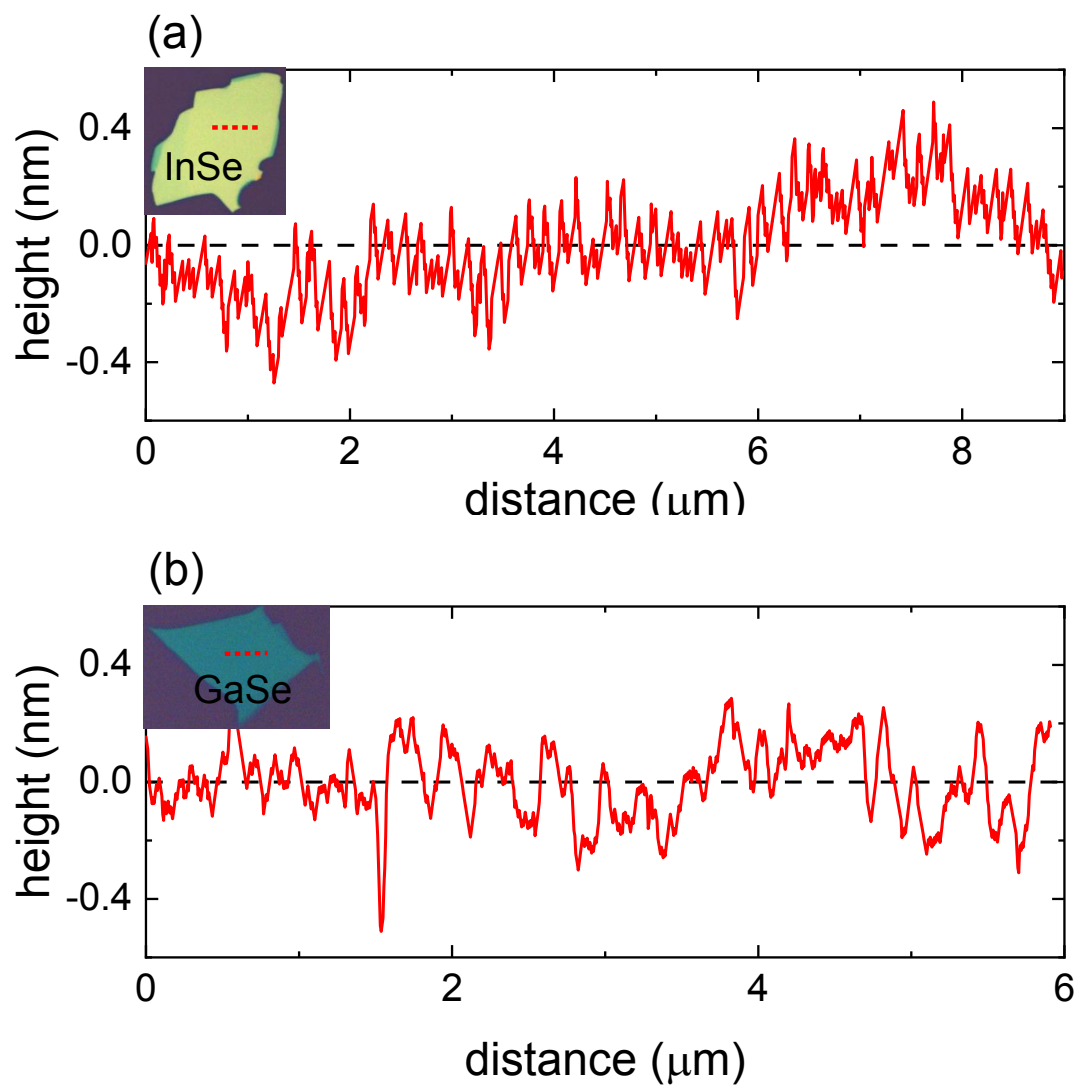


FIGURE S4 Room temperature I-V characteristics at different gate-voltages for the InSe-GaSe heterostructure sample shown in Figure 3 in main text. For each set gate-voltage value, source-drain voltage was swept from -0.5V to 0.5V in 1s, before setting the next gate-voltage value. I-V scans were done from low to high gate-voltage.

4. Surface characterization of InSe and GaSe nanoflakes



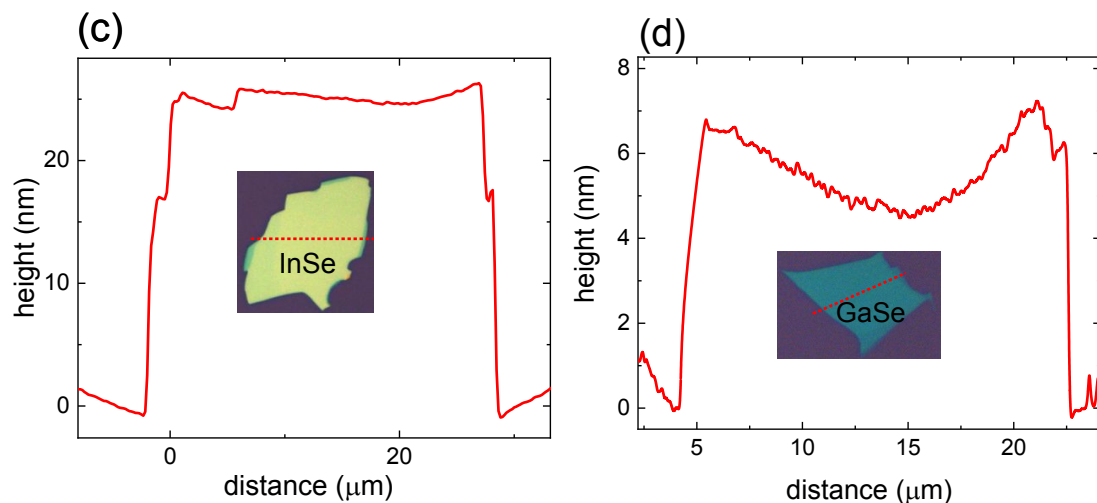


FIGURE S5 Atomic Force Microscopy surface characterization of (a) InSe and (b) GaSe nanoflakes from the same bulk crystals and exfoliated using the same methods as used in this study. Red dotted line in inset image of flakes marks the scan region. (c),(d) show corresponding scans to estimate flake thickness.

Note that the AFM scans shown in Figure S5(c) and (d) were done at a lower resolution over a larger thickness range with the purpose of estimating flake thickness and therefore do not reflect the actual surface profile of the flakes. Flake thickness: InSe – 25 nm, GaSe – 6 nm.

5. Temperature dependent gate-transfer characteristics of InSe-GaSe heterostructures

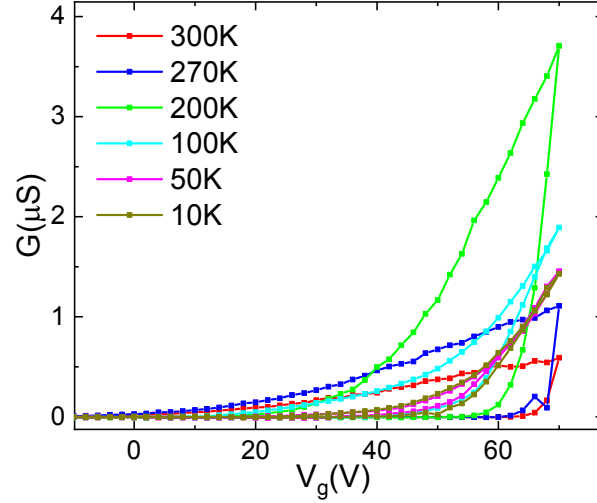


FIGURE S6 Gate-transfer curves (V_g scanning rate = 13.33 V/s) at different temperatures for InSe-GaSe heterostructure sample – same data as shown in Figure 6 in main text, device structure in Figure 3 of main text.

6. Band bending calculations

In the experiment shown in main text (Figure 2 in main text), placing a GaSe flake on top of a device with a conducting InSe channel was shown to result in a negative threshold voltage shift ΔV_{TH} in the gate-transfer curve.

For a given shift in the threshold voltage, we can calculate the corresponding change in carrier density in the device channel Δn using the equation

$$\Delta n = C_g \Delta V_{TH} \quad (1)$$

Where C_g is the gate capacitance per unit area. Δn represents the density of charge carriers transferred from GaSe to InSe, in this case. For a 2D system of electrons/holes (as is the case in gate confined electrons in our devices), we can calculate the corresponding change in Fermi energy ΔE_F using

$$\Delta E_F = \frac{\pi \hbar^2}{m^*} \Delta n \quad (2)$$

Where m^* is the effective mass of the active channel material (in our case, InSe). For our InSe/GaSe heterostructure devices, the corresponding energy shift due to band bending is given by $\Delta E_B = \frac{\Delta E_F}{2}$.

For heterostructures with InSe on top of GaSe (Figure 3 in main text), when a small gate voltage V_g is applied, there are only a small number of carriers in InSe and both InSe and GaSe can be treated as dielectrics. The potential drop across each of the layers (InSe, GaSe) of the heterostructure device is given by:

$$\Delta V_{InSe} = \frac{C}{C_{InSe}} V_g \quad (3)$$

$$\Delta V_{GaSe} = \frac{C}{C_{GaSe}} V_g \quad (4)$$

Where C is the equivalent gate capacitance of the device, given by:

$$C^{-1} = C_{SiO_2}^{-1} + C_{InSe}^{-1} + C_{GaSe}^{-1} \quad (5)$$

Where $C_i = \kappa_i \epsilon_0 / d_i$ for $i \equiv InSe, GaSe, SiO_2$

Here, κ_i is the static dielectric constant of each layer, d_i is the layer thickness and ϵ_0 is vacuum permittivity.

At $V_g = 10V$, for a 40 nm layer of InSe ($\kappa_{InSe} = 8.0$) on 20 nm layer GaSe ($\kappa_{GaSe} = 7.6$) and 300 nm SiO_2 ($\kappa_{SiO_2} = 3.9$), assuming uniform electric field in these layers, we find $\Delta V_{InSe} = 0.6V$ and $\Delta V_{GaSe} = 0.3V$.

Therefore, at $V_g \sim 10V$, Conduction Band Minimum (CBM) in InSe bends down by ~ 0.6 eV. We estimate 10V as the V_g where the InSe's CBM meets the Fermi level E_F at the InSe/GaSe interface and significant accumulation of electrons in InSe happens (the observed $V_{TH} \approx 10V$ in bare InSe (Figure 2c in main text) is consistent with this estimate since the GaSe dielectric does not influence the total C much).

Further increasing V_g fills electrons in the CB of InSe, which behaves like a conductor. At $V_g \approx 10V$, GaSe still behaves like an insulator since the dip in its CBM is still significantly higher than InSe's E_F . Therefore, increasing V_g beyond 10V,

$$C^{-1} = C_{SiO_2}^{-1} + C_{GaSe}^{-1} \quad (6)$$

Using this to estimate the band bending in GaSe at $V_g > 10V$, we estimate that, at $V_g = 30V$, CBM in GaSe dips down by 0.9 eV, which brings it in contact with InSe's E_F as well (Figure 6b in main text).

Therefore, for $V_g > \sim 30V$, electrons can accumulate in GaSe, which behaves like an electron trap (Figure 6c in main text).

7. Interfacial charge transfer model

In the following section, we propose an interfacial charge transfer model with the objective of getting an order estimate of the time scales of conductance decay (observed in Figure 4 in main text) due to thermionic emission and tunneling processes.

Consider the experiment shown in Figure 4(a) in main text, where the InSe-GaSe heterostructure device (Figure 3(a)) is subjected to a sudden increase in V_g from 0V to 50V.

Immediately after we apply $V_g = 50\text{V}$, the gate-induced electrons in InSe ($\cong 10^{12}/\text{cm}^2$ at $V_g = 50\text{V}$) experience an electric field given by $E = \Delta V_{\text{InSe}}/t$ where $t = 40\text{ nm}$ is the thickness of the InSe flake. As shown in the previous section, we can estimate ΔV_{InSe} from the capacitance of the individual layers in the heterostructure (It is to be noted that the gate-induced carriers will modify the electric field through this layer which will then have to be treated self-consistently. However, for the sake of this simple model, we will consider a constant electric field determined by the dielectric properties of InSe).

The electrons experiencing this electric field will travel towards the InSe/GaSe interface with an average group velocity determined by the diffusion of these electrons through the layers. This is given by

$$\langle v \rangle = \mu_z E \quad (7)$$

Where μ_z is the electron mobility in the z-direction (perpendicular to the 2D layers). We estimate μ_z from our measured room temperature field-effect mobility in the x-y plane ($\mu \sim 100\text{ cm}^2/\text{V.s}$) using $\mu_z = \mu \times m_x^*/m_z^*$, where m_x^* and m_z^* are the effective masses of InSe along and perpendicular to the 2D layers, respectively ($0.14 m_e$ and $0.08 m_e$ respectively¹). From this mobility and the carrier density at $V_g = 50\text{V}$, we also estimate the mean free path $l = 2\text{ nm}$, which validates our diffusive model since $l \ll t$.

In this proposed model, we can calculate the rate of change of 2D carrier density n in the InSe layers due to the applied gate-electric field by

$$\frac{dn}{dt} = -n_{3D} \langle v \rangle T(\langle \epsilon \rangle) \quad (8)$$

Where $n_{3D} \cong n/t$ is the 3D density of electrons in InSe and $T(\epsilon)$ is the transmission coefficient of electrons through the interface as a function of electron energy ϵ (which is the probability of an electron having energy ϵ passing through the interface). The right-hand side of the equation therefore determines the rate of electrons per unit area that pass through the interface. We can see that this equation predicts an exponential decay in density, with a time constant

$$\tau = \frac{t}{\langle v \rangle T(\langle \epsilon \rangle)} \quad (9)$$

We note that the time-constant for the decay in conductance is the same as above since $G = ne\mu \left(\frac{L}{W}\right)$, where L and W are device dimensions.

For thermionic emission, we have

$$T_{th}(\epsilon) = e^{-\frac{E_b - \epsilon}{k_b T}} \quad (10)$$

Where E_b is the energy barrier seen by the electrons (Here, 0.9 eV) and $T=300\text{K}$.

For tunneling (through an approximately triangular barrier given by potential profile shown in Figure 7(c) in main text), the transmission coefficient is found through the WKB approximation for Fowler-Nordheim tunneling.

$$T_{tun}(\epsilon) = \exp\left(-\frac{8a}{3}\sqrt{\frac{2mE_b}{\hbar^2}}\left(1 - \frac{E_b - \epsilon}{E_b}\right)^{\frac{3}{2}}\right) \quad (11)$$

Where $E_b=0.9\text{ eV}$ and $a \simeq 15\text{ nm}$ are the height and width, respectively, of the triangular barrier at $V_g=50\text{V}$.

Since these coefficients depend on the energy of each electron, we calculate them at the average energy of electrons in our system, to simplify calculations. This is given by :-

$$\langle e \rangle \simeq \int_0^\infty \epsilon e^{-\frac{\epsilon - \mu(T)}{k_b T}} d\epsilon \quad (12)$$

With $\mu(T) \simeq n/g_{2D}$ (where g_{2D} is the 2D density of states). We estimate $\langle e \rangle \simeq 25\text{ meV}$. For these values, $T_{th}(\langle e \rangle) = 6 \times 10^{-16}$ and $T_{tun}(\langle e \rangle) = 10^{-26}$. From the rate equation, we can estimate the time-constant of the exponential decay, given by (as shown previously) $\tau = t / \langle v \rangle T(\langle e \rangle)$. We obtain the following estimates:

$$\tau_{th} \simeq 60\text{ s} \quad (13)$$

And

$$\tau_{tun} \sim 10^{11}\text{ s} \quad (14)$$

Thus, we see from this rudimentary model that interfacial charge transfer due to thermionic emission can lead to a conductance decay over the time scales observed in Figure 4(a), while tunneling only contributes minimally over these time scales.

While our model only predicts a simple exponential decay, it does not take into account the redistribution of electric field by gate-induced carriers, which would modify this picture.

At lower temperatures (50K), $\tau_{th} \sim 10^{78}\text{ s}$, indicating that thermionic emission charge transfer does not play a role at these temperatures.

References (1) Kress-Rogers, E.; Nicholas, R. J.; Portal, J. C.; Chevy, A. Cyclotron resonance studies on bulk and two-dimensional conduction electrons in InSe. *Solid State Communications* **1982**, *44*, 379–383.