Supporting Information

Decreasing Interface Defect Densities via Silicon Oxide Passivation at Temperatures Below 450°C

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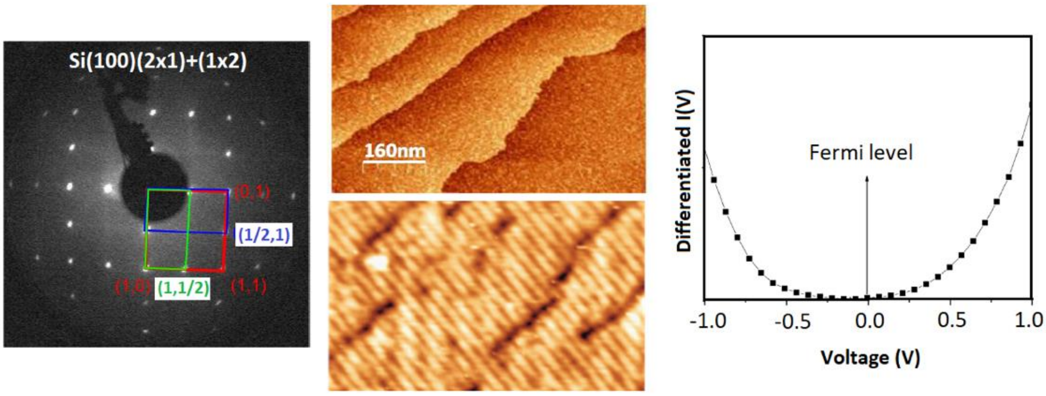

Figure S1. *Properties of a typical Si(100)(2x1)+(1x2) surface cleaned by the flash heating around 1200^{o}C, as characterized by LEED, STM, and STS. The clean surface is reconstructed, i.e. surface unit cell is different from that of the (100) bulk planes. The reconstruction-related unit cells in the LEED reciprocal space are shown by green and blue rectangles, while the red square marks the bulk (1x1) cell. Large-scale STM image shows smooth two-dimensional terrace-step structure. Zoomed-in image shows the dimer rows plus dimer-vacancy trenches, latter of which appear as meandering dark rows. STS curve shows that the band gap decreases to about 0.5 eV at the surface due to the surface reconstruction and related dangling-bond levels (bulk gap about 1.1 eV).*

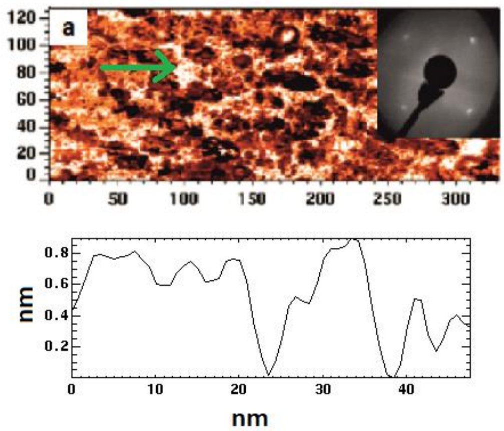

Figure S2. *Contour line profile along the green arrow in the STM image shows that the height of the islands can be at least 0.8 nm.*

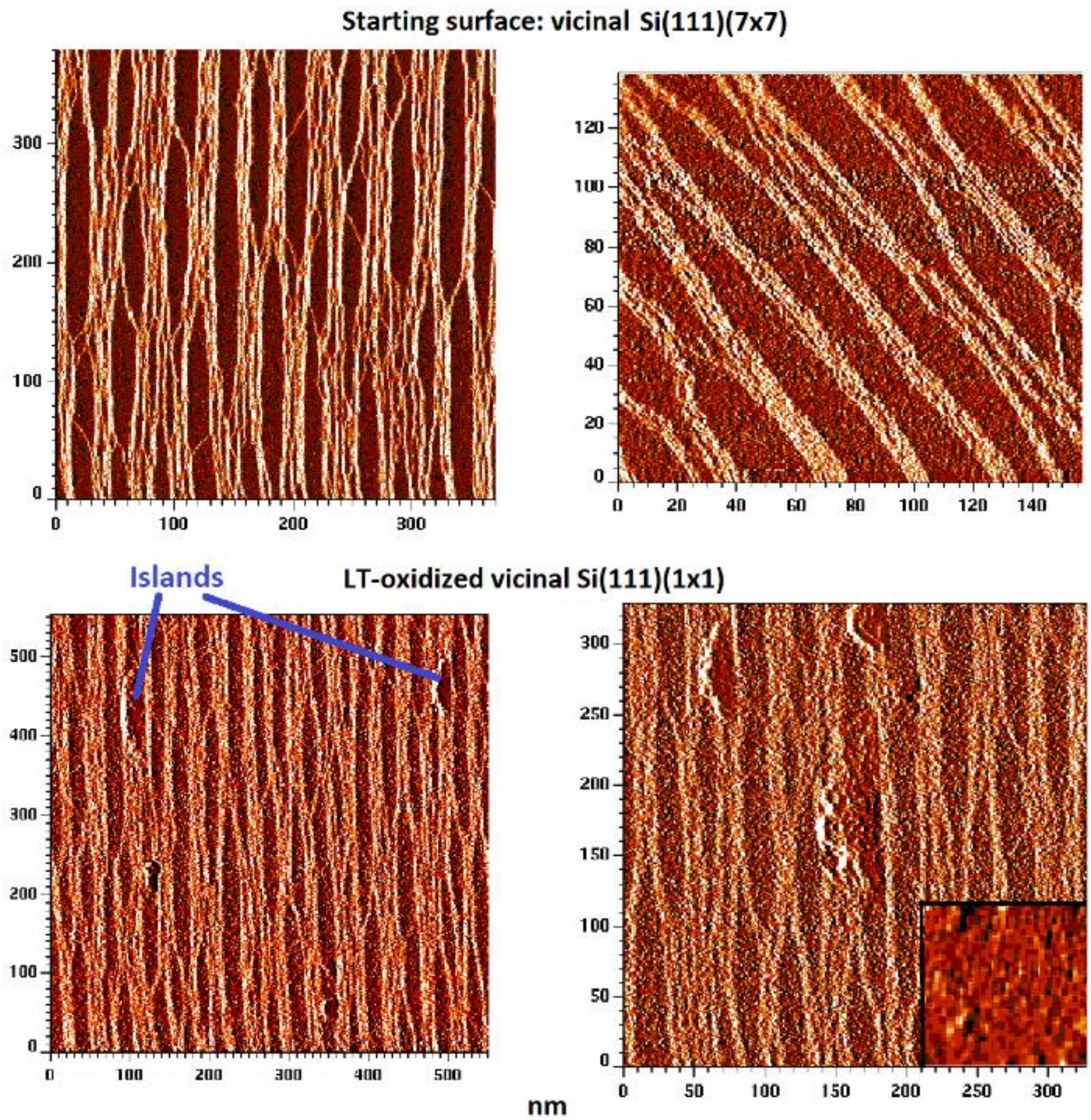

Figure S3. *STM characterization of vicinal (or offcut) Si(111) before and after LT oxidation, respectively, in the top and bottom images. The zoomed-in STM in the inset is taken from the top of a smooth, epitaxial type island seen on the larger scale image after the controlled oxidation. LEED showed the (7x7) pattern before the oxidation and (1x1) pattern after the oxidation.*

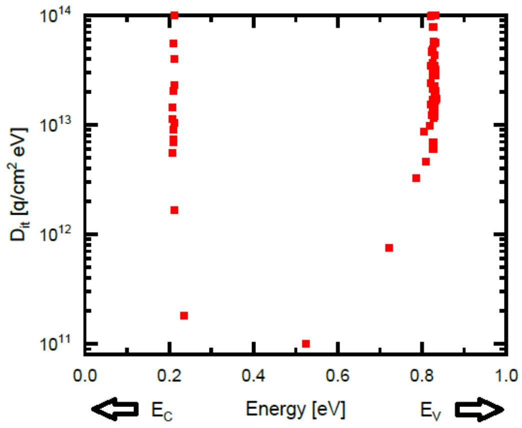

Figure S4. *Example for defect-density distribution around the band gap, as determined by COCOS measurement. The arrows indicate the directions for valence band (E_V) and conduction band (E_C).*

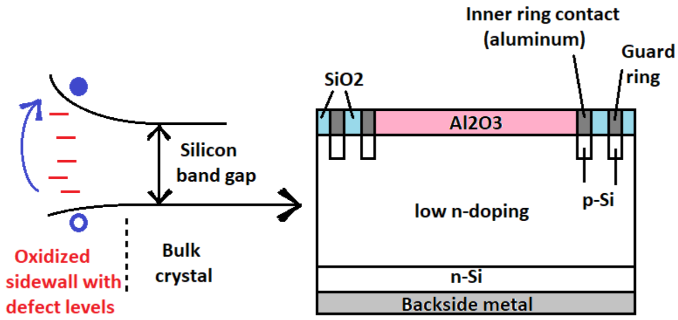

Figure S5. *Right: Schematic layer structure for the photodiodes (not in correct scale). Left: Possible explanation for that why the leakage current decrease was observed, when measured between the inner ring contact and backside contact. Blue circle represents hole created by the thermal excitation of an electron via the defect levels (red lines) in the band gap to the conduction band. Because the sidewalls contain oxidized Si, their band gap can increase as compared to the Si band gap. There is most likely an internal electric field also near the sidewalls, because of trapping of electrons in the defect levels. Thus, the band bending occurs near the sidewalls pushing the carriers toward the Si bulk, affecting the leakage measured between the inner ring and the backside.*

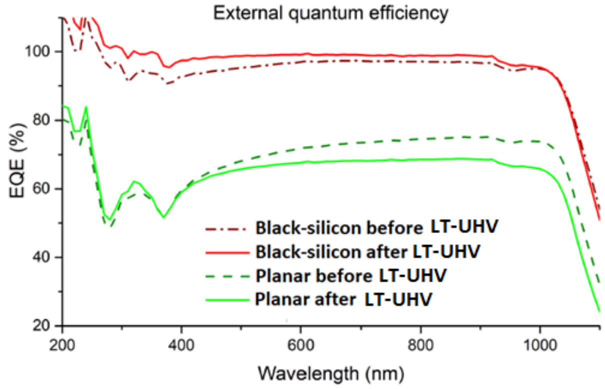

Figure. S6 *Effect of the LT-UHV post-treatment on photodiode external quantum efficiency (EQE). The LT-UHV post-treatment did not significantly change EQE of the photodiodes with a black-silicon or a planar surface structure.*

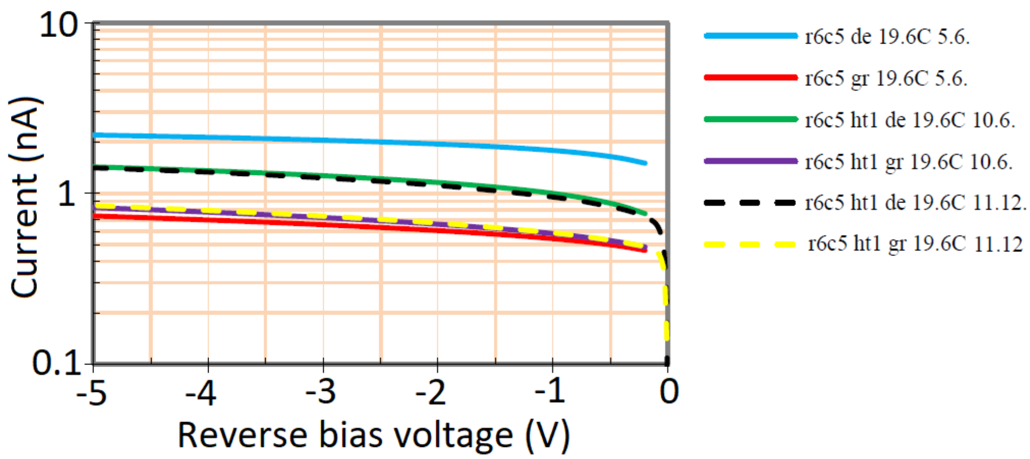

Figure S7. *The decrease in the leakage current is found to be durable. The leakage current measurements of the same component (r6c5) in dark as a function of time at the defined temperature of 19.6°C. The blue and red curves were measured on June 5, 2019, before the LT-UHV post-treatment. The green and violet were measured on June 10, after the treatment. Dotted black and yellow were measured on December 11. The leakage decreased between the inner contact ring and backside (curves labeled with "de") due to the treatment (blue vs. green), while the leakage between the outer ring and backside (curves labeled "gr") hardly changed. About half-year air exposure did not change the leakages (green vs. black dashed; and violet vs. yellow dashed).*

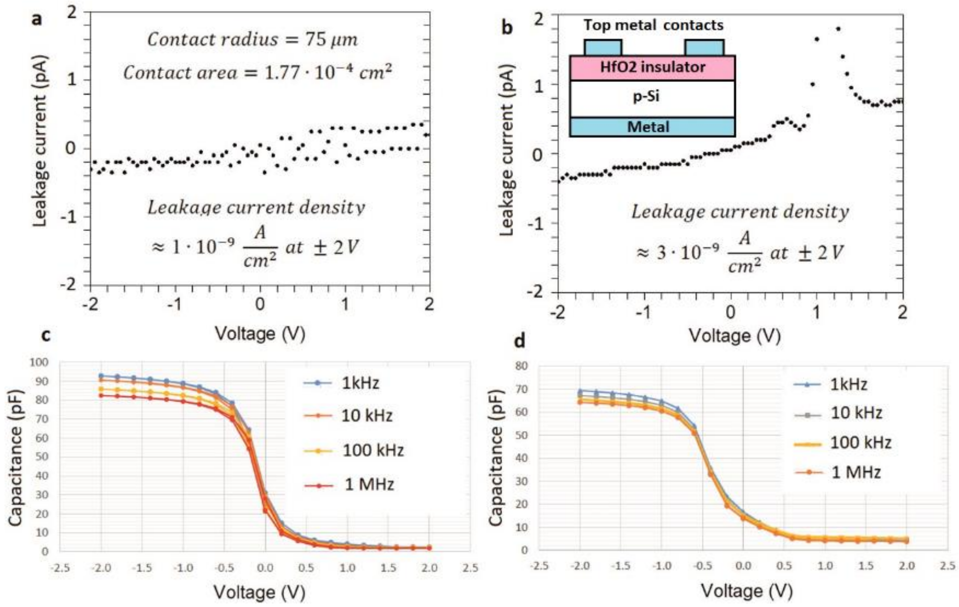

Figure S8. *Capacitor HfO_2(22nm)/p-Si(111) measurements for surface-science samples (6 mm x 12 mm pieces). Leakage current (through HfO_2 film) comparison between (a) LT-UHV pre-treated interface and (b) RCA-based chemical oxide interface; a peak around 1.2 V probably arises from trap levels, which is reasonable because these samples were not passivated by hydrogen in the forming gas. Capacitance-voltage curve comparison between (c) LT-UHV pre-treated interface and (d) RCA-based chemical oxide interface. Decreased leakage current of the LT-UHV treated capacitor, and its sharper depletion-region capacitance step (i.e. less stretched out capacitance step) are consistent with the results that D_{it} decreases[1] by proper vacuum treatment. The obtained leakage current near $1\cdot10^{-9}$ A/cm^2 is also promising, when compared to the state-of-the-art capacitor values for similar oxide-film thicknesses.[2] The capacitors were prepared on small scale Si-wafer pieces using the surface-science UHV system.*

REFERENCES

(1) Wang, T.; Chang, T.-E.; Huang, C.; Interface Trap Induced Thermionic and Field Emission Current in Off-State MOSFET's. *IEEE Int. Electr. Dev. Meet. IEDM* **1994**, 161.

(2) Dietz, D.; Celik, Y.; Goehlich, A.; Vogt, H.; Kappert, H.; High-Temperature Trench Capacitors Using Thin-Film ALD Dielectrics, *Internat. Confer. Exhib. High Temper. Electr. Network* (HiTEN), **2015**, 000130.