**Supporting Information for:**

**Low Voltage Operating 2D MoS2 Ferroelectric Memory Transistor with Hf1-xZrxO2 Gate Structure**

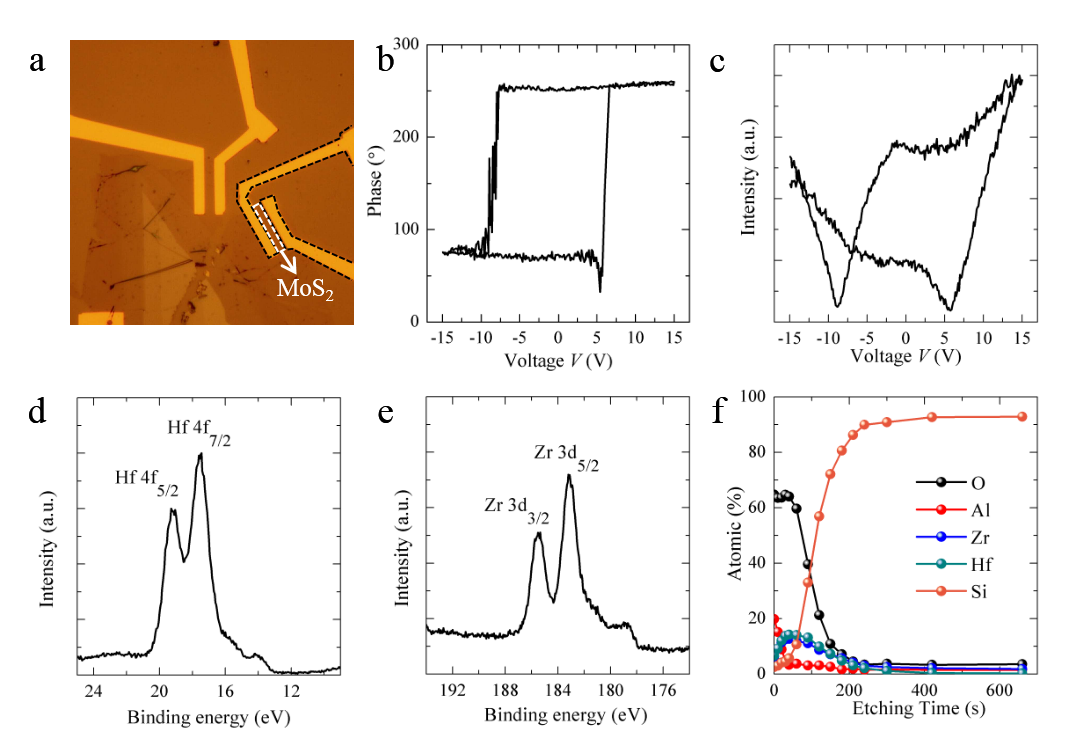
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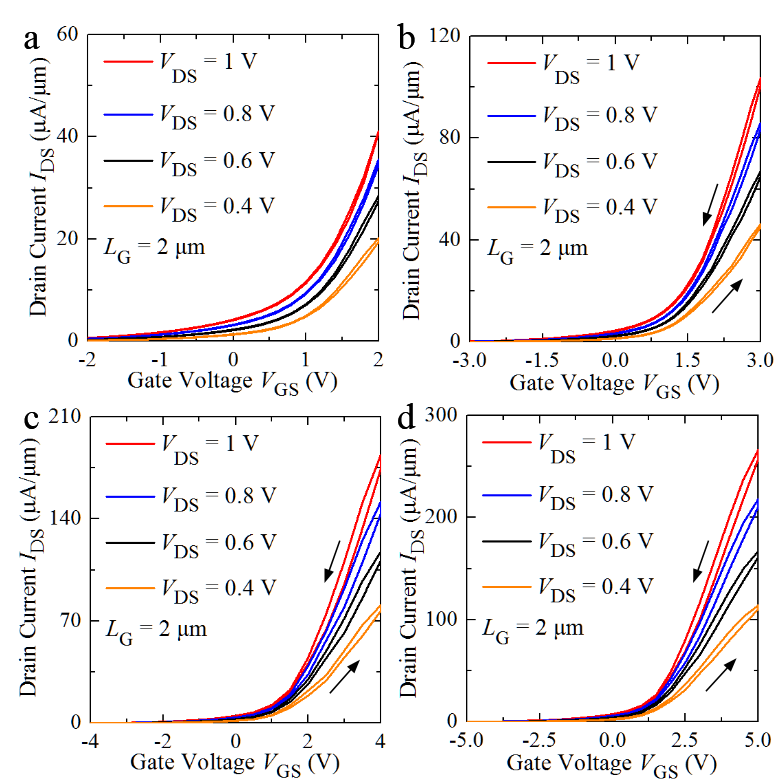
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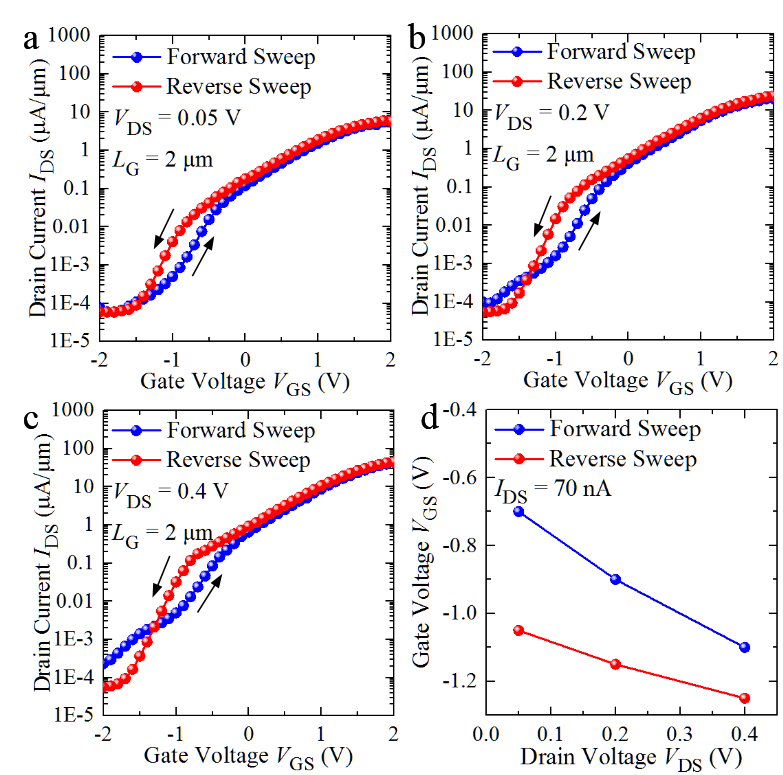
**Fig. S1** **a** Optical image of the MoS2/HZO FeFET. **b** *PRphase* and **c** *PRampl* of the HZO capacitor. XPS analysis of the 2 nm Al2O3/6 nm HZO/p+ Si shows pristine **d** Hf and **e** Zr peaks. **f** XPS depth profile of the Al2O3/HZO/p+ Si tri-layer structure.

A top-view optic image of the HZO/MoS2 FeFET is shown in Fig. S1a. As shown in Fig. S1b and c, *PRphase* and *PRampl* of the HZO capacitor suggest ferroelectric behavior after 450 ℃ rapid thermal annealing (RTA) measured at 1kHz. As shown in Fig. S1d and e, the elemental and bond composition of HZO were examined by the X-ray photoelectron (XPS) measurements. Peaks are found to be 19.05 eV, 17.6 eV, 185.5 eV, and 183.2 eV, which correspond to the Hf 4f 5/2, Hf 4f 7/2, Zr 3d 3/2 and Zr 3d 5/2, respectively [27]. The atomic concentration along the depth profile in Fig. S1f further confirms the distribution of the Al2O3/HZO/p+ Si tri-layer structure. All the above confirm that the HZO film grown via our ALD system is highly crystalline.



**Fig. S2** Transfer curves of the HZO/MoS2 FeFET at increasing gate voltage (*V*GS) ranges with the linear y-axis.

For a start, the transfercurves of the HZO/MoS2 FeFET under different back gate voltage sweep ranges (*V*GS,range) and different drain voltages (*V*DS) have been characterized in Fig. S2. It is demonstrated that, the counterclockwise hysteresis windows have been obtained at various gate voltage range (*V*GS,range) from (-5, 5V) to (-2, 2V). Simply, the mechanism underlying the hysteretic behaviors shown in the transfer curves during the bi-direction sweeping of *V*GS is threshold voltage shift, which can be modified by the effects of trapping/de-trapping [29] and polarization switching [30]. If the applied voltage is not high enough to switch the polarization in HZO film, charge trapping/de-trapping mechanism dominates and will cause clockwise hysteresis. The energy band at the interface between the MoS2 channel and ferroelectric back gate tends to bend downward after the positive back gate voltage. The more traps located below the Fermi-level; the more electrons are captured close to the interface. This will increase the threshold voltage after the positive gate pulse. The energy band at the interface between the MoS2 channel and ferroelectric back gate tends to bend upward after the negative back gate voltage. The more traps locate above the Fermi-level; the more electrons are released close to the interface. This will decrease the threshold voltage after the negative gate pulse [29]. If the applied voltage exceeds the coercive voltage in the HZO film, ferroelectric polarization mechanism dominates and will cause anti-clockwise hysteresis window [31-34]. Thus, it is easily concluded that the electrical performance of the device shown in Fig. S2 is dominated by ferroelectric switching. When the back-gate sweeps are in small ranges of 2V in Fig. S2a, we observed the nearly hysteresis-free switching. The hysteresis loops in Fig. S2b are counterclockwise for the back-gate sweep range of 6 V (from -3 V to 3 V). The minimum voltage under the drain is *V*GS – *V*DS = 2 V at *V*DS = 1 V, which should be larger than the coercive voltage *V*c to switch the ferroelectric at the drain side. The estimated coercive voltage is consistent with *V*c of 1.9 V when the maximum sweeping voltage is 3 V in Fig. 2a. When the applied voltage in HZO film exceeds +*V*c, the ferroelectric polarization points into the MoS2 channel. Therefore, the electron charges in the MoS2 channel accumulate and the threshold voltage decreases. When the applied voltage in HZO film exceeds –*V*c, the ferroelectric polarization points away from the MoS2 channel. Therefore, the electron charges in the MoS2 channel deplete and the threshold voltage increases. Nonetheless, we observed that the wider back-gate voltage range leads to larger counterclockwise hysteresis loops in Fig. S2c and d. Due to the increment of *V*c in Fig. 2a with increasing applied voltage, the ferroelectric polarization switching in the HZO film can be enhanced with a larger shift in threshold voltage.



**Fig. S3** Transfer curves of the HZO/MoS2 FeFET on logarithmic scales with **a** *V*DS = 0.05 V, **b** *V*DS = 0.2 V, **c** *V*DS = 0.4 V. **d** Extracted back gate voltage *V*GS when drain current (*I*DS) equals to 70 nA with different *V*DS.

Notably, besides the impact of *V*GS,range, it is found that *V*DS can definitely adjust the memory window as well, which requires a further investigation. The *I*DS-*V*GS curves on logarithmic scales under different *V*DS are characterized in Fig. S3. It is exhibited that, at a fixed *V*GS,range = (-2, 2 V), the values of *V*GS extracted at *I*DS = 70 nA for the bi-directional sweeping of *V*GS all shift towards the negative direction and the variation in forward sweeping of *V*GS is much more obvious over that of reverse sweeping, indicating the significant phenomena of negative drain induced barrier lowering (DIBL) [36-40]. Generally, DIBL is a conventional short channel effect. With a short enough channel length, the increased *V*DS can easily pull down the barrier between source/drain and enable a negative shift of threshold voltage, which is the so called effect of DIBL. However, for a ferroelectric FeFET, an increased *V*DS is capable of producing a reduction of channel surface potential via the coupling between gate and drain induced by the parasitic capacitance between gate and drain (CGD), which means a positive shift of threshold voltage and can be called as negative DIBL.