

Supporting Information

“Stickier”-Surface Sb₂Te₃ Templates Enable Fast Memory Switching of Phase Change Material GeSb₂Te₄ with Growth-Dominated Crystallization

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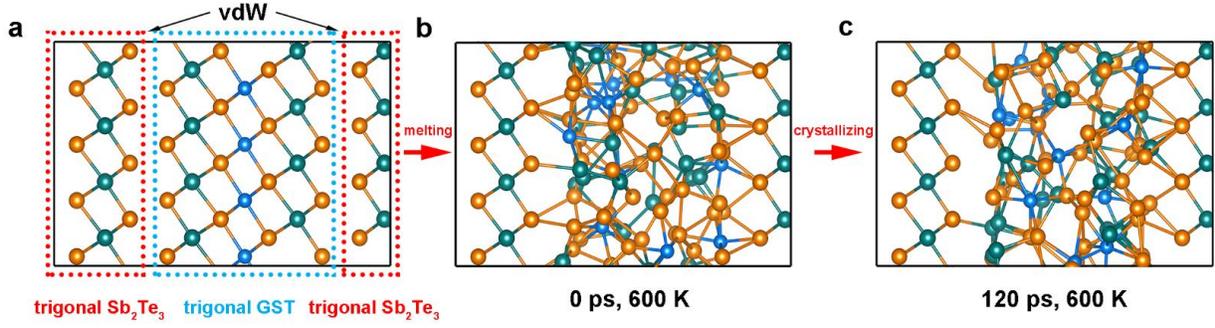


Figure S1. Epitaxial growth simulations in the trigonal-phase GST/Sb₂Te₃ heterostructure. a) Crystalline trigonal GST/Sb₂Te₃ heterostructure with van der Waals (vdW) gaps at the interfaces. b) Initial state of GST/Sb₂Te₃ heterostructure for the epitaxial growth simulation (trigonal phase), which is acquired by melting the sandwiched GST part in (a) at 3000 K. c) Final state of GST/Sb₂Te₃ heterostructure (trigonal phase) after 120-ps epitaxial-growth simulation at 600 K.

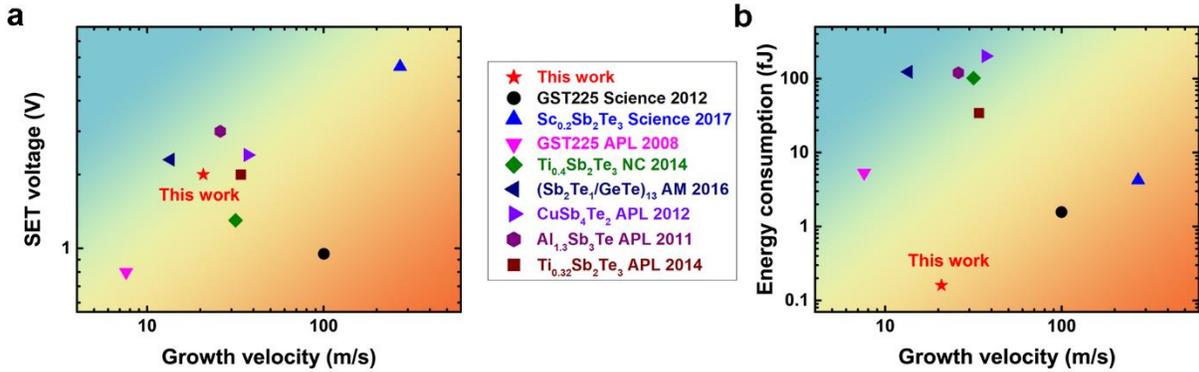


Figure S2. Some comparisons of energy efficiency between this work and other works from references (S1-S5, 12, 13, 20). Growth velocity, defined as dividing the diameter of phase change materials in the hole by SET time, is adopted to exclude the size effect and characterize the true speed of crystallization. a) SET voltage and b) energy consumption versus growth velocity. The SET energy consumption is roughly calculated through $E_{SET} = \frac{U^2}{R_{amorphous}} \cdot t$, where E_{SET} , U , $R_{amorphous}$, t is the energy consumption of SET operation, pulse voltage, resistance of amorphous state, and SET time, respectively. A 20.8 m/s fast crystallization speed can be achieved by 0.16 fJ

energy in $[(\text{GST})_1/(\text{Sb}_2\text{Te}_3)_3]_{13}$ -based PCM devices. This 0.16 fJ SET energy consumption is the lowest one among all other works.

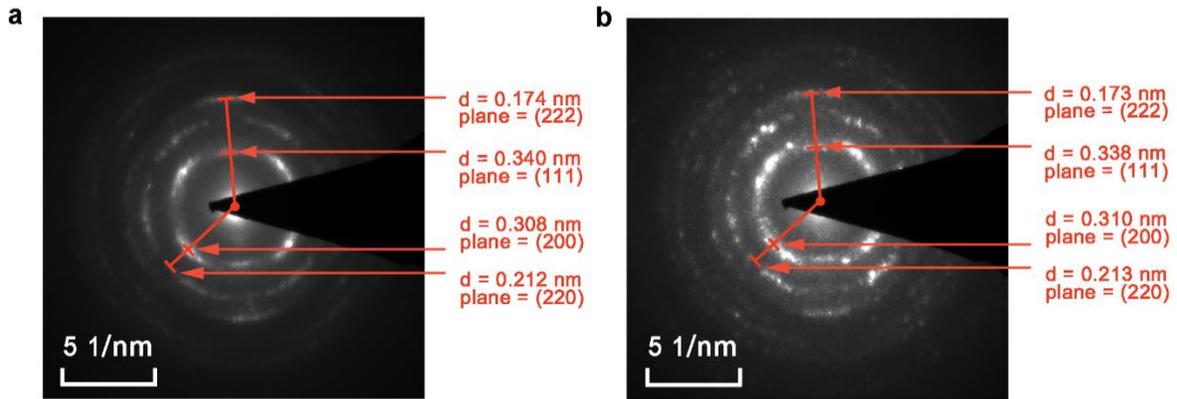


Figure S3. Selected area electron diffraction (SAED) results of GST/Sb₂Te₃ heterostructure in the memory cells a) before and b) after SET operations, which are well in coincidence with the fast Fourier transform (FFT) results. The interplanar spacing values d and their corresponding lattice planes are shown beside.

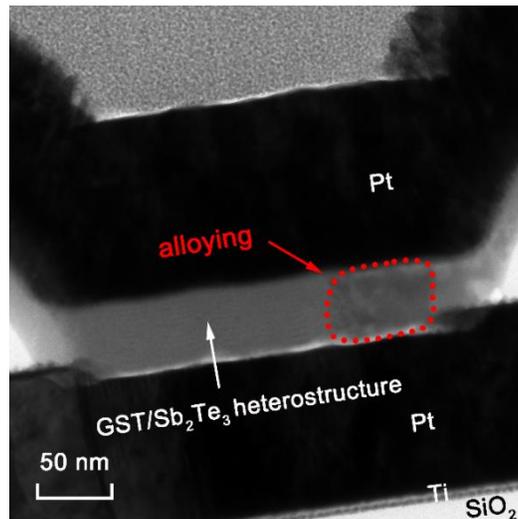


Figure S4. Cross-sectional TEM image of “T”-shaped $[(\text{GST})_1/(\text{Sb}_2\text{Te}_3)_3]_{13}$ PCM after the direct current sweep. Besides the multi-layered GST/Sb₂Te₃ heterostructure, an alloyed area induced by the long-duration direct current sweep is marked by a dotted red curve.

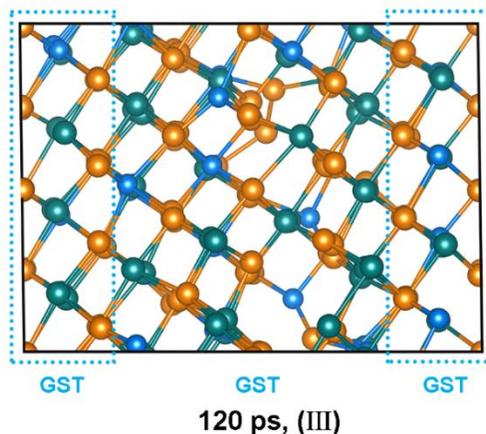


Figure S5. Final structure of intrinsic GST templated model after 120 ps at 600 K. Due to the exemption of lattice mismatch, fewer disorders exist in the final crystalline structure of simulated GST (middle).

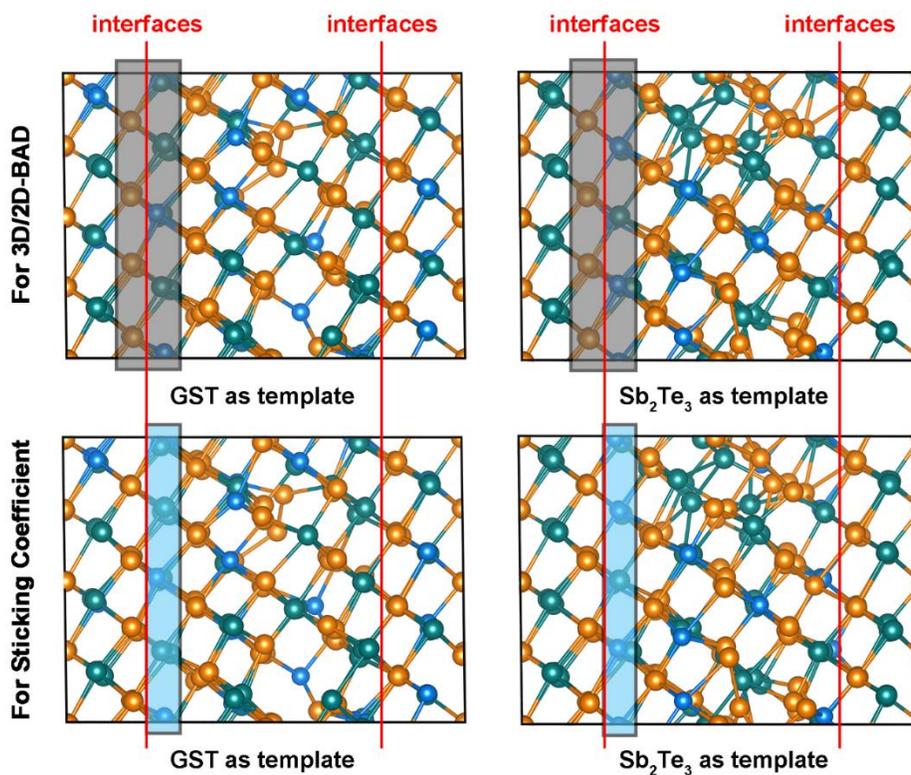


Figure S6. The gray (blue) regions set for the atom selections of 3D/2D-BAD (sticking coefficient) calculations in both intrinsic GST templated (left panel) and Sb_2Te_3 templated (right panel) models.

Each left or right boundary of gray (blue) regions is set in the middle of its two adjacent atomic layers. The interfaces between simulated GST and templates are indicated by red lines.

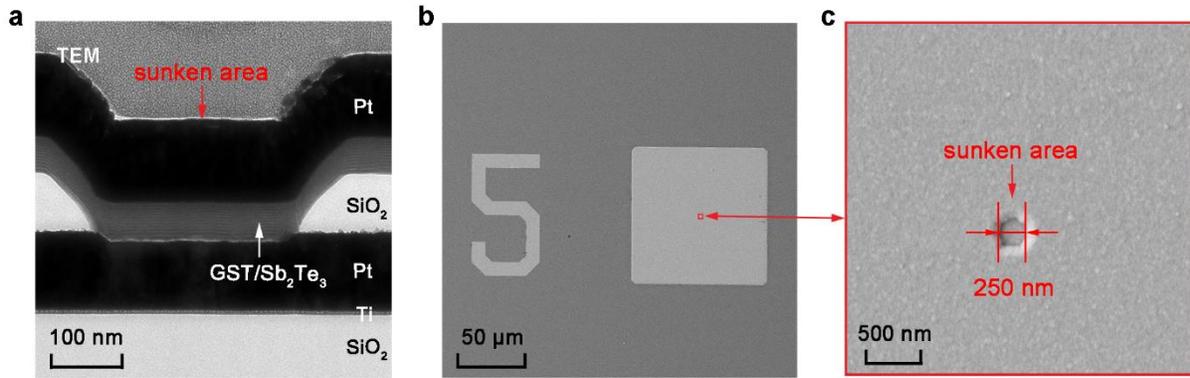


Figure S7. The sunken area of top electrode from different perspectives. a) Side view of the sunken area of top electrode (TEM image). b) Top view of the sunken area of top electrode, captured by scanning electron microscopy (SEM). c) A zoom image of the area marked by a red square in (b).

Note S1. Figure S1 shows the epitaxial growth simulations in the trigonal-phase GST/Sb₂Te₃ heterostructure. The simulated model initially has a sandwiched amorphous GST part (see Figure S1b) which retains even after 120-ps simulation (see Figure S1c). As comparison, in the latter epitaxial-growth simulations of fcc-phase GST/Sb₂Te₃ heterostructure (Figure 5b), the amorphous GST part gets fully crystallized after 80 ps. This is because the weak vdW forces on the surfaces of trigonal Sb₂Te₃ templates are not so effective to adsorb moving atoms. In a word, the epitaxial growth happens harder when the templates have the trigonal-phase surfaces terminated by vdW gaps. Therefore, the epitaxial growth of annealed trigonal-phase films in Figure 1 can be used to examine that of fcc-phase GST/Sb₂Te₃ heterostructures in Figure 3, 5, and 6.

Note S2. Two effective methods were used to locate the positions of holes during the fabrications of TEM specimens: (1) The use of overlay alignment in lithography made the holes be in the center of square-shaped top Pt electrodes, so that the approximate locations of holes were known even they were covered by top electrodes; (2) And most importantly, the thickness of SiO₂ insulator layers (100 nm) was designed to be much thicker than that of phase change material layers (50 nm). Therefore, the 50-nm-thick phase change materials couldn't fill up the 100-nm-deep through-holes in the insulator layers totally, which caused some parts of top electrodes fell into the through-holes, as shown in Figure S7a. Finally, there would be some round sunken areas on the surfaces of top electrodes, which were easy to discover (see Figure S7c).

References

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