A Versatile Power Electronic Interface for a Fuel Cell and Ultra-Capacitor Energy Buffer for a DC Micro-grid System

Thesis submitted for the degree of

Doctor of Philosophy

at the University of Leicester

by

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January 2018

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Abstract

Micro-grid systems are small-scale power supply networks that are designed to provide electricity to a local community from local generators. Micro-grids operate with a common AC or DC bus, and power converters are key components for interfacing the generators and storage devices (and sometimes the loads) to the common bus. The aim of this research study is to investigate and develop high-efficiency power electronic converters for the interconnection of fuel cells and ultra-capacitors to a DC micro-grid for stationary power distribution systems.

The converter for the fuel cell and its dynamic control have been designed, simulated, and further improved by introducing a new modified active clamp circuit that enhances performance and increases the efficiency of the converter. This new modification has been designed and verified by PSpice/Simulink approach and implemented using dSPACE.

To control the power flow status of the ultra-capacitor, a bidirectional DC–DC converter is required. A number of different alternative DC–DC converter topologies were compared. It was concluded that, the bidirectional voltage–fed topology is better suited for dealing with the fast dynamic response of the ultra-capacitor. However, this topology exhibits a higher circulating power flow and higher conduction losses. Based on this limitation, a modulation scheme that minimises the circulating power flow in the converter was introduced and this was verified by simulations.

The hardware for the ultra-capacitor (bi-directional) converter has also been designed and implemented. The test results demonstrate the ability of the converter for fast and bidirectional power flow. The development of simulation models and the control system are experimentally implemented in dSPACE.

I dedicate this thesis to my parents, wife and sons

Acknowledgements

First, I would like to thank both Dr. Hans Bleijs and Dr. Paul Lefley, my supervisors here at University of Leicester for their guidance and support throughout my years as a PhD student. Their guidance, support, comments and suggestions throughout the writing of this thesis are invaluable and are highly appreciated. I am also grateful to Mr. Mohan Kansara for his support and encouragement.

Special thanks are given to Mr Luigi Alessandro for his technical help and support.

Also, I would like to thank the Iraqi Ministry of Higher Education for granting me a PhD scholarship. I am grateful to all those who assisted me in my PhD study at the Department of Engineering.

I would like to thank University of Basrah/ Engineering Department and my colleagues for their support and wishes.

Most importantly, I would like to thank my family (mother, father, wife, sons, and brothers) and friends for their support throughout my PhD project.

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Introduction to Micro-grids

1.1 Micro-Grid Systems

In recent years, significant concerns have been emerging regarding the inherent problems of conventional power systems such as the continuing depletion of fossil fuel resources, and the increasing rates of pollution. Researchers have been considering resorting to alternative renewable energy sources such as wind power, solar cells, and fuel cells which lead to a new trend of generating power locally with the help of these non-conventional sources. This type of power generation is labelled as distributed generation system (DG) and the energy sources are termed as distributed energy resources (DERs) [1, 2, and 3]. Together these systems are combined in the form of Micro-grids.

A Micro-grid is a local energy network, offering integration of distributed energy resources (DER) with local loads, which can operate in parallel with the grid or in an intentional island mode to provide a customized level of high reliability and resilience to grid disturbances. Micro-grid loads are commonly categorized into two types: fixed and flexible. This advanced and integrated distribution system addresses the need for application in locations with electric supply and/or delivery constraints, in remote sites, and for protection of critical loads and economically sensitive development. The main benefits of micro-grids are high energy efficiency, high quality and reliability of the delivered electric power, more flexible power network operation, in addition to environmental and economic benefits [4, 5]. The main components of a micro-grid are:

(i) Distributed generation sources such as photovoltaic panels, small wind turbines, fuel cells, diesel and gas micro-turbines etc.,

(ii) Distributed energy storage devices such as batteries, super-capacitors etc.,

(iii) Critical and non-critical loads.

Fig.1.1 shows typical micro-grid parts.

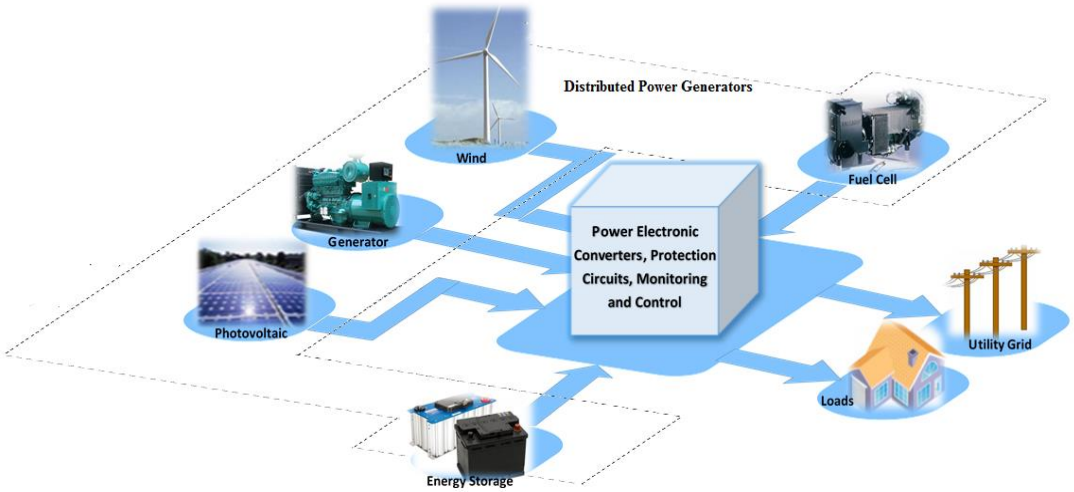


Fig.1.1 Parts of a typical micro-grid

1.2 Configuration of a Micro-Grid System

A Micro-grid system can be classified into two categories according to the bus connection type: AC or DC. In the AC micro-grid, all the energy sources and loads are connected through an applicable power electronic interface within the AC grid. On the other hand, within a DC micro-grid different alternative energy sources are connected to a main DC bus-bar through a suitable power electronic devices (PEDs). It can also be connected to an AC grid or AC loads through a DC–AC converter.

1.2.1 A.C Micro-Grid Structure

In an AC micro-grid, all DERs and loads are connected to a common AC bus. DC generating units such as photovoltaic generators and fuel cells as well as energy storage will be connected to the AC bus through DC-AC inverters. Furthermore, a DC–DC converter with a boost capability is occasionally required as a front-end to step up their low input voltage. In spite of several advantages provided by the micro-grid, there are some technical considerations:

1) Synchronisation is essential for all AC generators and output of the power converters of the DC sources and energy storage devices.

2) Power factor correction (PFC) and advanced topologies with control strategies for harmonic distortion reduction are needed to improve the power quality of the AC bus due to the non-linear characteristics of the power converter circuits.

3) Renewable energy sources suffer from rapid variations in their outputs which can lead to excessive voltage and frequency variations on the AC bus of an AC micro-grid. Therefore, the limits of their maximum permeation is normally restricted in the AC micro-grid bus.

Fig. 1.2 shows a typical block diagram of an AC micro-grid system.

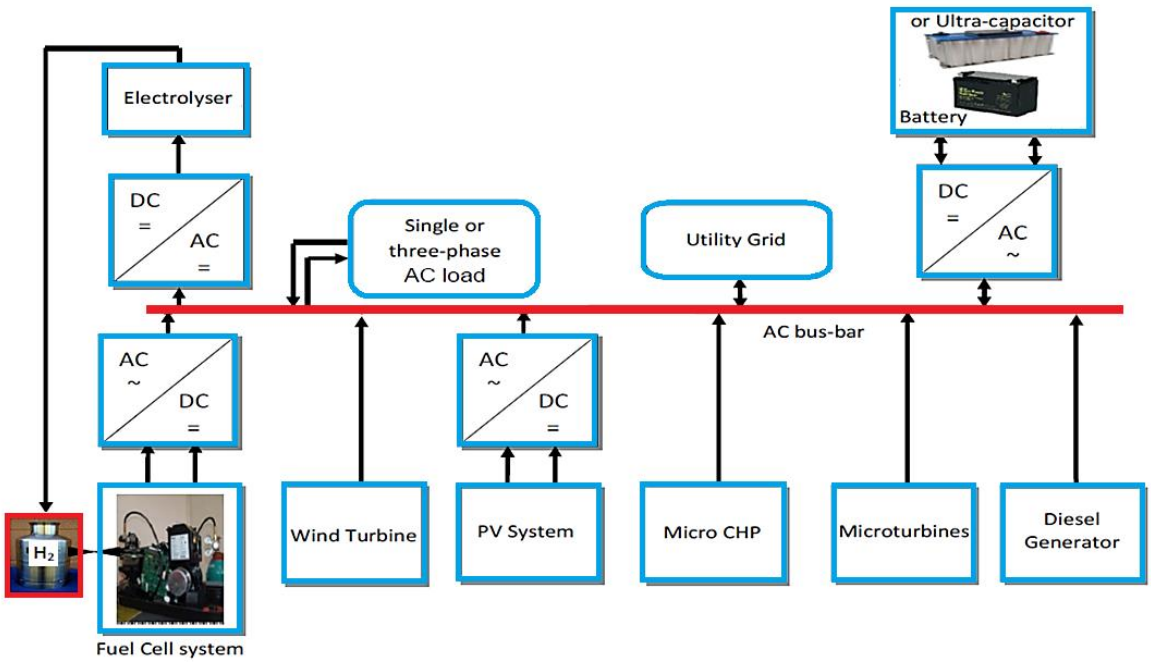


Fig. 1.2 AC micro-grid system configuration

Recently, DC micro-grids have shown encouraging features such as improving the grid efficiency and the power quality in addition to increasing the integration of the renewable energy sources to the micro-grid bus and the elimination of the DC–AC power conversion stage required in an AC micro-grid for the renewable sources and loads. Thus, some negative effects associated with an AC micro-grid can be avoided.

1.2.2 D.C Micro-Grid Structure

The DC micro-grid system consists of two types of power generators: dispatchable power generators such as a fuel cell, back-up diesel generator or micro (gas) turbine, and non-dispatchable ones, such as solar photovoltaic and wind turbines. In addition, it contains energy storage in the form of ultra-capacitors or batteries. Fig.1.3 shows the basic configuration of a DC micro-grid. All the above mentioned generators and storage units are connected to the DC bus-bar. From Fig.1.3, it can be seen that different configurations of power electronic converters are used to interface these generation resources to a common DC bus-bar. These converters are working to manage the power flow between generators, storage sources and the load, and to adjust the DC bus voltage regardless of the voltage variations at their inputs.

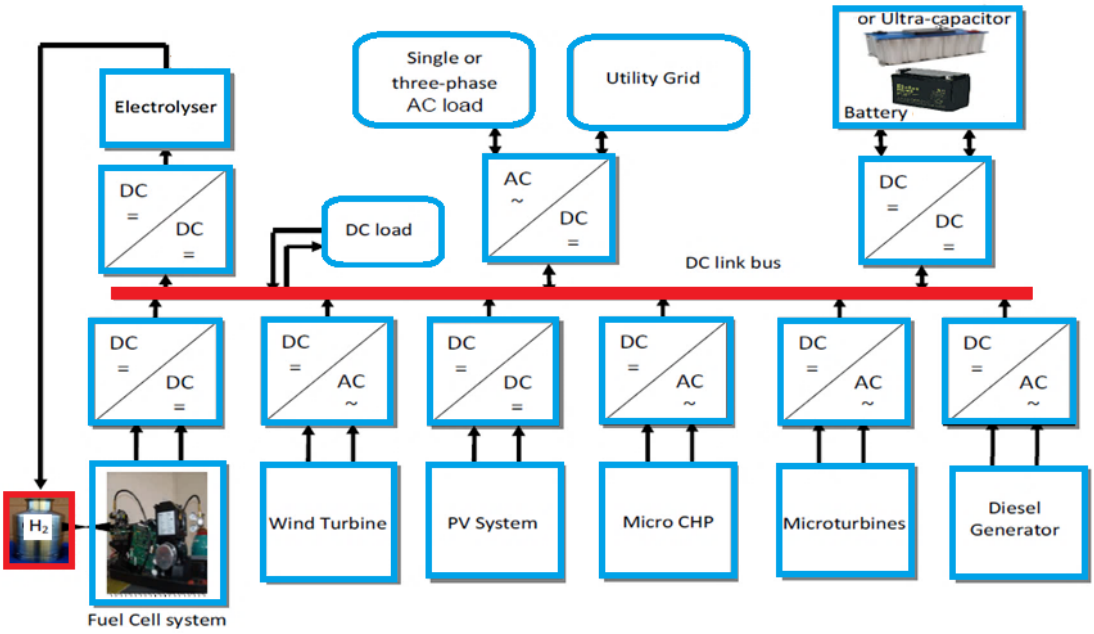


Fig. 1.3 Basic configuration of the DC micro-grid system

DC micro-grids could offer several advantages compared with AC micro-grids such as:

- Higher efficiency and reduced losses due to the reduction of multiple converters used for dc loads.
- Using simplified interfaces, it allows for different dc distrusted energy resources to be merged with the mutual bus.

- More efficient supply of dc loads, such as electric vehicles and LED lights.
- It allows the rotary generating units to run with their optimum performance without the need for these generators to be synchronized.
- Allowing bus connections to be operated without the need for synchronizing the buses [6, 7].

1.3 Micro-grid Distributed Energy Sources

In order to construct a micro-grid system there should be generating sources that cover the requirements of the load in the micro-grid. There are two kinds of distributed sources in the micro-grid system: first, distributed generation sources such as photovoltaic panels, small wind turbine, and fuel cells; and secondly, distributed storage devices such as batteries, super-capacitors. Below is an overview of the most important energy sources that are used within a micro-grid structure [6].

1.3.1 Photovoltaic Cells

Photovoltaic (PV) cells or system generates voltage when they are directly exposed to the sunlight using the photovoltaic effect [8, 9]. The photovoltaic effect was discovered by Alexander-Edmond Becquerel in 1839. The first build of a photovoltaic device was in 1939 [10]. The cost of PV has significantly dropped since the first solar cell was produced. A number of modules, formed by the interconnection of photovoltaic cells, constitute a photovoltaic generator. These cells are connected together and arranged according to different arrays to provide the required voltage and current. The resulting power of PV's systems spans from a few watts for transportable applications like mini light bulbs up to megawatt-producing powerhouses [11]. A DC–AC inverter is essential to convert the DC power into AC power at the specified frequency and voltage level and then interfaced with the AC utility grid and loads [12]. This is because PVs are DC generating devices. For stand-alone or grid connection, PV systems can be merged with an energy buffer to store energy when there are low levels or no sun light present. While

PV cells can be effectively used as a source in a micro-grid, however they are currently considered as unreliable due to the high costs of installation and low energy efficiency [13].

1.3.2 Wind Energy Conversion System

A wind energy conversion system (WECS) transforms wind energy into electricity [1, 4]. Wind may be regarded as a renewable energy source, which has been extensively developed during the last few decades because of its ability to produce an abundance of green power [14]. Therefore, wind has been considerably preferable by researchers and manufacturers of power plants for a variety of reasons like low cost, rapid technological development, and the achievable power levels rating produced. The core component of any WECS is the turbine which is either directly attached to the generator (in case of multi–pole generator) or through a step–up gearbox. The other components of the WECS are the tower, the rotor and the casing into which all components are assembled [15, 16]. However, wind generation are not reliable in the technical sense because they are characterized by the unstable nature which is conditioned by the presence of wind, the lack of which may cause potential deviations in the output voltage and frequency; a potential problem that may limit the possibility of integrating multiple generators into a micro-grid [17]. To surmount this problem the wind turbine generators can be incorporated with other power resources like a back-up diesel generator, and energy storage or fuel cells. Energy storage devices such as batteries or ultra-capacitors can be used as temporary power substitutes to reduce the problem of intermittency wind designated generator [18]. Therefore, the integration of fuel cells with wind generator systems appear to be an applicable solution that addresses the problem of intermittency which results in providing a sustainable source of energy.

1.3.3 Combined Heat and Power Systems

Combined heat and power systems (CHP) or Cogeneration systems are considered as one of the promising elements for micro-grid applications. Since it produces two kinds of energy; that is to say, electric power and heat energy [19], CHPs play an effective role to ensure the enhancement of energy efficiency in micro-grid applications [20]. During the production of electricity, CHP systems maintain the waste heat and convert it into thermal energy [21, 22]. Moreover, micro-CHP systems can be used in small scale terminals, such as residential units or small commercial buildings [23, 24]. In addition to that, while most large industrial CHP units generate electricity as the primary product with heat as a secondary output, others are used to generate heat as the primary product with electricity as a by-product [1, 25]. Consequently, the power generation which is based on micro-CHP systems is largely conditioned by the heat demanded by users. Most micro-CHP systems operate on gas and this fact can be attributed to its availability, the ease with which it is pumped through pipelines, and most importantly it is a clean type of fuel compared to other fossil fuels. The CHP system can be connected to the DC micro-grid through an AC–DC converter (rectifier) as Fig. 1.3 illustrates.

1.3.4 Energy Storage

A micro-grid presupposes that an energy storage unit is an essential requirement so as to, first, allow instantaneous power balancing of distributed generation resources and loads when the micro-grid is disconnected from the utility grid (islanding or autonomous) and, secondly, to ensure an uninterrupted supply to priority loads. Furthermore, in the micro-grid system the energy storage devices function as a store where surplus energy is kept. There are three types of energy storage devices that could be contained within micro-grids: storage batteries, flywheels, and ultra-capacitors. Batteries and ultra-capacitors generate DC voltage, a bidirectional DC–AC converter, therefore, is needed to interface

between the storage devices and the AC-MICRO GRID (see Fig.1.2) while a bidirectional DC–DC converter is used to mediate the DC bus of a DC micro-grid (see Fig.1.3). On the other hand, flywheel generators can directly produce AC and thus are capable of directly feeding into the AC bus of the AC micro-grid [1, 4]. However, a bidirectional AC–DC converter is a prerequisite interface between the flywheel generator and a DC micro-grid bus. However, flywheels are notorious for having a low energy density, and yet, it takes them long time to discharge the energy stored in them, whereas ultra-capacitors store power at high power density but they discharge it faster than flywheels [1].

1.3.5 Fuel Cells

Due to unexpected weather changes associated with the wind and PV power generation, the fuel cell (FC) is considered one of the solutions for the uncertainty in environmental changes. FCs use hydrogen as a main energy source which is generated from a variety of fuels like hydrocarbons and water as well as other sources [26, 27].

Fuel cells are clean and efficient electricity generators that have much promise for the near future. They can be alternative energy generators for electrically powered devices, such as transportation, communications, computing and residential systems. Fuel cells produce low voltages. Thus, it is necessary to design a step-up converter to interface the FC to various loads [28, 29, and 30].

1.3.6 Energy Storage devices

There are three main energy devices that are mostly used within the micro-grid system: batteries, flywheels, and super-capacitor or ultra-capacitor (UC). The storage devices are considered as the most vital requirement for a micro-grid. That is due to the important features offered by these devices to the micro-grid, such as immediate power flow to the

loads connected to the grid, and to ensure a continuous supply to priority loads whenever they need it. Moreover, the energy storage devices help to store surplus energy. An overview for the energy storage devices are listed below. However, the ultra-capacitor will be explained in more details as it is considered in this research study.

1.3.6.1 Batteries

Electrochemical storage, more commonly referred to as “batteries”, are electrochemical devices that convert electricity into potential chemical energy during charging, and convert the latter into electric energy during discharging. A “battery” is composed of several cells stacked together. A cell is an independent and complete unit that possesses all the electrochemical properties. Basically, a battery cell consists of three primary elements: two electrodes (positive and negative) immersed into an electrolyte [31, 32, and 33].

1.3.6.2 Flywheel

A flywheel is basically a rechargeable kinetic energy store. It is used to absorb electrical energy from a source, store it as kinetic energy of rotation [34], and then deliver it to a load at the appropriate time, in the form that meets the loads needs. Moreover, it is a mechanical device with a significant moment of inertia used as a storage device for rotational energy [35, 36, and 37]. Since the voltage produced by the flywheel generators is usually on AC voltage, thus an AC-DC interface is required when they are used with a DC micro-grid [18].

1.3.6.3 Ultra-capacitor

Electric double-layer capacitors, also known as super-capacitors or ultra-capacitors (UC), are very high-capacity electrolytic devices that store energy in the form of electrostatic charge [38] Super-capacitors can have very high discharge rates and could handle fast

load changes in a Micro-Grid. They store power at high power density but are limited in the amount of energy stored, whereas others like batteries and flywheels which are capable of discharge energy over a longer period of time [39, 40, 41, and 42]. If uninterrupted energy is required for a long duration, then batteries is a preferred choice. Otherwise, ultra-capacitors are used to compensate fast dynamic requirements. Fig. 1.4 shows discharge curves of an electrochemical capacitor and a battery.

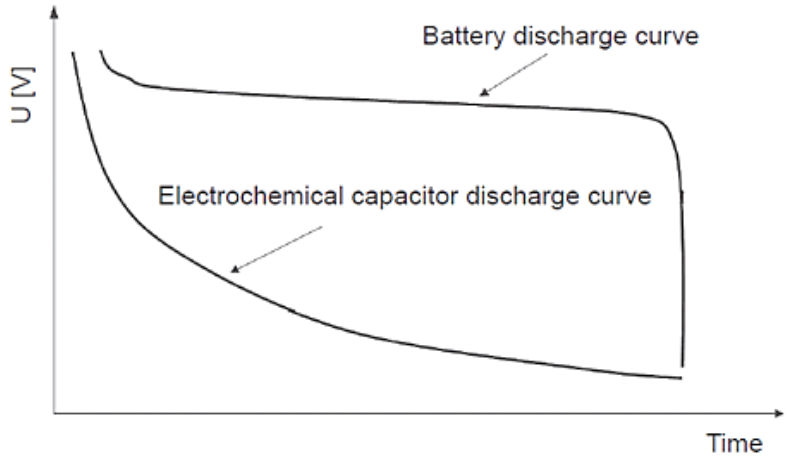


Fig. 1.4 Discharge curves of Electrochemical Capacitor and a Battery [42]

1.4 Micro-grid Interfacing Converters

The world is now full of electronic devices without which it is very difficult for mankind to keep going. So it is very important to develop devices that are reliable, fast, and highly efficient. In our field of interest, there are two main sources: FC generator and ultra-capacitor. These sources should be connected to the DC micro-grid as high voltage is needed (high voltage transmission is used to reduce losses of power, since the power transmission loss is proportional to the square of current and resistance of the conductor). Power converters are necessary to interface between the micro-grid and the above sources. Power converter circuits manage the flow of electrical energy between an electrical source and a load. A number of converter configurations, such as AC–DC rectifiers, DC–DC converters, and DC–AC inverters, are necessary to attain the many

functions within a micro-grid, as shown in Fig. 1.2 and Fig. 1.3. Power converters can be classified based on various categories. These converters can be classified as isolated and non-isolated converters, unidirectional and bidirectional converters, step-up and step-down converters, single input and multi-input converters, low power application and high power application converters etc. However, the field is still open for more study and development for different power converter topologies. The converters are studied based on their efficiency, dynamic response, gain, switch stress, switching loss, robustness, voltage and current ripple, harmonics, wide operating range, etc. A number of converter topologies that are used to interface the FC and ultra-capacitor are reviewed in chapter two.

1.5 Power Electronics Simulation Software

Power electronics computer aided simulation and design (PE-CAD) tools play a vital role in the design and analysis of the converters. Various types of software are used to simulate those converters such as MATLAB, PSIM, PSpice, SABER, and MULTISIM. Using these software packages helps the researcher to have optimum design of power electronics circuits. Moreover, it is possible to identify performance improvements. Evaluation of the effects of noise and signal distortion without the need for expensive measuring instruments is possible. Despite the advantages of this simulation software, they have a number of limitations such as their inability to support an interactive method of solution. If the elements of a circuit are fully specified, the response can be predicted [43] PSpice software is the most commonly used software in power electronics since it uses accurate models of devices, often supplied by the device manufacturers, which are valid under all conditions, including transients.

1.6 Aims and Objectives

The aim of this research study is to investigate and develop high-efficiency power electronic converters for the interconnection of various elements within a DC micro-grid. The main focus is on the power electronic converter topologies for connecting fuel cells and ultra-capacitors to a DC micro-grid for stationary power distribution systems. The objectives of this research can be divided into the following parts:

- To identify converter topologies that match the output characteristics of fuel cells and ultra-capacitors for integration into a DC micro-grid.
- Propose new optimised circuit topologies to maximise performance, efficiency and reliability of the system components.
- Determine limitations of the proposed driver circuits and devise appropriate remedial solutions. Produce simulation models for the converter circuits to be used to aid control system design.
- Propose controller methodologies for the converters with sufficient flexibility for them to exploit the performance of the converters and to work within an overall control scheme for a micro-grid system.

1.7 Outlines of the Thesis

The structure of the thesis is organized as follows: Chapter one presents an introduction to the micro-grid configuration and its components. In Chapter two, the fuel cell and the ultra-capacitor characteristics are described and studied. Experiments have been conducted on a fuel cell to establish the steady-state and the dynamic performance of this source. A number of fuel cell–ultra-capacitor DC micro-grid configurations are presented. The advantages, disadvantages, and features of several unidirectional and bidirectional DC–DC converter topologies for the fuel cell and ultra-capacitor applications are discussed. In Chapter three, the fuel cell converter is investigated.

Simulations using the software packages (PSpice, Matlab, and SLPS) are used to validate the converter model. The converter timing control and firing pulses are described. An efficiency and performance improvement of the converter will be investigated by introducing a new active clamp circuit. An efficiency test has been carried out and a prototype model has been tested in the laboratory. A comparison was made for both simulated and measured efficiency using different sources connected to the converter (Fuel cell, and a standard DC source).

In Chapter four, the current fed converter controller is described and implemented using the dSPACE. Chapter five presents the UC converter design, modelling, and implementation. The converter timing control is also described. Finally, chapter six concludes the main findings of the study and offers suggestions for future work.

Chapter Two

Chapter Two

DC Micro-Grid Configuration

2.1 Introduction

As described in the previous chapter, FCs and ultra-capacitors are considered as components of the DC micro-grid to provide the steady-state and transient power demanded by the load. Power converters are needed to interface these sources with the DC grid bus-bar. Many different power converter topologies have been described in the literature. The power converter plays a vital role in improving the overall efficiency of the micro-grid. For the FC a unidirectional DC–DC converter is suitable. On the other hand, for the ultra-capacitor a bidirectional DC–DC converter is necessary to allow charging and discharging the ultra-capacitor.

2.2 Ragone Plots

Ragone Plots can be used to describe the relationship between the energy density (in Wh/kg) and the power density (in W/kg) for FCs, batteries, and ultra-capacitors [44, 45]. Unlike batteries, the fuel cells can provide power for very long periods. However, these cells are restrained by the available amount of fuel. Yet, it has a very low power density (Fig. 2.1). When there is a high transient power requirement within the dc grid, such as a high load disturbance, the fuel cell cannot provide the demanded amount of power within the required time. Fig.2.1 also shows that the ultra-capacitor has a high power density [46]. Hence, it is capable of providing a large amount of energy within a short time.

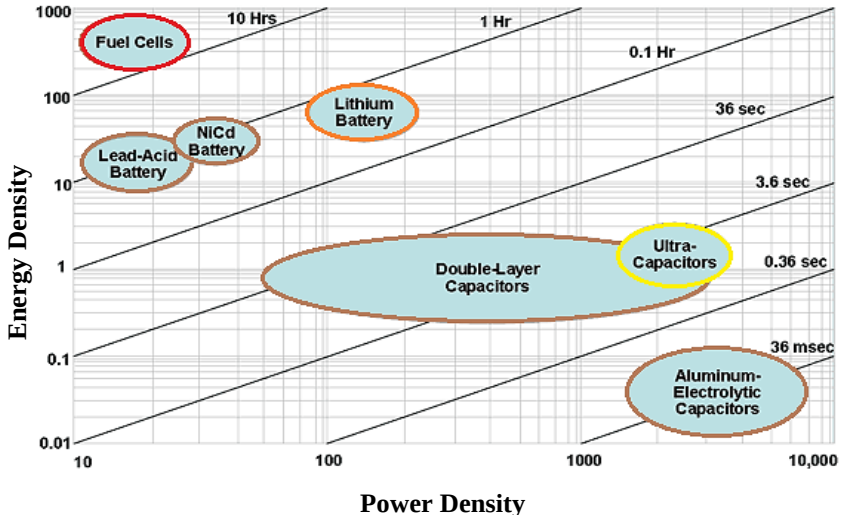


Fig. 2.1 Ragone Chart

2.3 Fuel Cell system

In this work, only considered the power generation using fuel cell. The fuel cell was invented by William Grove in 1839, and its principle of operation, shown in Fig.2.2, has not changed over more than 160 years [13, 47, and 48]. As shown in Fig.2.2 a catalyst on the anode separates the applied hydrogen into electrons and positive ions. The anode and the cathode electrodes are separated by a membrane which allows the positive ions only to pass through and rejects electrons. This process will force the rejected electrons to flow through an external path to the cathode and thus generate an electric current. Once the electrons reach the cathode, they will recombine with the oxygen atoms and the hydrogen ions to produce water and heat. The following chemical reactions describe the processes involved [11, 49, 50, 51, and 52]:

Anode side: $2H_2 \rightarrow 4H^+ + 4e^-$ (2.1)

Cathode side: $O_2 + 4H^+ + 4e^- \rightarrow 2H_2O$ (2.2)

Overall process: $2H_2 + O_2 \rightarrow 2H_2O$ + heat + electricity (2.3)

The principle method of operation of the polymer electrolyte membrane (PEM) fuel cell is demonstrated in Fig.2.2.

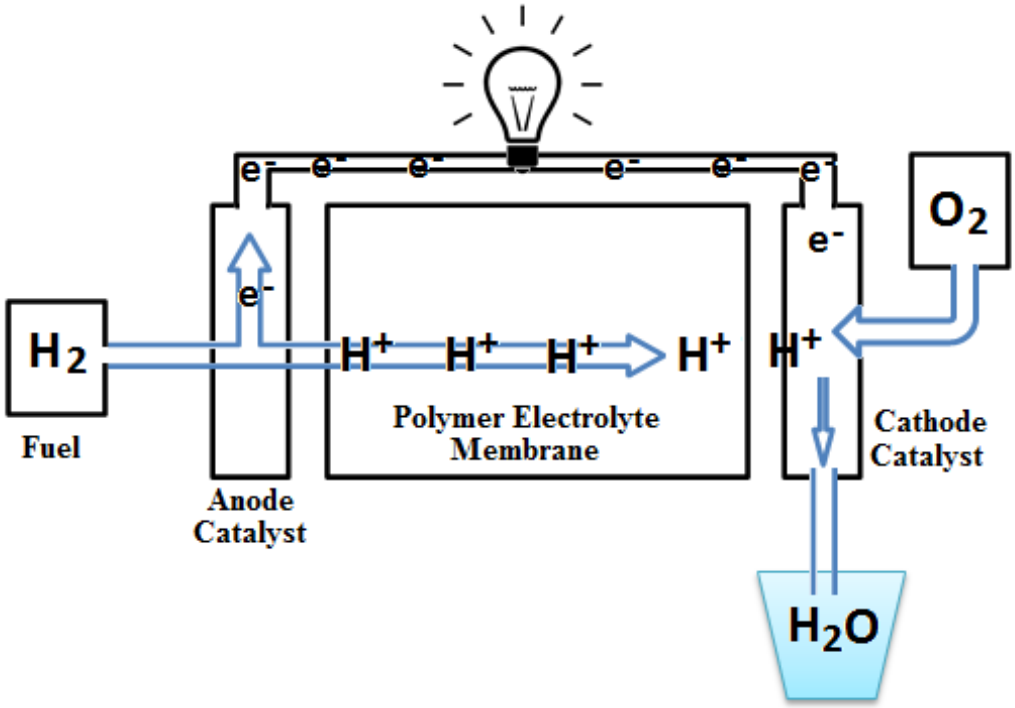


Fig.2.2 PEM Fuel cell principle

The fuel cell is considered as one of the promising technologies for electricity generation due to its many advantages such as: high power density with unlimited operation time, potential indoor use since it has zero emissions, environmental friendly because it generates DC power with only water and heat as by-products [53, 29]. In addition, fuel cells can continuously produce power as long as the fuel is supplied. However, at present the costs of hydrogen is relatively high in comparison with conventional fuel, and its wide spread use will require a substantial reduction in costs and/or environmental legislations.

The fuel cell has a relatively slow dynamic response to sudden load changes which could cause problems in a fuel cell based system [54, 55, 56, and 57]. In order to overcome the slow response of the FC to the sudden load changes and improve the FC performance, energy storage devices such as ultra-capacitors or batteries are required to fill the temporary mismatch between the load demand and the FC output [58, 59, 60, 61, 62, 63, 64]. Furthermore, storage devices can improve the efficiency of the whole system.

2.4 Fuel Cell Characteristics (Voltage-Current characteristic of the FC)

Since the FC uses two electrodes (anode and cathode), its construction is similar to that of the battery [13]. The main advantage of the FC over batteries is the ability of the FC to deliver DC power as long as hydrogen fuel is supplied. However, in the FC a larger internal voltage drop is incurred. This is due to the activation losses, the ohmic losses, and the concentration losses [13], as a result of the local chemical processes involved. Fig.2.3 shows the V-I characteristic of a single cell of a FC which illustrates the effect of these losses in the FC. The activation loss happens because of the sluggish response of the electrochemical reaction of hydrogen and oxygen as a result of electrode kinetics. This creates a highly non-linear voltage drop at low current densities as can be seen in Fig. 2.3. Ohmic losses originate from the flow of electrons through the electrolyte and electrodes. Unlike activation losses which are non-linear, ohmic losses are essentially linear and are directly proportional to the current density. Concentration losses result from the inability of the surrounding material to maintain the initial concentration of the fuel at high currents [65, 66].

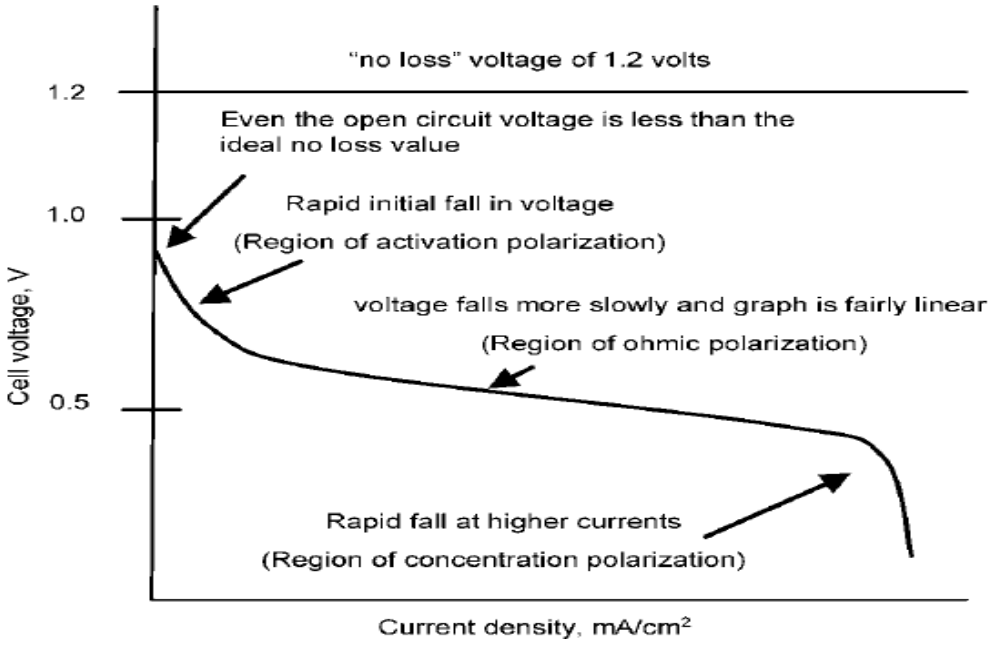


Fig.2.3 FC voltage-current characteristics [66, 67].

To obtain an efficient use, the FC is normally operated in the ohmic polarization region. This is the reason why the FC is often modelled as an ideal DC voltage source with an internal series resistance as shown in Fig.2.4 below.

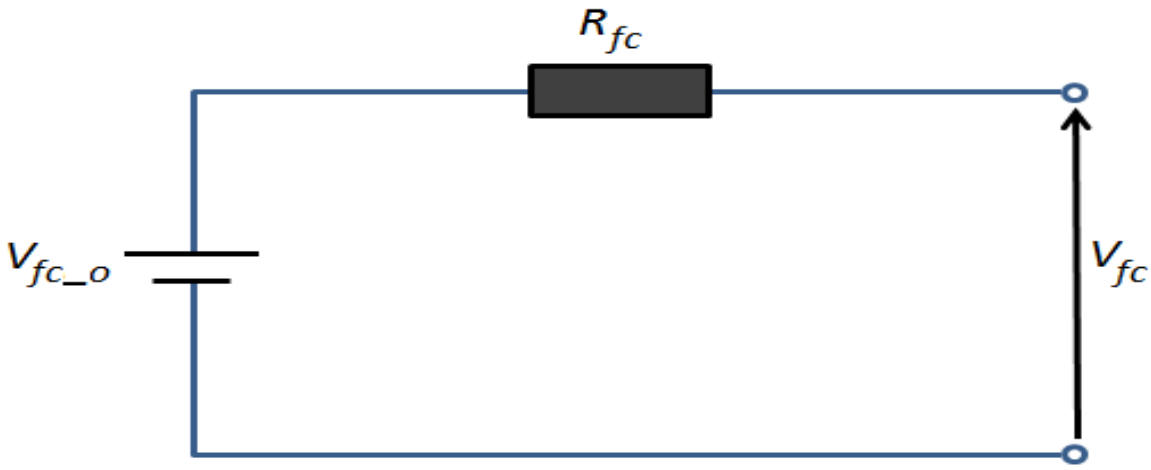


Fig.2.4 Simplified equivalent circuit of a FC

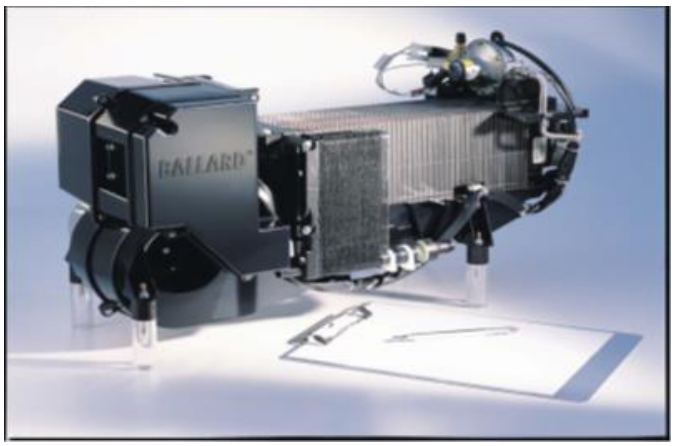
2.5 Fuel Cell Modelling and Experimental Set-up

In order to design an efficient controller for the fuel cell converter, the exact dynamic response of the FC needs to be measured. As the Nexa 1.2kW FC module will be used in this research, tests were conducted on the Nexa module to establish its response to load changes, as will be described in the next section.

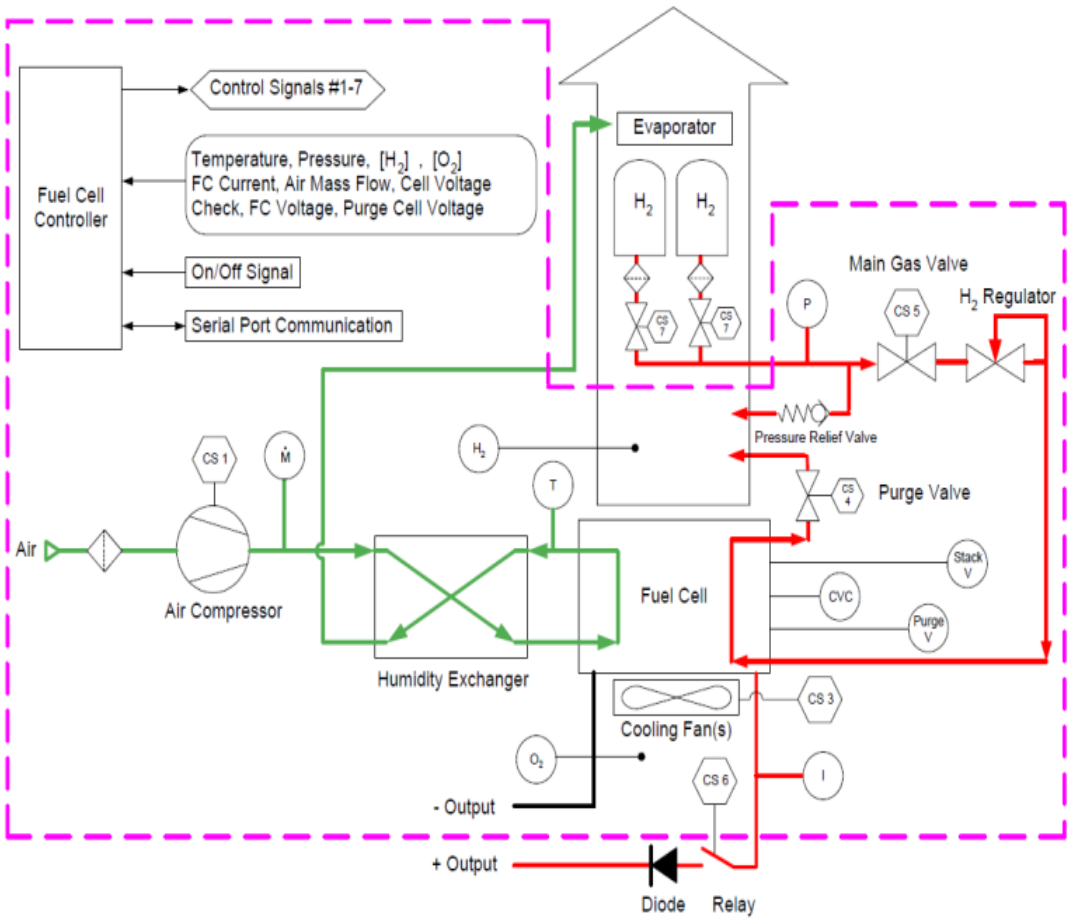
2.5.1 Nexa 1.2kW FC Module

One of the popular PEMFC technologies is the Nexa power module. It is a fully integrated system that produces unregulated DC power from a supply of hydrogen and air. It contains a BALLARD fuel cell stack, as well as all the ancillary equipment necessary for fuel cell operation. Ancillary subsystems include hydrogen delivery, oxidant air supply and cooling air supply. On board sensors monitor system performance and the control board and microprocessor fully automate the operation. The Nexa system also incorporates operational safety systems for indoor operation. Table 2.1 describes the main

specifications of the Ballard Nexa FC Power Module [68]. Fig.2.5a shows a picture of the Nexa power system, and a schematic of its internal components is depicted in Fig.2.5b.



(a)



(b)

Fig.2.5 (a) Photo of the Nexa power module set, (b) Nexa System Schematic

TABLE 2.1: MAIN SPECIFICATIONS OF THE BALLARD NEXA FC POWER MODULE

Start-up process of the system	**10-30s from cold starting to running state**
H2 pressure ranging	0.7-17.2 bar
Composition for H2	99.99%
Composition for O2	21% (from air supply)
The maximum acceptable peak-peak ripple current	35% at rated current
Ambient temperature	3.3^0C-30^0C
FC efficiency	38% at full load and 50% at light load
Maximum fuel consumption	18.5 Standard Litres per minute (slpm)
Air flow consumption	less than 90slpm at rated power

2.5.2 Experiment Setup

In order to understand the FC operation and study the response behaviour of the FC through the no-load and the load states, as needed for future research, the dynamics of the fuel cell need to be measured. The Ballard Nexa FC incorporates a control board that transmits the data via a serial communications port to a host PC. On the host PC a LABVIEW software program (NexaMon OEM Software) is installed and it provides a graphical user interface to the NexaTM module's operational status and performance. However, it only provides basic data monitoring, i.e., logging and diagnostic features that can be very helpful when conducting a fuel cell testing program in the lab, but cannot control the FC operation. Moreover, OEM Software is too slow to display the dynamic behaviour of the fuel cell. Fig.2.6 shows the main screen of the NexaMon OEM software.

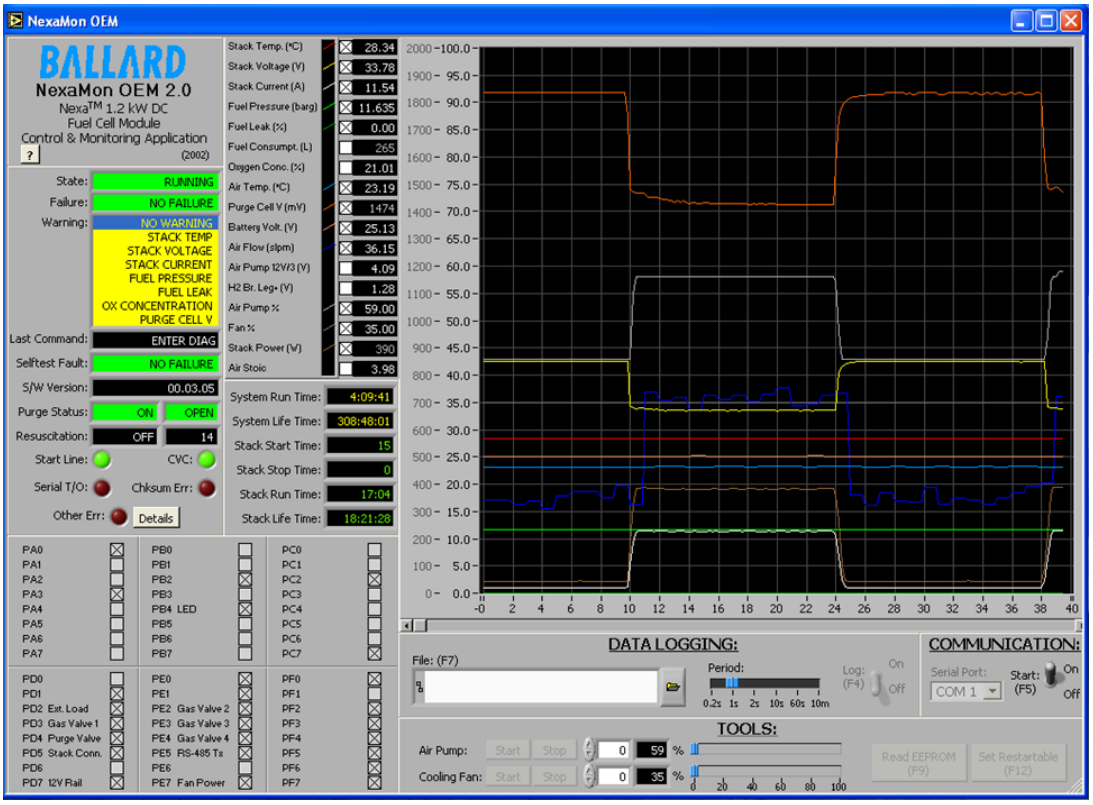


Fig.2.6 The main screen of the NexaMon OEM software

Therefore, an experiment was implemented by using the Nexa 1.2kW power module as shown in Fig.2.7.

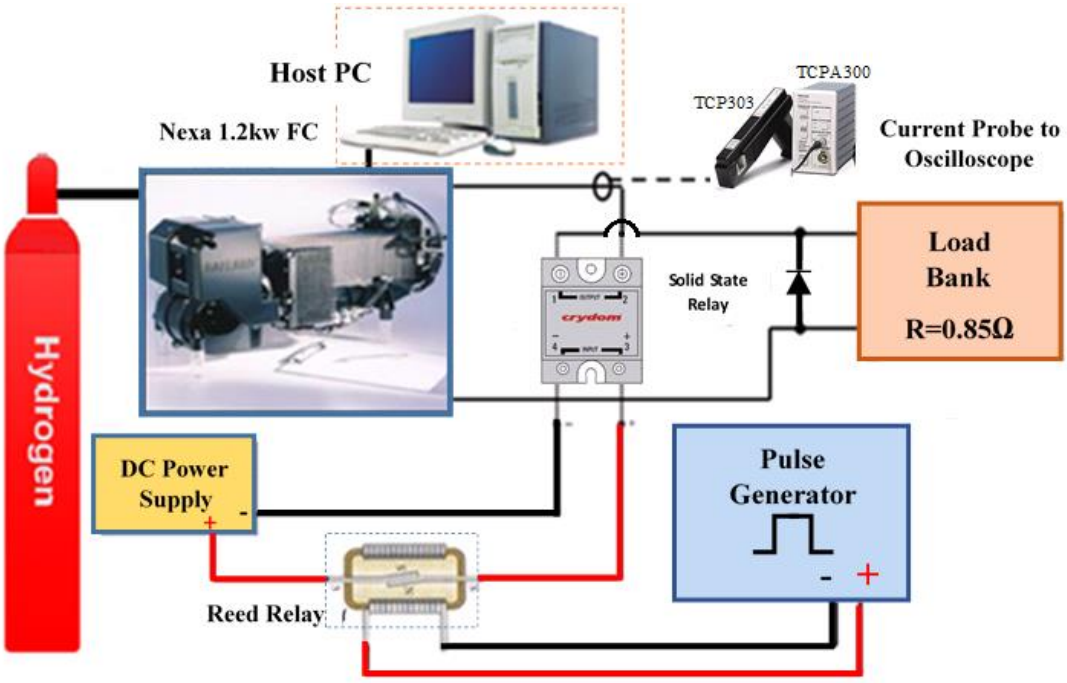


Fig.2.7 The experimental set-up of the Nexa 1.2kw power module

The experimental setup includes a low inductance resistive load bank with four 0.85 ohm sections. In order to record the accurate response result, a digital phosphor oscilloscope (TDS3014B) has been used. As can be seen from Fig.2.7 a switching relay (Crydom D06D) was connected between the FC and the load. In order to control the operation of the solid state relay, a reed relay was connected in series between the 5V power supply and the solid state relay. Using a pulse generator set to approximately 70 mHz and applied to the reed relay coil, the on/off state of the solid state relay was controlled. The experiment was set for two different loads; firstly it was set with four resistor sections that were connected in series, thus applying 3.4Ω across the FC and drawing 11.6 A. and secondly the load were set with three resistor sections with two sections connected in series and paralleled with the third section, thus applying 0.57Ω across the FC to draw the nominal current of 46A (using a current probe (TCP303) of 15MHz BW and 150A DC, connected to a current probe amplifier (TCPA300) of 100 MHz BW). In order to operate the unit, a 24V power supply was connected to support start-up and shutdown load. Fig.2.8 shows the measured transient response of Nexa FC Power Module using the "Nexamon OEM" data log file [68], and Fig. 2.9 shows the accurate transient response using the experimental set-up in Fig.2.7.

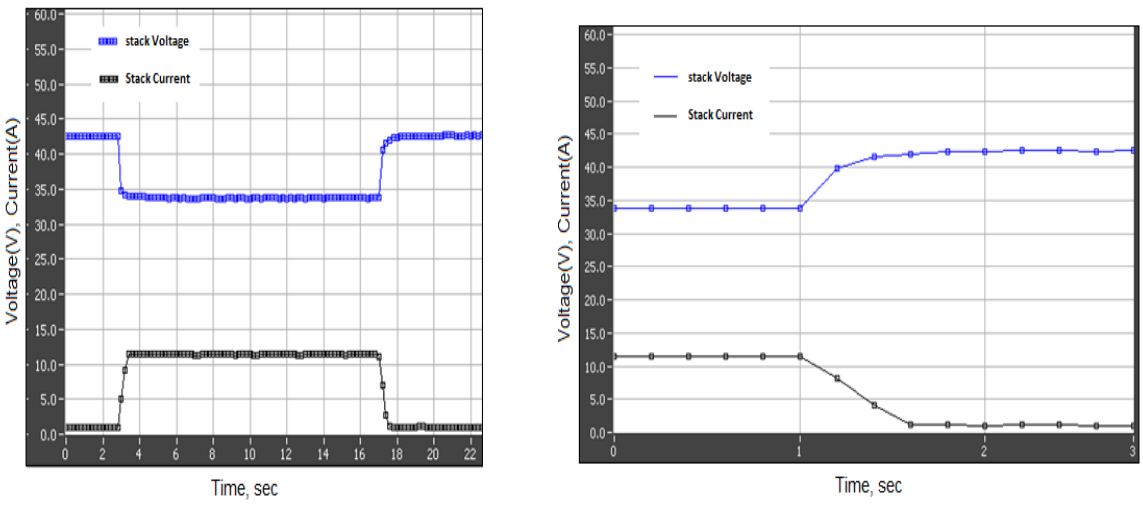


Fig.2.8 Measured transient response of Nexa FC Power Module using "Nexamon OEM" data log file

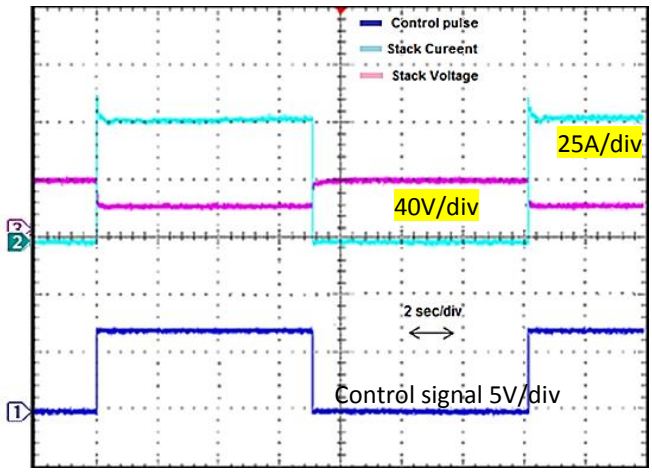


Fig. 2.9 Accurate transient response using experimental set-up in Fig.2.7

Fig.2.9 shows the change of the current from the no-load to the load state and the voltage drop due to the load change. It can be seen that when the load current steps up from 0 A to 11.6 A the FC output voltage changes from 42 V to 34 V in 0.4 sec which is due to the internal resistance of the cell. That means the FC needs time to recover to the steady state voltage which demonstrates that it cannot keep the output voltage constant during the load change. This shows that, a dc-dc converter is needed to obtain a constant voltage. As can be seen in Fig.2.8 at the no-load state, there is small amount of current (about 1A) drawn from the FC stack due to the ancillary loads (such as control board, pump, and cooling fan). Fig.2.9 shows that when full-load is applied from no-load the gross stack current initially increases to about 1.2 times the nominal current (46A) before settling to the rated value in about 0.24 second. In comparison, the recorded response in the FC "Nexamon OEM" data log files, taken under the same condition (Fig.2.8) doesn't show this current spike. Fig.2.10 shows the extra current peak from during the no load transition. This is due to the charge of the double-layer on the FC electrodes during no-load. However, this double layer does not exist during normal load operation and the load response is normally much more sluggish.

Fig.2.10 Fuel cell current transient at load application from no-load on first load application

2.5.3 Fuel Cell Internal Resistance

The measured external V-I characteristic of a Nexa 1.2 kW FC (details below) is shown in Fig.2.11, where it can be seen that under normal operation the voltage drop is mainly due to ohmic losses. This is the reason why the FC has been modelled in this study as a DC voltage source of V_{fc_o} = 35 V with a series resistance of R_{fc}=0.25 Ω. The open-circuit voltage of the module is 46V, but this drops rapidly under load due to the activation polarization.

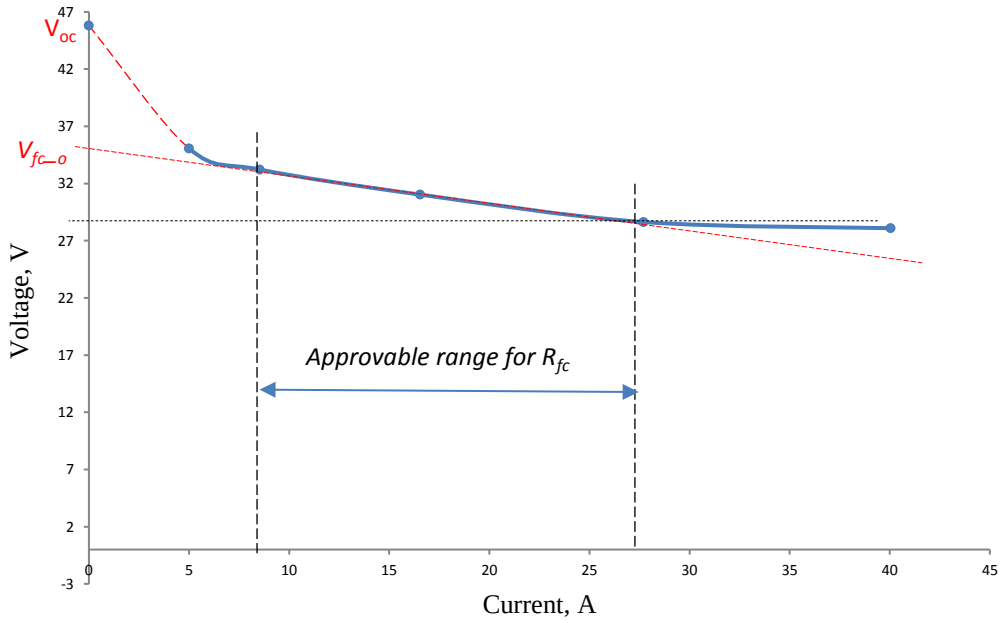


Fig. 2.11. Measured Nexa 1.2kW FC voltage-current characteristic

2.6 Fuel Cell Converter Selection

Wind and PV power generation is subject to unexpected power changes associated with weather changes. A fuel cell (FC) can provide a solution for the uncertainty of environmental changes. FCs use hydrogen as the main energy source which can be generated from a variety of sources such as hydrocarbons or water via electrolysis [26, 69].

Fuel cells are clean and efficient electricity generators that have great potential for the near future. They can be alternative energy generators for transportation, communications, computing and residential systems. Fuel cells produce low output voltages so the voltages and current can easily have the same order of magnitude in kilowatts applications. However, the output voltage of the FC is load dependent (see Fig.2.11) and most loads require a higher and constant supply of voltage to operate correctly. Thus, it is necessary to use a step-up converter to interface the FC to various loads [28, 70, and 71].

A fuel cell for a distributed DC power generation system at an elevated DC voltage requires a power DC-DC converter in order to step up the fuel cell DC output voltage to meet the bus voltage. The main requirements for the power converter for FC applications are high efficiency during load operation, a large step-up ratio, a low input ripple current and galvanic isolation [72, 73].

Two types of converter topologies can be used to boost operation: isolated and non-isolated front-end converters [74, 75]. However, non-isolated converter topologies may not be appropriate for an FC converter due to direct connection to the high voltage output side. Also, the FC converter must achieve a high boost ratio which is difficult to accomplish in a non-isolated converter [76, 77]. Therefore, a DC-DC converter with a

high frequency transformer (HF) is generally used to provide not only galvanic isolation from the DC bus bar, but also to permit interconnection of the DC-DC converters [78].

2.7 Fuel Cell Converters with High Voltage Step-Up Ratio

2.7.1 Voltage-fed vs Current-fed Converter

There are many different isolated DC-DC converter topologies presented in the literature. Front-end converters with an HF transformer can be classified into two topologies: voltage-fed converters (VFC) and current-fed converters (CFC). Fig. 2.12 shows a typical arrangement for a VFC.

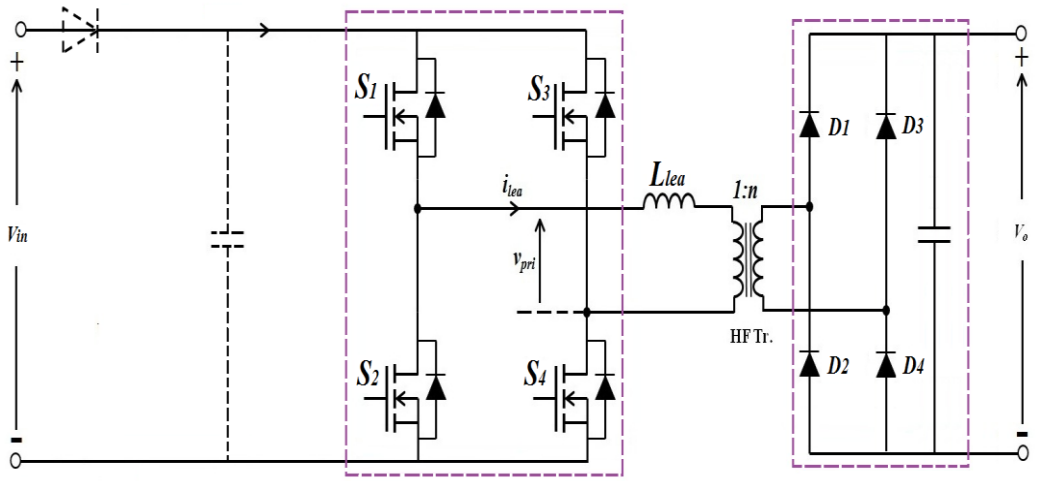


Fig.2.12 Typical topology of a voltage-fed DC-DC converter.

Due to its principle of operation, the VFC suffers from a large input current ripple that may even lead to current reversal which is not acceptable for FC operation. To avoid reverse and pulsating current flow in the FC a series diode must be inserted in the FC output and a large buffer capacitor must be placed at the converter input (shown dashed in Fig.2.12). However, at the prevailing low output voltage of an FC a series diode will result in a sizable voltage drop which will reduce the efficiency of a VFC. In the VCF topology, the voltage boosting action is only achieved through the turns ratio of the HF transformer. In order to avoid through-shoot in either leg, a blanking time must be

imposed between the pulses for the upper and lower switches, which affects the achievable boost action.

In contrast to the VFC, in a CFC the boosting action is obtained from both the converter operation and the transformer winding ratio. A typical arrangement for a CFC is shown in Fig. 2.13.

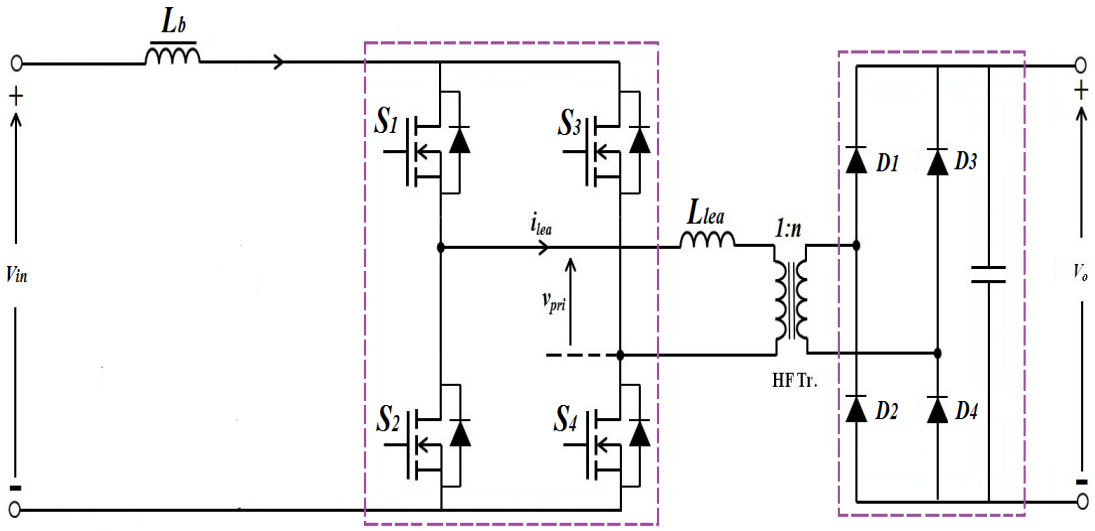


Fig. 2.13 Typical topology of current-fed DC/DC converter.

During operation, the bridge is periodically shorted by turning on all switches (S_1-S_4) in order for the current in the boost inductor (L_b) to build up and store energy. Then two diagonal switches turn off (S_2 & S_3 or S_1 & S_4) and the inductor current is diverted into the transformer primary and subsequently to the load. The process is repeated with the other two diagonal switches opening to reverse the current in the primary winding. Due to the inherent boost action of the CFC, a lower winding ratio is needed with a consequent reduction in the leakage inductance, hence improving the converter efficiency [79]. In a CFC the input current ripple is small, and the frequency is twice the switching frequency; this helps to reduce the inductor size for a given maximum input current ripple requirement. Also, input current reversal is impossible in a CFC and a series diode is

therefore not required. In view of the low input voltage of the bridge, MOSFET switches are mostly employed in the input bridge due to their lower on-state voltage.

2.8 Full-bridge Current-fed Converter with Regenerative Clamp Circuit

The full bridge current fed converter (FBCFC) with HF transformer is the most suitable converter for achieving durability and efficiency of the FC because it is unidirectional and has low-ripple current. The main drawback of the FBCFC is the presence of the leakage inductance of the HF transformer, which leads to a high voltage overshoot across the main switching devices during turn-off of the bridge diagonal switches. Fig. 2.14 shows the voltage overshoot and subsequent ringing across the main bridge switching due to the leakage inductance which impedes a rapid current transfer to the primary winding. This result was obtained without any clamp or snubber across the bridge or the switches. It can be seen that the voltage overshoot across the switching devices is approximately Four times the bridge input voltage. The test in Fig.2.14 was carried out with an input voltage of less than 20V to protect the MOSFETs. At the no-load voltage of a FC (typically 50V) the voltage rating of the MOSFETs (200V) would be exceeded and the high voltage overshoot could destroy the devices. Of course, MOSFETs with a higher voltage rating can be selected to withstand the switching transient, but the converter efficiency will suffer because of the losses associated with the ringing and the higher on-state resistance of higher voltage MOSFETs.

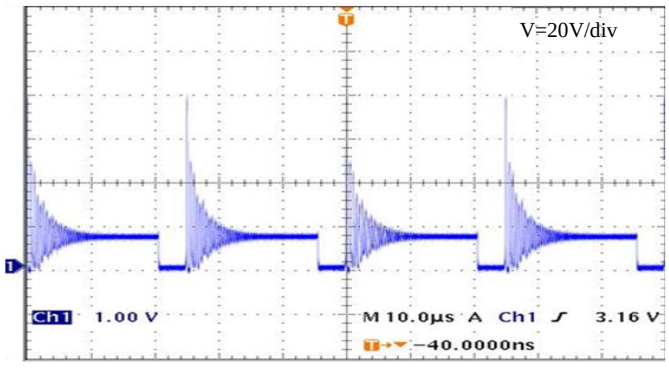


Fig. 2.14 Voltage overshoot across the switches of the FBCFC

In order to avoid this overshoot, passive or regenerative clamps or snubbers can be added. However, passive clamps and snubbers waste the FC's energy. An active regenerative clamp was introduced in [80] as shown in Fig. 2.15. This clamp consists of an auxiliary switch in series with a capacitor; this configuration is further referred to as a conventional active clamp circuit (CACC). This circuit, together with further modifications to improve its efficiency, is described in chapter three.

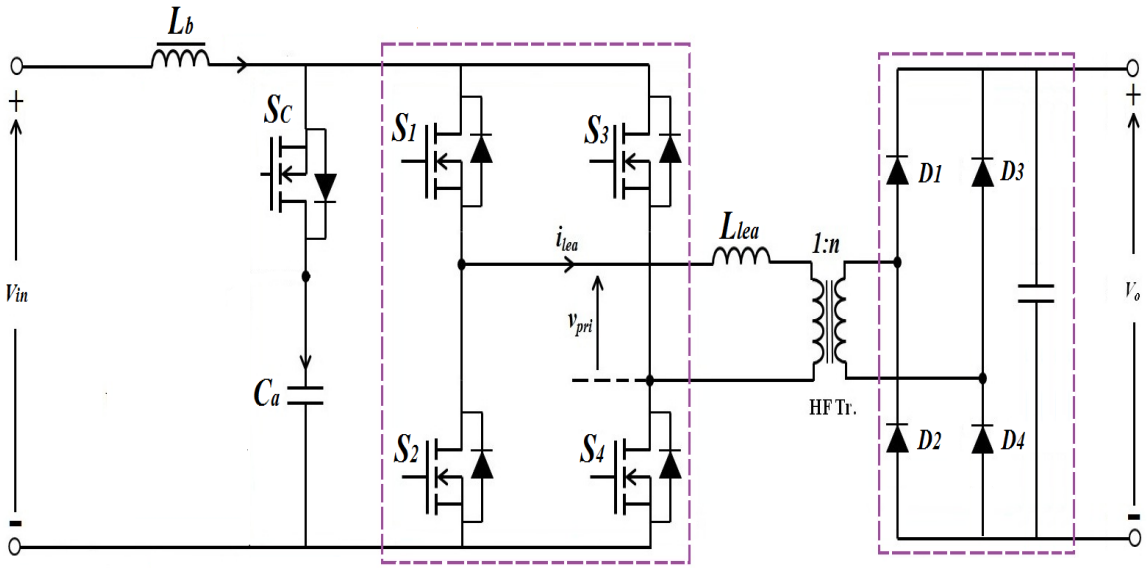


Fig. 2.15 FBCFC with CACC [11]

2.9 Ultra-Capacitor System

As shown in Fig. 2.16, the Ultra-Capacitor (UC) consists of two electrodes, a separator, and an electrolyte. In an UC, energy is stored by the separation of positive and negative charges at the interfaces between the electrode and the electrolyte. This is called the double–layer capacitor phenomenon [38, 81].

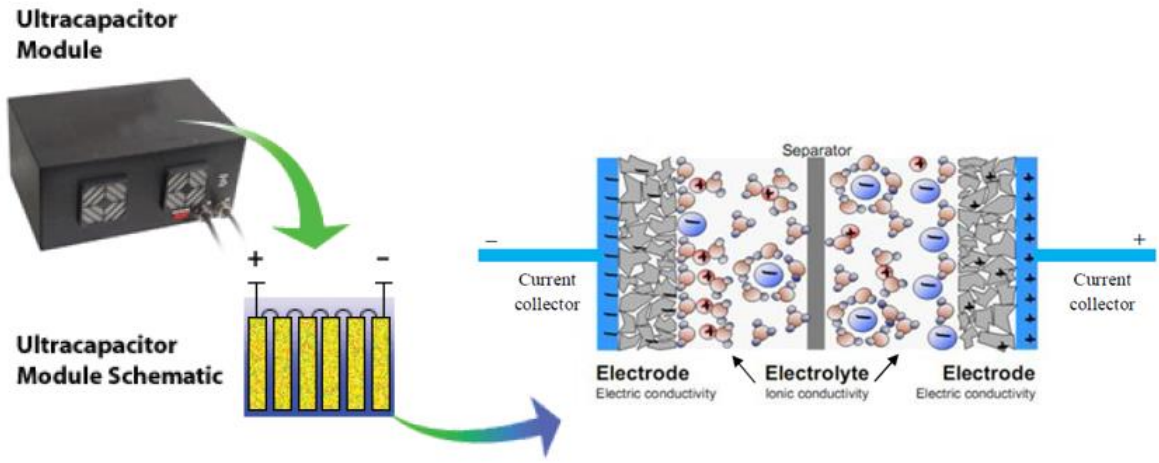


Fig. 2.16 Principle of the ultra-capacitor [42]

UCs currently have a breakdown voltage of 2.67 V per cell [82, 83]. Therefore, UCs are generally purchased as modules consisting of several cells stacked in series and parallel to increase the voltage and energy storage for a specific application.

The performance of an UC can be characterised by its terminal voltage during discharging and charging at different current rates. Unlike batteries, the parameters of an UC depends on the voltage, rather than the current, since the charge stored is based on the capacitance and the voltage. An UC's voltage profile has capacitive and resistive components. The capacitive component indicates the charge or discharge energy within the UC. The resistive component represents the voltage drop due to the internal ESR of the UC [84, 85]. The voltage profile of the UC during constant current discharge is illustrated in Fig. 2.17.

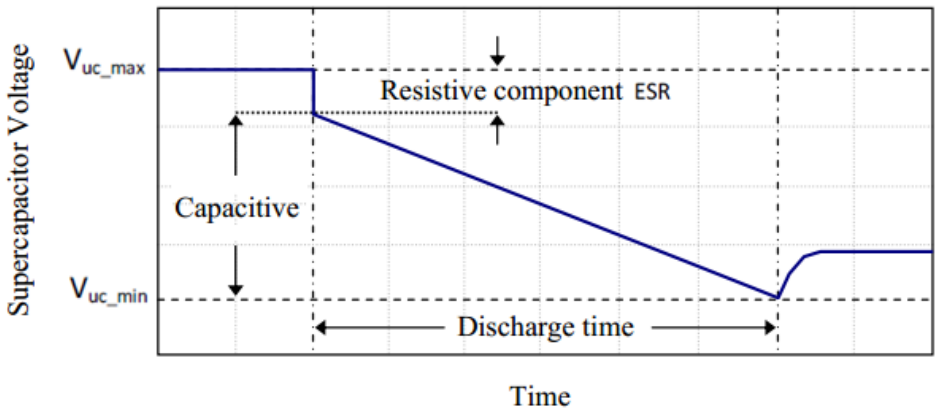


Fig. 2.17 Constant current discharge profile of the UC [85]

Compared to batteries, UCs can deliver 10–20 times more power and they can be discharged and charged very fast [38]. This important feature makes them a suitable companion for an FC since it can match the slower power output of the FC and thus provide the required transient power for the DC load or AC grid to improve the performance characteristics of the FC-UC DC micro-grid. However, this feature will only be of use if a suitable DC-DC converter has been selected to connect the UC to the DC grid. The ultra-capacitor is equivalent to an ideal capacitor C and a small series resistance R, the equivalent RC charging circuit is shown in Fig. 2.18.

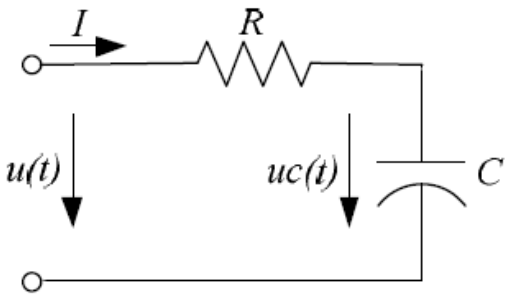


Fig. 2.18 Ultra-capacitor equivalent circuit [86]

The ultra-capacitor can be charged with a large current. However, its internal resistance would reduce the charging efficiency of the ultra-capacitor to a certain extent. Therefore the influence of the charging current on the charging efficiency of the ultra-capacitor should be considered [87].

2.10 Experimental Test of Maxwell Ultra-Capacitor

The existing UC (MAXWELL -BMOD0165 P048) will be used with the bidirectional converter (BDC). Hence, an experimental test has been carried out to investigate its value and behaviour. Table2.2 shows the MAXWELL capacitor specifications. A circuit has been designed for charging the UC with a constant current process and discharging the UC with a fixed resistor as shown in Fig.2.19.

Table2.2 Product specifications of the MAXWELL UC

Nominal Capacitance C	165F
UC Voltage Vuc	28-48V
Max continuous Current Iuc_max	98 A
Leakage current	5.2 mA
Operating Temperature range	-40^0C to $+65^0$C
Energy Available Euc	54 Wh
Number of cell Nuc	18
Capacitance of each cell Cuc	3000 F
Constant Capacitance Cco = (2/3)×C	110F
ESR, DC Rv	6.3 mΩ
ESR, AC	5.2 mΩ
Ci = Cco	110F

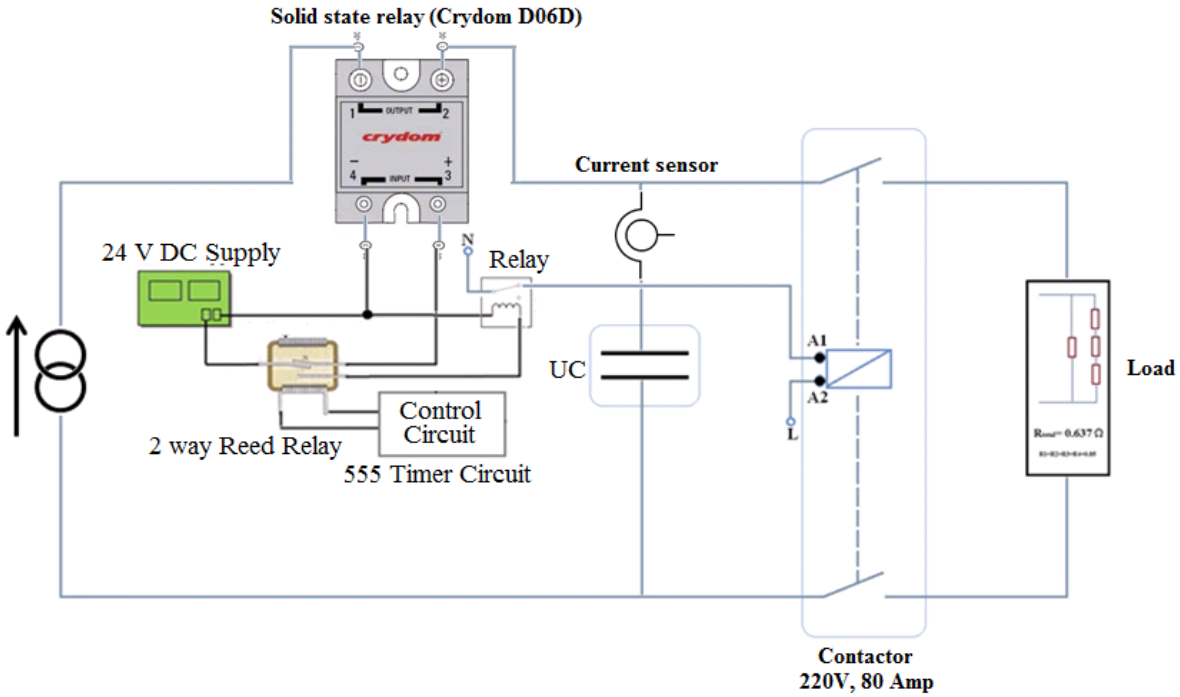


Fig.2.19 The experimental set-up of the UC Maxwell module

A low inductance resistive load bank with four 0.85 Ω sections was used for discharging the UC. As can be seen from Fig.2.19 a solid state relay (Crydom D06D) was connected in series to connect the UC and the Source (Farnell Power supply 3kW, 100V, 90 A). The contactor was used to connect the resistive load with the UC. The charging and discharging process was controlled by controlling the operation of the solid state relay and the contactor to work sequentially. Therefore, a two way reed relay has been used and controlled by a 555 timing circuit for charging and discharging the UC automatically. When the circuit is turned on, the UC starts charging until a constant voltage across the UC has been reached. Then after a pre-set time the UC will be discharged. The capacitor value was calculated for the charging period with the following formula:

$$C = \frac{i \times \Delta t}{\Delta V} \tag{2.4}$$

Where C is the capacitor value in Farads, i is the charging current, Δt is the charging period in sec, and ΔV (V_{limit}-$V_{initial}$) is the change in the voltage of the UC from initial value to a certain voltage level. Fig.2.20 shows typical waveforms of the UC voltage and current during the charging and discharging process. As can be seen from Fig.2.20 the voltage increases linearly during the charging period, and when the capacitor is fully charged the current drops to zero.

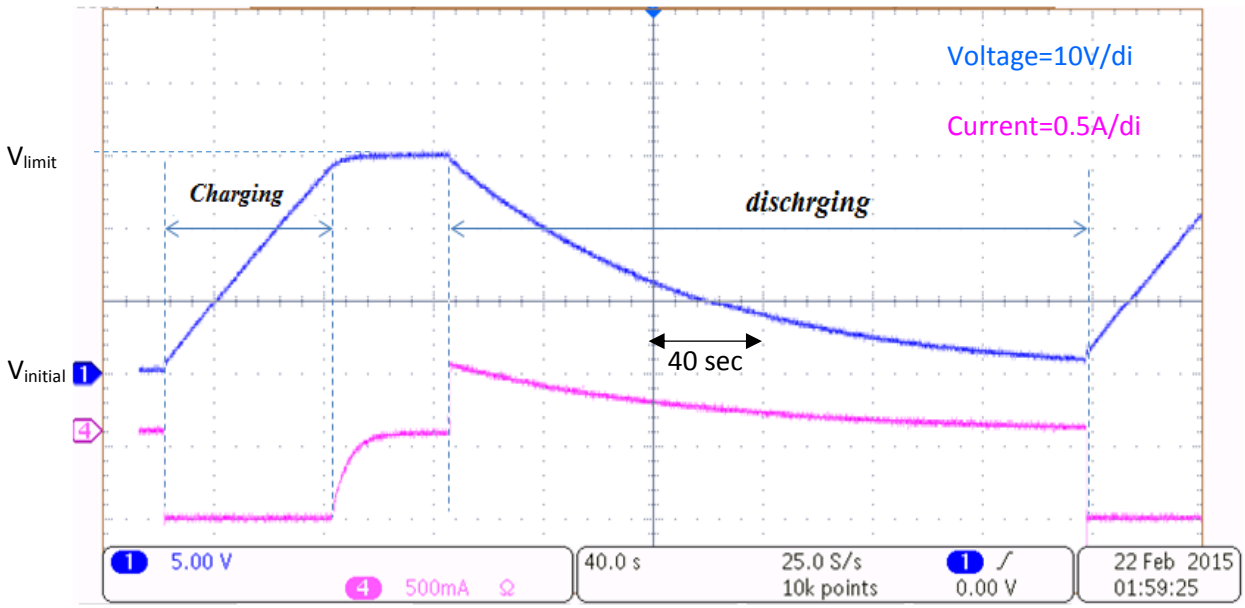


Fig.2.20 UC charging and discharging waveforms from the top: the capacitor voltage, and the capacitor current

The test was implemented with two different set-ups, firstly it was set for a constant current with different voltage levels. Secondly, for a constant voltage with different currents level as shown in Table 2.3, and Table 2.4 respectively.

Table 2.3: UC test for different voltage levels

I (A)	V_{limit}(V)	$V_{initial}$ (V)	t_{charge} (sec)	C (F)
40	12	0.0	50	166
	24	0.0	100	167
	34	0.5	140	166
	44	1.5	175	165
	48	1.5	192	165

Table 2.4: Effective UC value for different current levels

V_{limit} (V)	I (A)	$V_{initial}$ (V)	t_{charge} (sec)	C (F)
48	30	2.4	250	166
	35	2.7	216	166
	40	1.5	192	167
	45	2.7	168	166
	50	0	160	166
	55	2.0	138	165
	60	1.0	130	165

The results in Table 2.3 confirm that the actual value of the capacitor is within the manufacturers specifications. The results in Table 2.4 indicate that the amount of current during different range of operation has no effect on the value of the UC. Hence, these tests prove that the state of charge of the UC is not affected by the voltage and current levels.

Fig.2.21 illustrate another test for the UC current response during the charging and discharging processes.

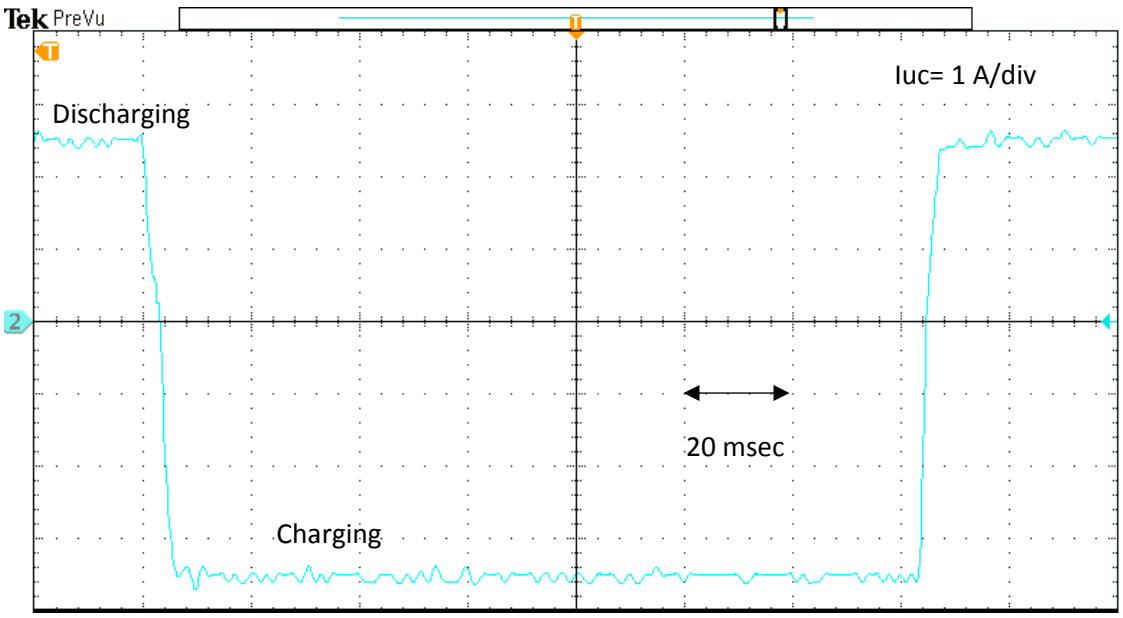


Fig.2.21 UC current during charging and discharging

It can be seen from Fig.2.21 that the UC is able to deliver power and accept power in less than five msec. Therefore, the UC is the perfect choice to back-up the FC and improve the performance of the DC micro-grid system.

2.11 Ultra-Capacitor Converter

It is a fact that fuel cells cannot respond as fast as required to sudden load changes due to their dynamic response [26, 88]. In order to improve the dynamic response of a fuel cell power source in a DC micro-grid and increase the system performance, an energy store with a fast response time such as an ultra-capacitor is required. This store is responsible for supplying energy to the DC grid during power shortfalls and absorb energy from the

DC grid during periods of excess, in order to maintain the DC grid voltage. A DC-DC converter is required to interface between the energy store and the micro-grid DC bus. The converter should be designed for both charging and discharging of the store. Fig.2.22 shows the arrangement of such a system.

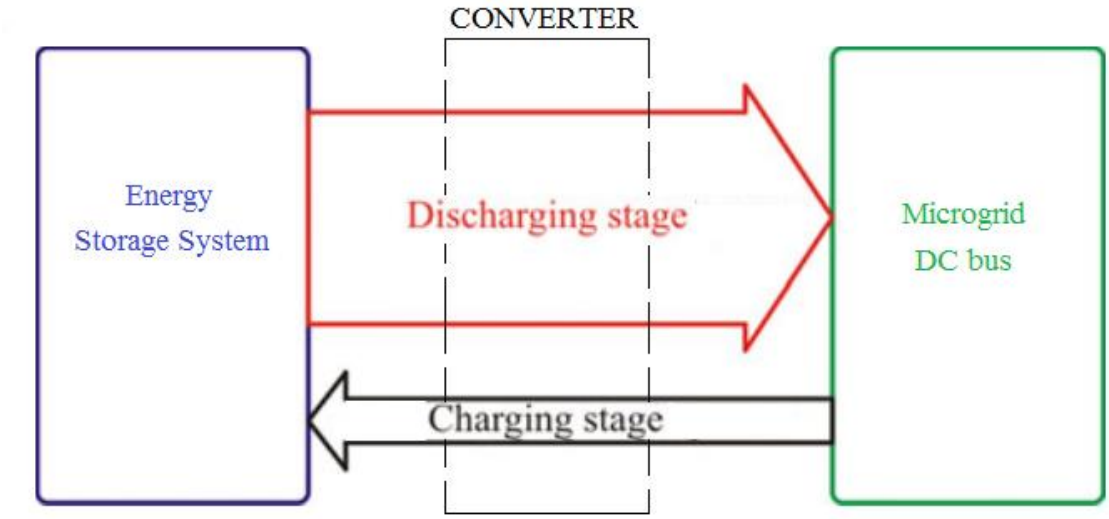


Fig.2.22 Power flow diagram between storage system and micro-grid DC bus

2.12 Isolated Bidirectional DC-DC Converters

With its capability of bidirectional energy transfer, bidirectional dc-dc converters (BDC) have recently received a lot of attention due to the increasing need to include energy storage in renewable energy systems. For micro-grid applications, BDCs are required to regulate the power flow between the energy storage devices such as batteries/ultra-capacitors and the load while also regulating the bus voltage [85, 89]. A number of isolated BDCs have been presented such as dual active bridge (DAB), dual active half bridge, full bridge current fed, and full bridge voltage fed converters [89]. Among those converters, the dual active bridge (DAB) is considered as the most appropriate converter in this field due to its features e.g. bidirectional power flow, high efficiency, power controllability, and galvanic isolation [90, 91]. The galvanic isolation and voltage matching are usually achieved by using a HF transformer.

2.13 BDC Structure and Principles of Operation

Generally, isolated BDCs have a structure similar to Fig. 2.23. As shown in Fig.2.23a, the isolated BDC can be represented as two high frequency switching DC–AC converters, Converter A (C_A) and Converter B (C_B) connected to two DC sources V_A and V_B and interfaced through an inductor L_t. As energy transfer in either direction is required, each dc-ac converter must also have bidirectional energy transfer capability [92, 93]. The DC bus in this structure must also be able to either generate or absorb energy. In order to transfer power, the voltages V_A and V_B must be supplied by the converters C_A and C_B through the inductor L_t. Hence, the BDC can be replaced by two independent AC voltage sources V_A and V_B connected through inductor L_t as shown in Fig. 2.23b. To simplify the BDC operation, the voltage and current relationships of the BDC can be analysed using the phasor diagram of the fundamental components, illustrated in Fig.2.23c.

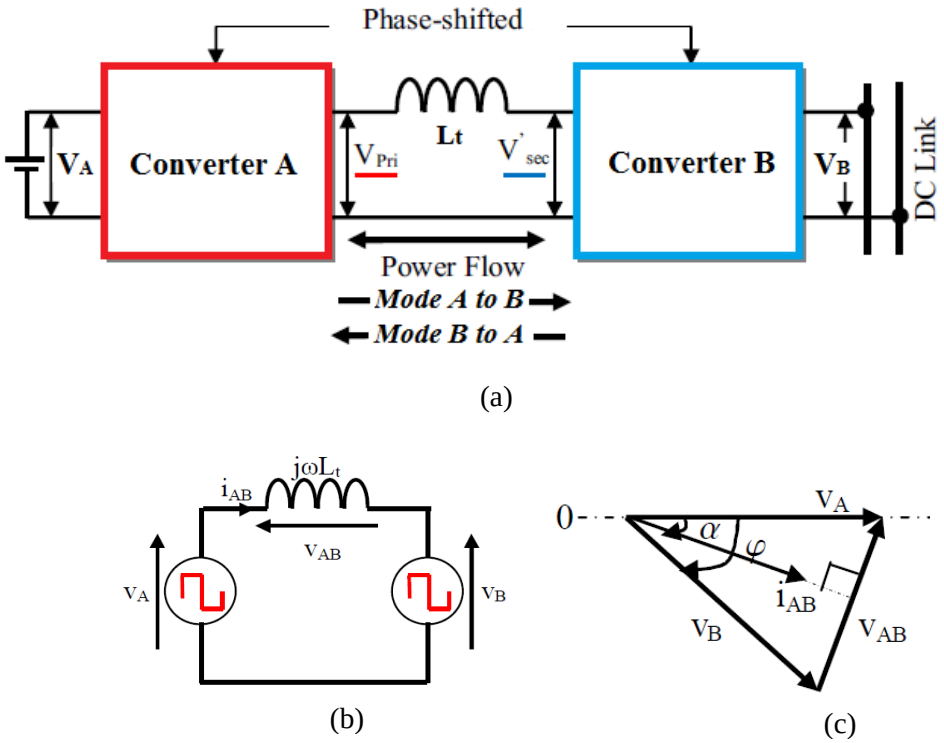


Fig. 2.23 Operating principle of a BDC (a) simplified block diagram (b) equivalent circuit model (c) phasor diagram of the fundamental components of the voltages and current

Basically, there are two modes of operation in the BDC in terms of power transfer. Based on Fig. 2.23a, these modes are indicated by Mode A-to-B and Mode B-to-A [94]. In the literature, different terms are used to describe the modes of operation such as buck and boost or step-up and step-down. Furthermore, it can be described as charging and discharging mode because of the energy store devices (batteries/ultra-capacitor) that are used.

Based on the fundamental components, the fundamental power flow between the two AC sources in Fig. 2.23c can be written as:

$$P_{AB} = \frac{V_A V_B}{2\omega L_t} \sin \varphi \tag{2.5}$$

Where, φ is the phase-shift between V_A and V_B.

It can be seen from equation 2.5 that the power direction in the BDC is determined by the phase-shift. Hence, the power transfers from source A to source B when V_B is lagging V_A (i.e. φ is larger than 0^0) and power transfer reverses in the case when V_B is leading V_A (i.e. φ is smaller than 0^0).

2.14 Common Configurations of BDCs

Different BDC configurations for UCs have been proposed in the research literature. The most interesting topology for the bidirectional applications is the dual H–bridge BDC (sometimes called the dual active full bridge converter (DAFB)), presented in [95]. Fig.2.24 shows the topology of a dual H–bridge bi-directional converter. This converter was first introduced in [96]. Full-bridge voltage-fed converters are used at both sides of the HF transformer and the control is achieved based on soft-switched phase-shift strategy to control both the amount of the power and the power flow direction. The diagonal switching pairs in each converter are turned on simultaneously with 50% duty cycle and with 180^0 phase shift between two legs to provide a nearly square wave ac

voltage across transformer terminals. The phase shift φ between the two ac voltages across the transformer is the key element which controls the direction and the amount of power transfer between the two sides of the converter.

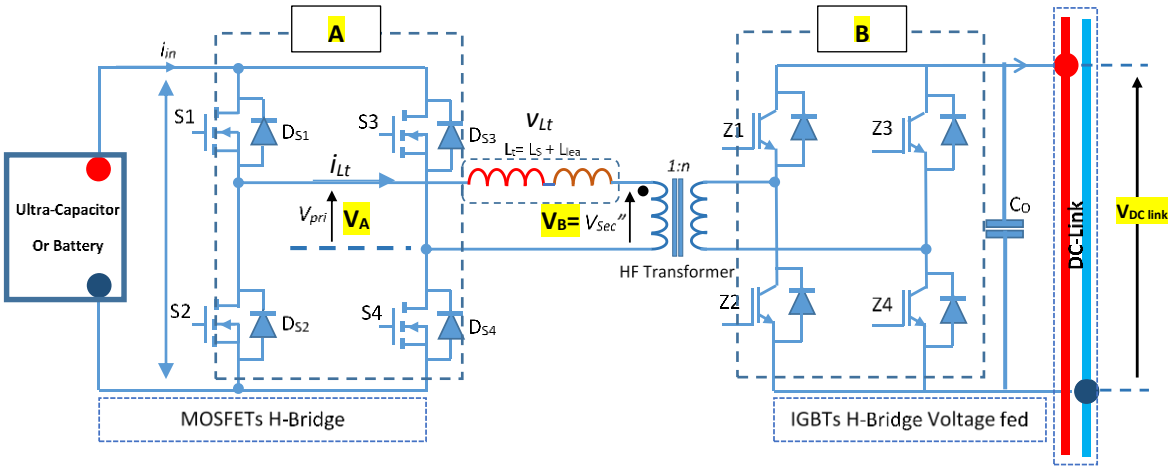


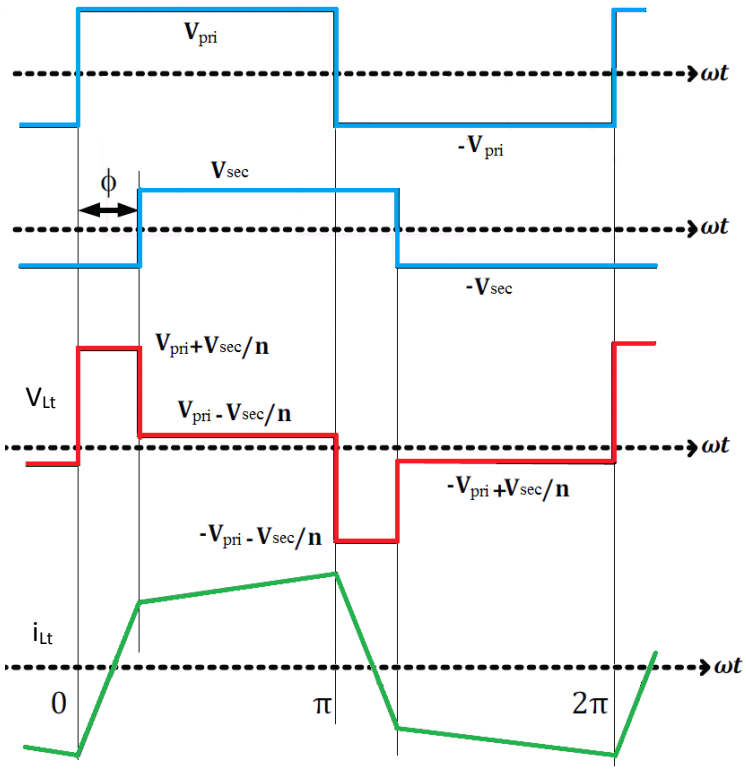
Fig. 2.24 Dual H–Bridge bidirectional converter

The average transferred power can be obtained by calculating the average power across the transformer terminals, i.e.

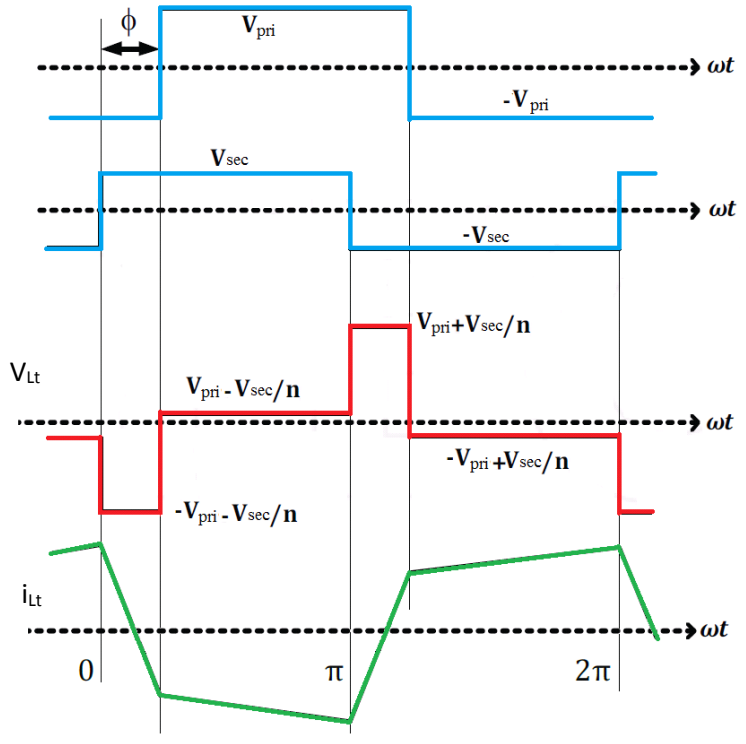
$$P_{DAFB} = \frac{1}{2\pi}\int_{0}^{2\pi} (v_{Lt}\, i_{Lt}) d\omega t \tag{2.6}$$

$$P_{DAFB} = \frac{V_A V_B}{2n\omega L_t} \sin\varphi \tag{2.7}$$

Where L_t is the series inductance plus the transformer leakage inductance, n is the transformer turns ratio and ω is the angular frequency. Fig. 2.25 shows the ideal waveforms of the converter for the two different power transfer modes. It can be seen from this figure that V_{Lt} is the voltage across the total inductance at the low voltage side of the transformer, and i_{Lt} is the resulting current also in the low voltage side of the transformer.



(a)



(b)

Fig.2.25 Operating waveforms of DAB. (a) Mode A-to-B and (b) mode B-to-A

To transfer power from side A to side B (Fig.2.25a), $v_{pri,A}$ should lead $v_{sec,B}$ and φ is considered as positive. In mode B-to-A (Fig.2.25b), $v_{pri,A}$ should lag $v_{sec,B}$ and φ is negative. This leading or lagging phase shift is simply implemented by proper timing control of the converter switches. L_t is an important element which determines the maximum amount of transferable power with a given switching frequency. Therefore, apart from other practical limitations, it is possible to reach a high power density converter with a low leakage transformer.

Generally, for high-power applications the DAFB converter (in Fig. 2.24) is preferred because it has minimal voltage and current stresses, low switching losses, and low ripple currents at the filter output [97, 98]. Another interesting topology is the isolated dual half–bridge BDC (DHB) which has also been considered for hybrid vehicle applications [99, 100]. As shown in Fig.2.26, in comparison with the converter in Fig.2.24, the main advantage of the DHB, is that the number of the switching devices is halved which reduces the size and the effort of the hardware. As a result it will reduce number of the gate drivers. Additionally, the DHB has a lower voltage stress. However, the main disadvantage of this converter is the RMS current ratings of the switching devices that should be twice the RMS current ratings of the DAFB switches [97].

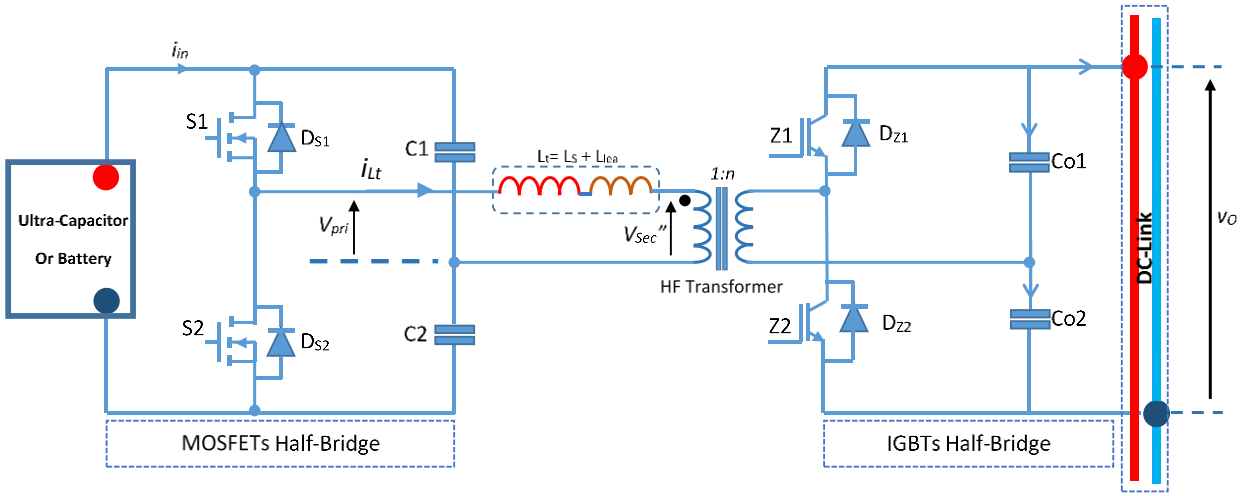


Fig. 2.26 Dual half bridge bidirectional converter

A new converter topology is proposed in [101]. By combining a bidirectional voltage doubler with an H-bridge, a converter with a lower number of active devices at the lowest voltage rating and highest efficiency can be realized. It consists of a low voltage MOSFET H-Bridge, connected to an ultra-capacitor operating from 50% to 100% of its rated voltage (from 24V to 48V), and an IGBT high voltage bidirectional voltage doubler circuit connected to the DC bus, Fig.2.27 shows the scheme of the proposed circuit. The proposed modulation scheme was verified by PSpice/Simulink using SLPS co-simulation software. This converter will be detailed in chapter five.

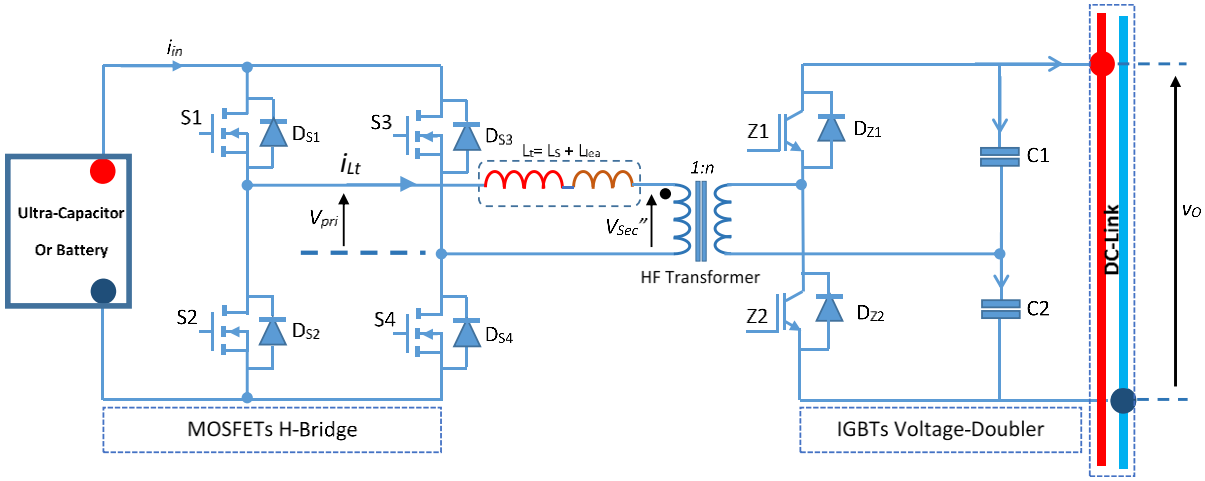


Fig.2.27 Schematic of the proposed BDC in [101]

2.15 DC Bus Connections

As mentioned previously, to compensate for the slow response of the FC to load changes in the DC micro-grid, a fast response storage energy device such as UC is needed.

Based on the FC-UC interfacing to the DC micro-grid, different types of connections have been proposed in [102, 103, 104, 105, 106, and 107]. These connections are; direct connection, one converter direct, and a two converter connection. Fig.2.28 shows the different proposed configurations for the hybrid FC-UC connections.

The configuration in Fig.2.28 (a) presents a direct connection [104]. The FC and UC are connected directly to the DC bus of the micro-grid. Although this entails lowering the

costs and decreasing losses, there is no direct control for either the FC or the UC. In the configuration proposed in [105], shown in Fig.2.28 (b), the fuel cell is connected to the DC link through a DC-DC converter and its output can be controlled. However, the ultra-capacitor is connected directly to the DC link, and the power flow between the UC and the DC bus is uncontrolled. Additionally, the UC must have a higher voltage rating.

A two-converter configuration, as proposed in [106, 107] is shown in Fig.2.28 (c). This configuration is widely used because it offers a good power flow controllability [102, 103]. In this structure, a low voltage rating UC could be employed due to the indirect connection to the DC link. Moreover, the FC and UC are decoupled from the DC bus so that the input currents can be limited to acceptable levels during rapid transient operation, while sustaining the DC link voltage at the required level even for wide input voltage variations. However, since two converters are used, the overall efficiency may be lower due to the converters losses [91].

In this research, the configuration of Fig.2.28 (c) was investigated for the DC micro-grid system. In order to achieve the best overall performance, it is not only necessary to optimise the performance of each converter, but also the control strategy for the system as will be discussed in later chapters.

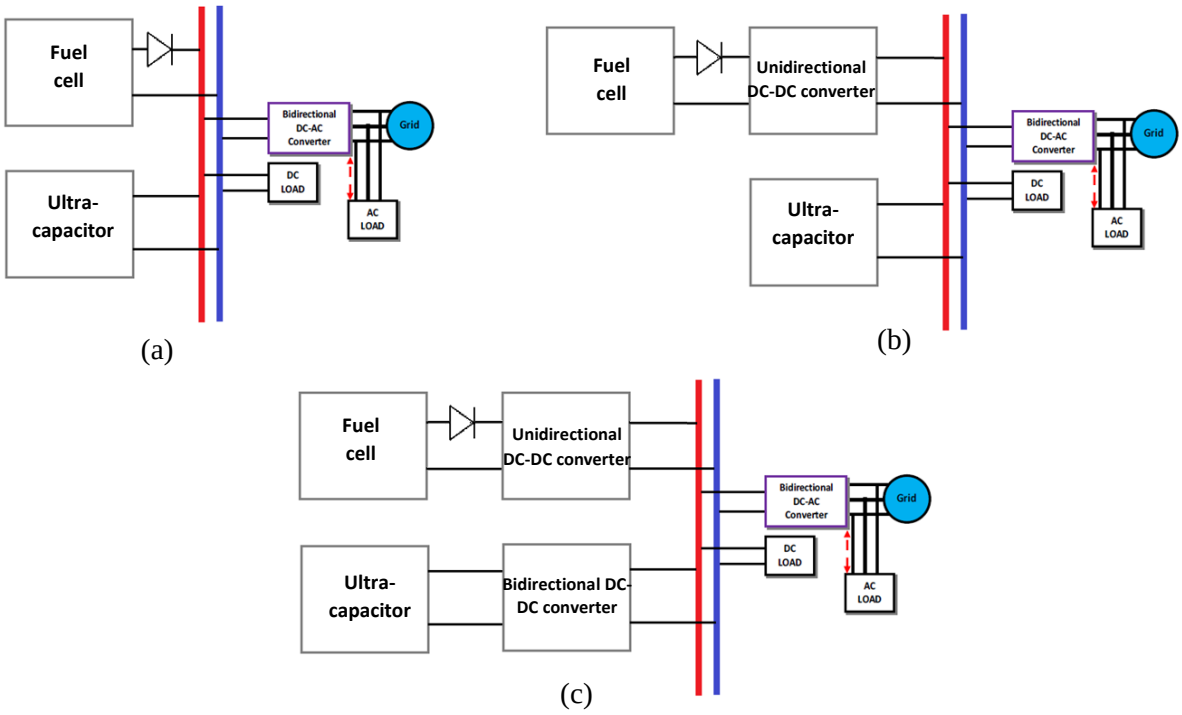


Fig.2.28 Different connection configurations of the FC–UC DC micro-grid: (a) direct connection structure, (b) one-converter connection, and (c) two-converter connection

2.16 Control of DC Bus System

In order to improve the FC-UC performance within the DC micro-grid system, and improve overall system efficiency, the power flow in the micro-grid system should be managed, and a control strategy is therefore needed.

The control strategy should not only manage the power flow between the micro-grid parts in order to maintain the DC bus voltage, but should also control the state of charge (SOC) for the UC. Fig.2.29 shows the most important management requirements that the control strategy should cover.

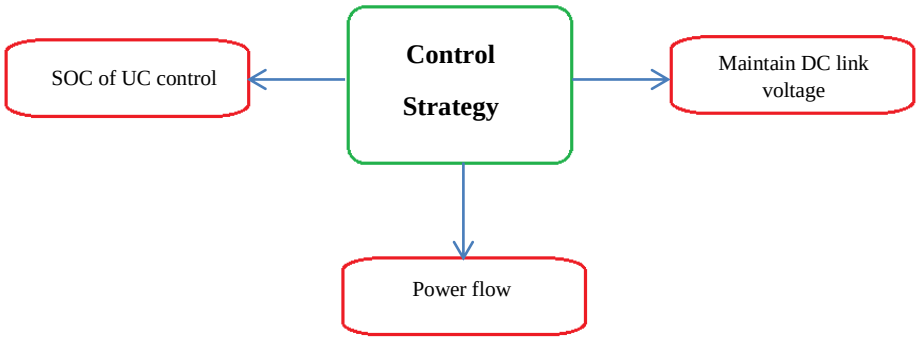


Fig.2.29 BDC control strategy

A number of modes need to be considered for the fuel cell and ultra-capacitor to operate within the dc micro-grid:

- Fuel cell delivers power to the load. When the load demand is within the FCs power range, the fuel cell can supply this amount of power without any assistance thus keeping the efficiency high.
- Fuel cell charges the ultra-capacitor and supplies the load. When the load demands less than the maximum FC power, the fuel cell will still supply the load to maintain high efficiency. Part of the FC's power goes to the load to meet its needs, and the rest of the power charges the ultra-capacitor to maintain the required voltage level of the ultra-capacitor.
- The load demand is suddenly increased, and when this happens, the fuel cell cannot instantly meet the load demand. The Ultra-capacitor releases its power to the load simultaneously with the FC to cover any transient shortfall.
- The load demand is suddenly decreased since fuel cell output cannot be instantly reduced, the ultra-capacitor should be able to absorb any surplus energy within the DC grid system.

A number of control strategies for the power management of a FC-UC hybrid system have been proposed in [92, 107,108, and 109]. Based on the configuration in Fig. 2.28c, an investigation for efficient DC-DC converter topologies with respect to electrical characteristics of the FC and UC is presented. Fig.2.30 shows a control scheme for the FC–UC DC micro-grid. This structure is composed of a unidirectional converter, a bidirectional converter, a FC, an UC, and a closed-loop control circuit. The closed-loop control circuit comprises a fuzzy logic controller (FLC), two inner current loops and an outer voltage loop.

In order for the FC to deliver the steady–state or average power required by the load and the UC, the FC inner current loop was used. The FLC was used to control the SOC of the UC within the allowed operating voltage range and to drive the FC current loop with the required charge current reference. The UC inner current loop was used to limit and control the UC current, and the voltage control loop was used to regulate the DC link voltage. Furthermore, the control module in Fig.2.30 takes into consideration the voltage level of the UC. Hence, the pulse width of the switching regime for the VFC needs to be controlled. For example, if the voltage is low; the switching pulses need to be changed to make longer pulses.

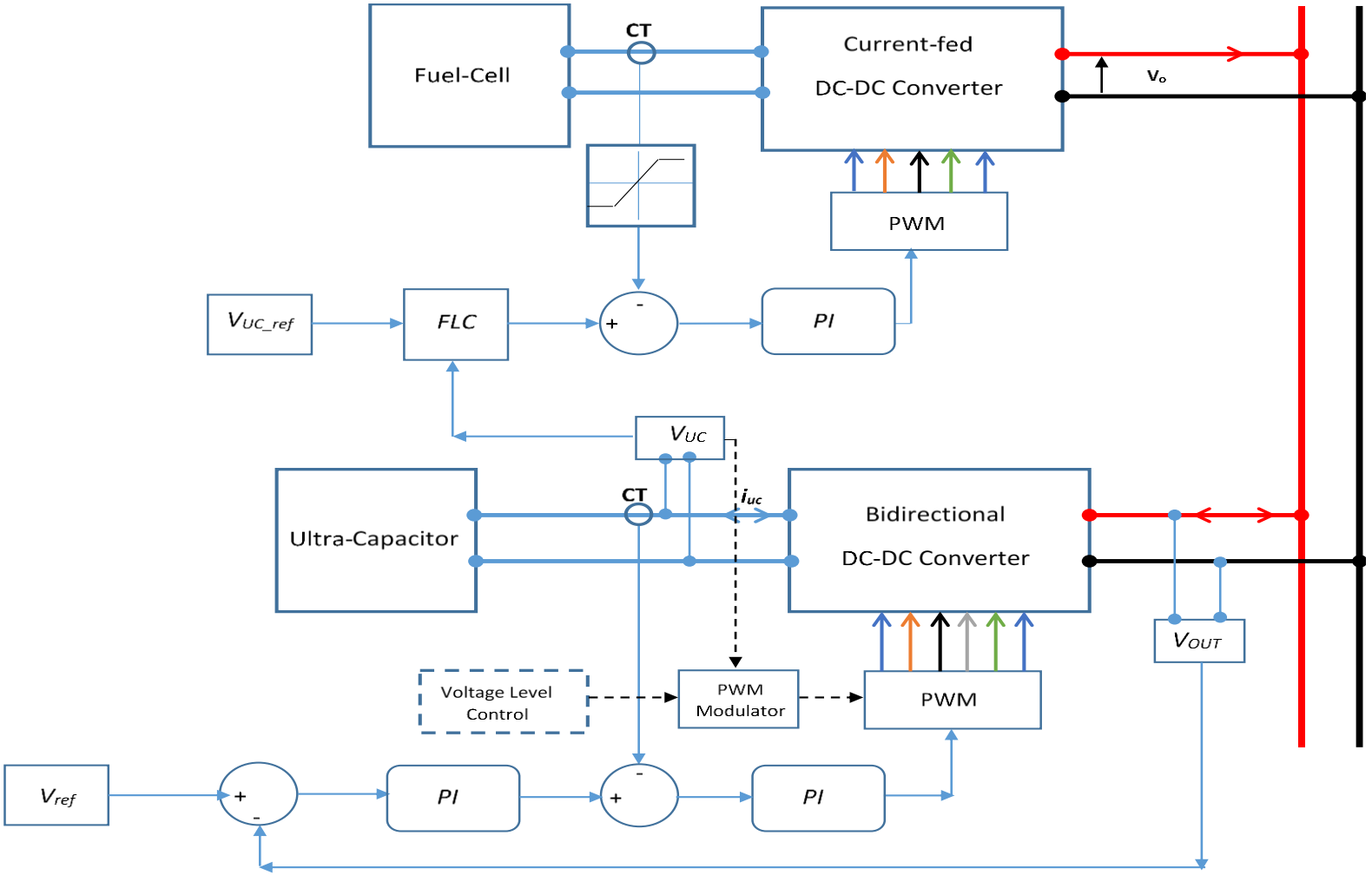


Fig.2.30 Control scheme for the FC–UC DC micro-grid

2.17 Conclusion

The fuel cell that that is fuelled by hydrogen can form the basis of an environmentally friendly electricity generator. However, the output voltage of a FC is typically too low and depends also on the output current; therefore, a DC-DC converter is required to deliver a higher and constant DC output voltage. But as shown in this chapter, the fuel cell has a slow dynamic response to changes in the load due to the mechanical parts within the cell which are used for maintaining the air pressure, the temperature, and the humidity in the cell. To overcome the slow response of the fuel cell and maintain the load voltage, an energy storage device is needed. One of the promising energy storage devices with a fast response is the ultra-capacitor, but this device also requires a DC-DC converter to control the amount of power and its direction. The fuel cell and the ultra-capacitor can then be combined to form a DC micro-grid. In this section a number of topologies for FC-UC hybrid connections have been reviewed and compared, and the most promising topology with respect to the management of power flow was found to be the use of a two-converter topology. A number of DC-DC converters that can be used to interface the fuel cell and the ultra-capacitor to the DC micro-grid have been reviewed in the literature. It has been demonstrated that the unidirectional isolated current–fed DC–DC converter has attractive features for the FC source, while for the UC the bidirectional isolated voltage–fed DC–DC converter with voltage doubling (synchronous) rectifier is the most promising with respect to the achievable converter efficiency and speed of response.

Chapter Three

Chapter Three

Fuel Cell Converter: Design and Implementation

3.1 Introduction

As mentioned in chapter two, fuel cells (FC) have received a lot of attention for being a promising technology in the field of electrical power production. This is due to their ability to provide clean and continuous electricity from primary energy sources. Hence, it helps in reducing the environmental negative impacts caused by the depletion and emissions resulting from fossil fuel power generation. However, a number of issues need to be considered when dealing with FCs. Generally, FCs have a low output voltage that further drops with FC loading and operational life; any output current ripple reduces the FC life time and efficiency [97], and the FC has a relatively slow response to load changes (see chapter four). Also, the FCs must be protected against reverse current flow. Moreover, for applications such as micro-grids and automotive applications a step-up DC/DC or DC/AC converter is required to transform the low and variable output voltage of the FC to a higher and constant level, suitable for the load.

3.2 Role of Power Converters in Fuel Cell Applications

As stated above, an FC requires a step-up DC/DC or DC/AC converter to transform its low and unregulated output voltage to a higher and constant level, suitable for the load. Micro-grids consisting of a dispatchable energy generator (fuel cell or diesel generator) and local energy storage (ultra-capacitor and/or batteries) are also suitable for the integration of intermittent renewable energy sources such as solar PV and wind power. The main requirements for the power converter for FC applications are high efficiency during load operation, a large step-up ratio to boost the FC voltage to the required level, a low input current ripple and galvanic isolation [110, 73]. Boost converter topologies can be classified into isolated and non-isolated configurations [75]. However, non-

isolated converter topologies may not be suitable for a FC converter since a high boost ratio usually incurs an efficiency penalty and there is also a direct connection from the FC terminals to the high voltage output side. Therefore, a DC-DC converter with a high frequency (HF) transformer is generally used to provide not only galvanic isolation from the DC or AC bus bar, but also permits interconnection of DC-DC converters [78].

3.3 Full-Bridge Current-fed Converter Basic Requirements

As mentioned in chapter two, the full bridge current fed converter (FBCFC) with HF transformer and a voltage doubler is the most suitable converter for achieving durability and efficiency of the FC because of its unidirectional, low-ripple input current. The main drawback of the FBCFC is the voltage overshoot across the main bridge devices due to the presence of the leakage inductance of the HF transformer during hard switching operation. The voltage doubler circuit has the additional advantage of reducing the turns ratio of the HF transformer winding and as a consequence it will reduce the transformer leakage inductance. While this will reduce the voltage stress across the devices, it will not entirely eliminate the leakage inductance effect.

In the literature a number of solutions are proposed to reduce the voltage overshoot and reduce the switching losses in the converter's switches as a consequence. This can be achieved by using an RC snubber circuit [111, 112] which may dissipate power and lower the efficiency of the converter. Another solution is the use of devices with a higher voltage rating; however these devices typically have a higher on-state resistance which increases the conduction losses as a consequence.

In this chapter a high efficiency CFC with a high voltage step-up, and low voltage rating of the switching devices, that includes a regenerative clamp circuit [113-124], as originally proposed in [97] and shown in Fig.3.1, is described to overcome the above

drawbacks. This converter will be explained further in this chapter. Furthermore, a modification will be implemented on the regenerative (or active) clamp circuit to improve the performance and the efficiency of the converter.

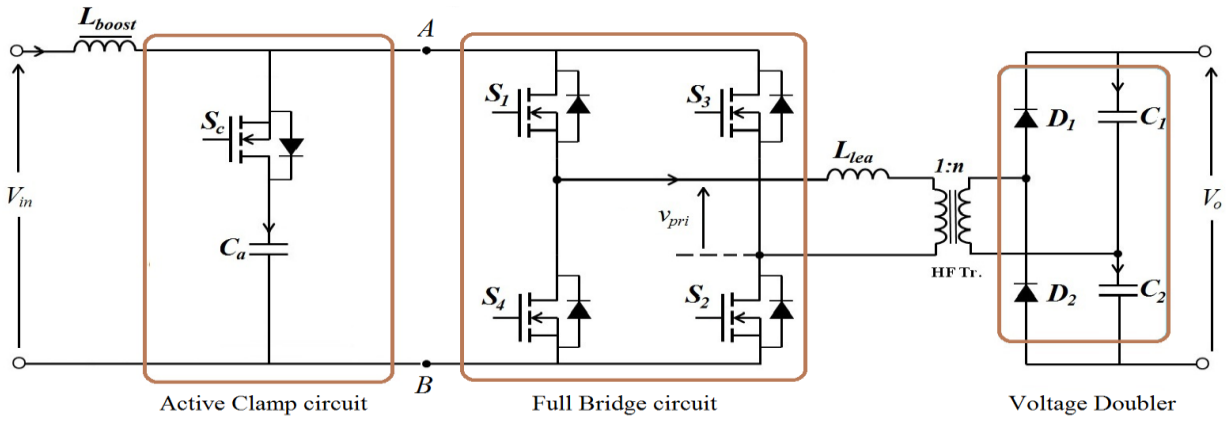


Fig.3.1 FBCFC with a regenerative clamp circuit

The converter has been analysed and implemented based on the 3kW converter prototype with the following specifications: V_{fc} = 42-26V, V_o = 650V, n = 7.4, f_s = 50 kHz, L_{boost} = 475µH, C_1=C_2=500µF, L_σ = L_{lea} = 2 µH, while the FC output power P_o =1.2kW.

One of the most important requirements for this converter when connected with the FC is the operation in continuous current mode (CCM). Overlapping pulses are necessary to ensure CCM. The overlap means that the turn-on period T_{on} is always greater than 50% of the switching time period T_s and the diagonal switches (S_1~S_2 or S_3~S_4 in Fig.3.1) should not all turn off at the same time. In addition, the boost inductor is considered large enough to ensure making the input current (i_{Lboost}) continuous.

In Fig.3.2 the timing of the gates pulses for all switches are illustrated. From this figure, the equations for the overlap pulses can be derived as follows:

$$T_e = \frac{T_{on} - T_{off}}{2} \tag{3.1}$$

$$T_s = T_{on} + T_{off} \tag{3.2}$$

$$D = \frac{T_{on}}{T_s} \tag{3.3}$$

$$(1 - D) = \frac{T_{off}}{T_s} \tag{3.4}$$

$$D = \frac{T_e}{T_s} + 0.5 \tag{3.5}$$

Where T_e is the overlap time for the bridge diagonal switches that keeps sufficient energy stored in the boost inductor so that the converter is capable of stepping-up the FC voltage to the required level, T_s is the switching period, T_{on} is the turn-on time, T_{off} is the turn-off time, and D is the duty ratio (for CCM D must range between 50% and 100%).

Due to the presence of the voltage-doubling rectifier, the converter's voltage conversion ratio (M) is equal to:

$$M = \frac{V_O}{V_{fc}} = \frac{2n}{(1-D)} \tag{3.6}$$

Where M is the conversion ratio, V_o is the output voltage, V_{fc} is the input voltage, and n is the transformer turns ratio.

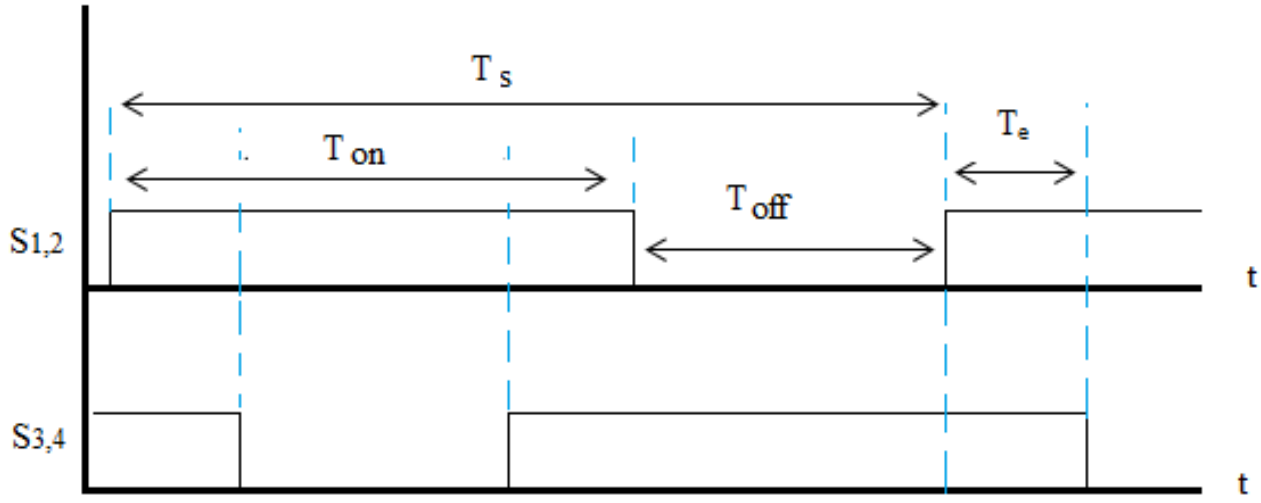


Fig. 3.2 Overlapping timing pulses

3.4 Isolated FBCFC Modelling and Software Implementation

In this section, the PSpice simulation package was used for power electronics simulation. PSpice has the advantages of using detailed component models which are often supplied by the manufactures. Hence, PSpice is considered as the best tool for power electronics simulations. The isolated FBCFC with a voltage doubler that was designed and implemented in [97] to meet the requirements of the FC has been modelled using PSpice. In order to study the converter model in detail, the FBCFC was simulated first using ideal components as shown in Fig.3.3.

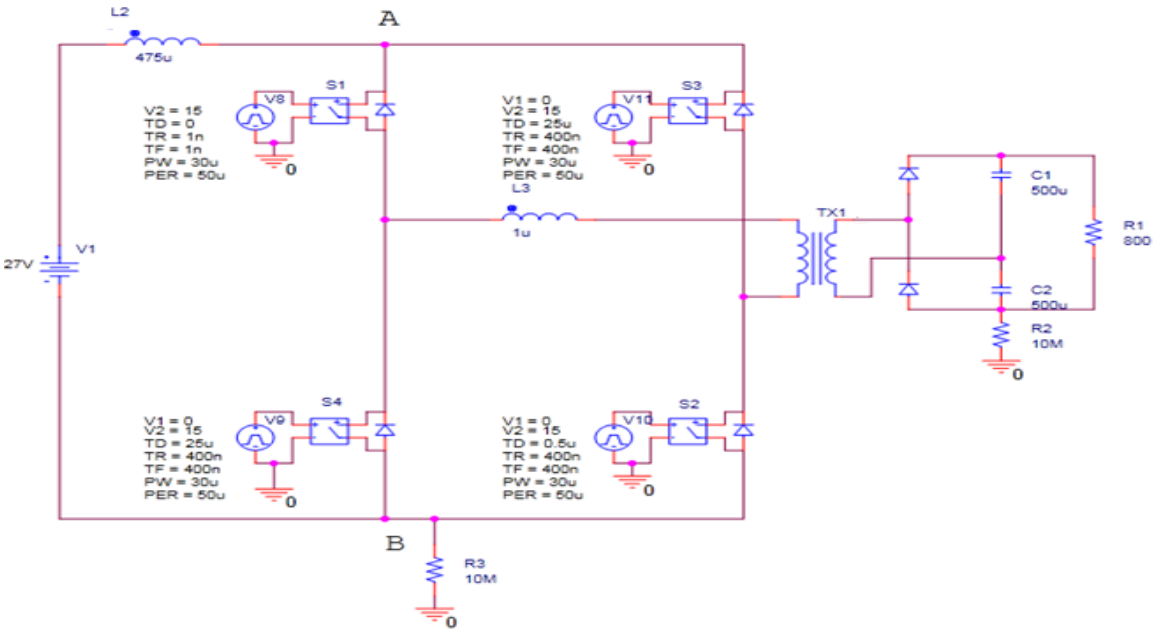


Fig. 3.3 FBCFC model using ideal components

These ideal switches have the following properties: Infinite breakdown voltage. When it is off there is zero current through the switch, when switch is on, there is zero voltage across the switch. It has no internal resistance, and the turn-on and turn-off transition times of ideal switches are zero; since either the voltage or the current is always zero in an ideal switch, the instantaneous dissipation which is the product of instantaneous voltage and instantaneous current is always zero. In contrast to a simulation with the non-ideal switches, the execution of the simulation time is much faster.

These operational modes of the circuit are explained below: during each mode, two of the bridge diagonal switches (S_1S_2 & S_3S_4) are turned on and off at the same time. Adding to that, during the overlap period all the diagonal switches are turned on. The overlap is needed to ensure the continuous conduction mode (CCM) operation.

Fig.3.4 shows a set of output waveforms for the circuit of Fig. 3.3. The operational modes for this circuit can be divided as follows:

(i) When two of the bridge diagonal switches are turned on, and the other two switches are turned off.

(ii) When all switches are turned on (the overlap period) [The circuit has two overlap times during the full cycle].

When two of the bridge diagonal switches are turned on, the boost inductor will be connected to the transformer primary winding (which has a leakage inductance), and the power will transfer to the load through the secondary winding. The boost current will decrease linearly. As can be seen from Fig.3.4, the voltage across the active switches when on is zero, and the switch current is equal to the boost inductor current. At the same time, the voltage across the inactive switches is equal to V_{prim}, and the switch current is zero. As can be seen from Fig.3.4 high voltage spikes (more than 1 kV) appear across the switches when they are turned off, which is due to the energy released by the leakage inductance during the off-state. Those spikes are one of the major problems of the FBCFC. As will be discussed later, this can be resolved by adding an active clamp circuit to eliminate the voltage overshoot across the switches.

When all the diagonal switches are turned on, the boost current will build up linearly, and current due to the leakage inductance will also circulate through the switches which will incur additional losses.

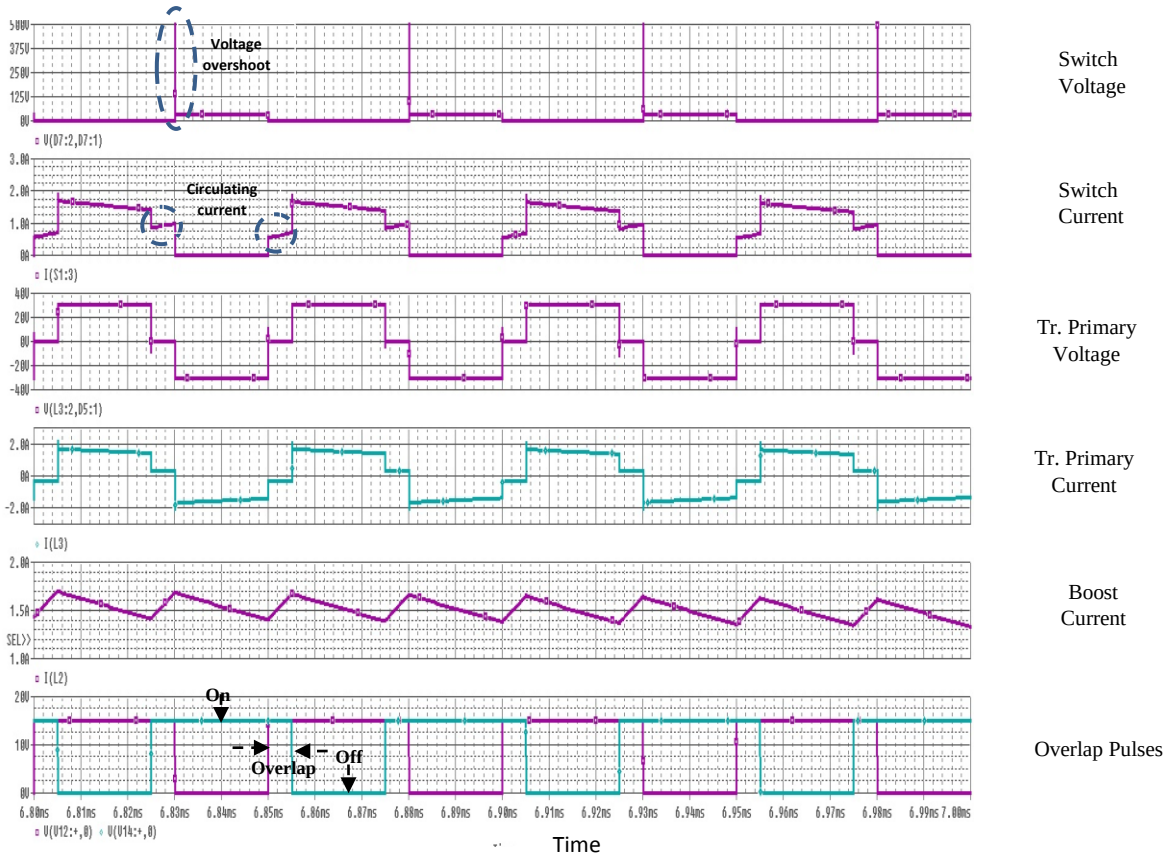


Fig.3.4 Output waveforms of the circuit of Fig. 3.3. From the top: voltage across the switches, switches current, transformer primary voltage, transformer primary current, boost inductor current, and overlap pulses

It can be seen from Fig3.4, both the transformer voltage and current are almost rectangular simultaneously. This means that the power flow is always unidirectional, and no reverse power flow occurs through the transformer. This results in a high efficiency for this converter.

3.5 Full Bridge CFC Using Non-Ideal Switches

Simulating ideal circuit components does not give the complete picture. Components in the real world are not ideal; they contain parasitic components. Fig. 3.5 shows the isolated FBCFC model in PSpice using non-ideal components.

Practical switches will have parasitic elements which cause a leakage current in the off-state, non-zero voltage across the switch in the on-state, and non-zero turn-on and turn-

off transition times. The voltage across the switch during the on-state and the non-zero transition times result in dissipation in the switches which must be managed.

As it can be seen in both the simulation and the practical validation results, the parasitic elements have an impact on the converter performance. The most important parasitic elements that effect the converter performance are the stray inductances of the switching devices, the drain-source capacitance of the MOSFETs, the stray capacitances of the boost inductor and transformer, and the parasitic capacitance of the rectifier diodes [97]. Fig.3.5 shows the simulation scheme of the FBCFC with the practical components[1] which includes the leakage inductance of the HF transformer.

In the simulation circuit of Fig.3.5, the turns ratio of the transformer was chosen according to the original data sheet of the transformer [see Appendix A] (the number of secondary winding turns was later reduced from 43 to 37 turn). Furthermore, the circuit of Fig.3.5 was simulated with the input voltage V_1=13V, and output voltage V_{10}=220V. These values were chosen in order to compare the results of the PSpice model with the practical circuit when tested without an active clamp circuit in order to limit the voltage overshoot that might otherwise damage the MOSFETs power switches of the real converter circuit as will be explained later.

[1] Using the datasheets of the clamp switch (IXFN73N30) and the bridge switches (SKM120B020) the parasitic elements of the practical parameters of Fig.3.1 can be obtained.

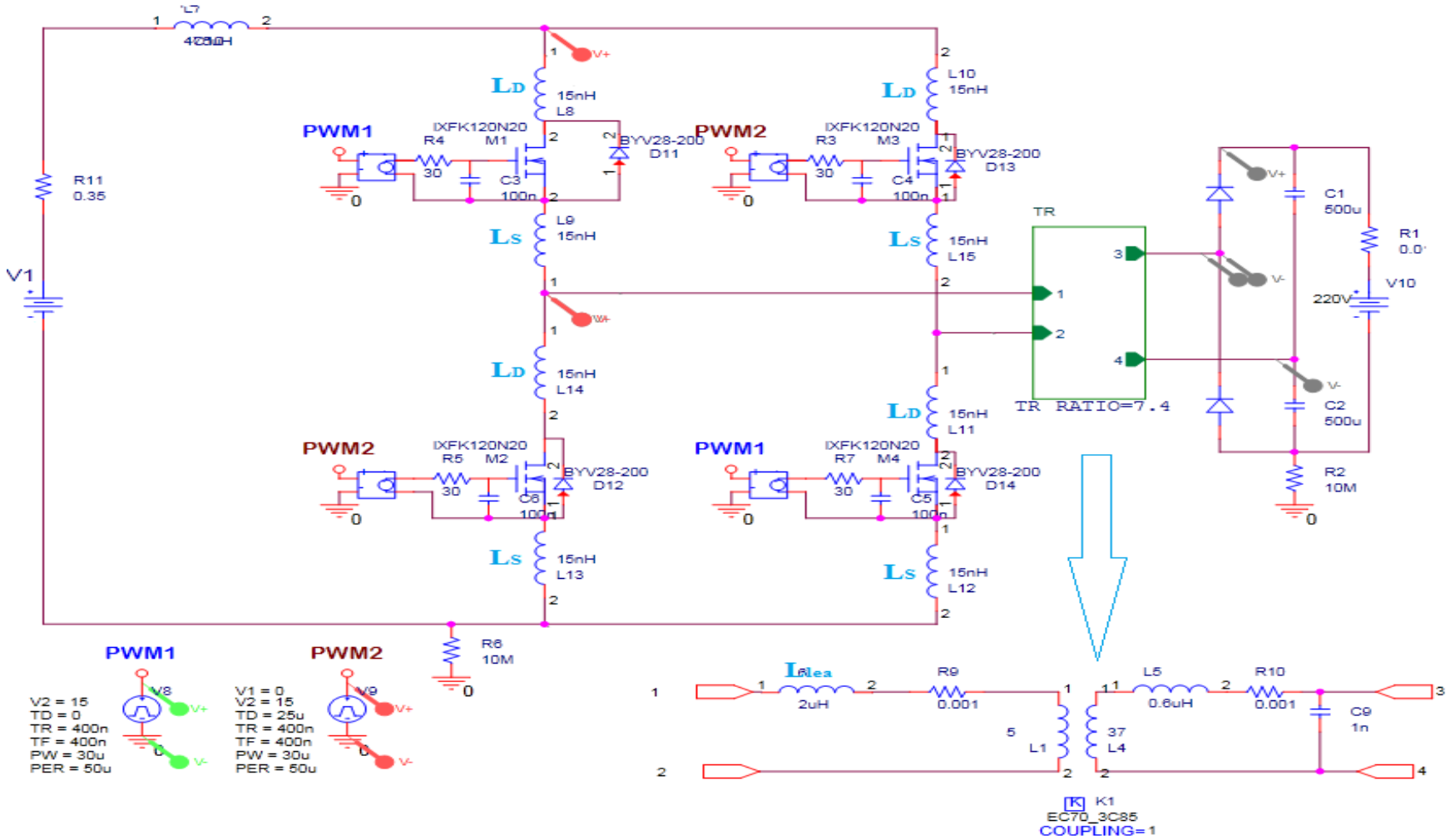


Fig. 3.5 The FBCFC model in PSPICE using non-ideal components

The resulting waveforms of the simulation including the parasitic elements are shown in Fig.3.6 for the transformer and switch voltages.

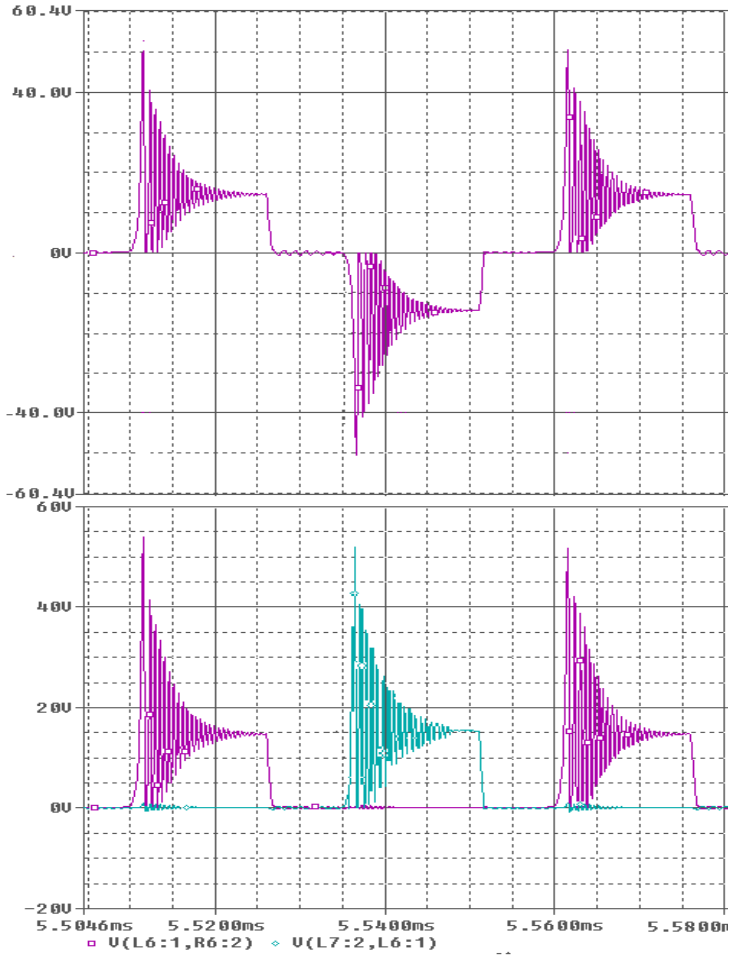


Fig.3.6 From the top: primary winding voltage, and voltages across the switches with super imposed ringing; frequency approx. 1.75 MHz

It can be seen from Fig.3.6 above, that a voltage ringing (approximately 1.75 MHz) is imposed across the bridge switches due to the effect of the parasitic circuit elements [125]. Additionally, when one pair of diagonal bridge switches of the FBCFC circuit in Fig3.5 is turned off, the input current (boost inductor current) tries to commutate to the transformer primary, which leads to a rapid rise in the voltage across the bridge (voltage overshoot) due to the presence of the transformer leakage inductance. Fig.3.7 shows both the voltage and the current of one of the diagonal switches during the on/off state

transition. The figure illustrates the voltage overshoot occurring across the switches due to the leakage inductance and the parasitic elements effect of the converter low voltage side [125]. As a result of this, the converter losses will be increased.

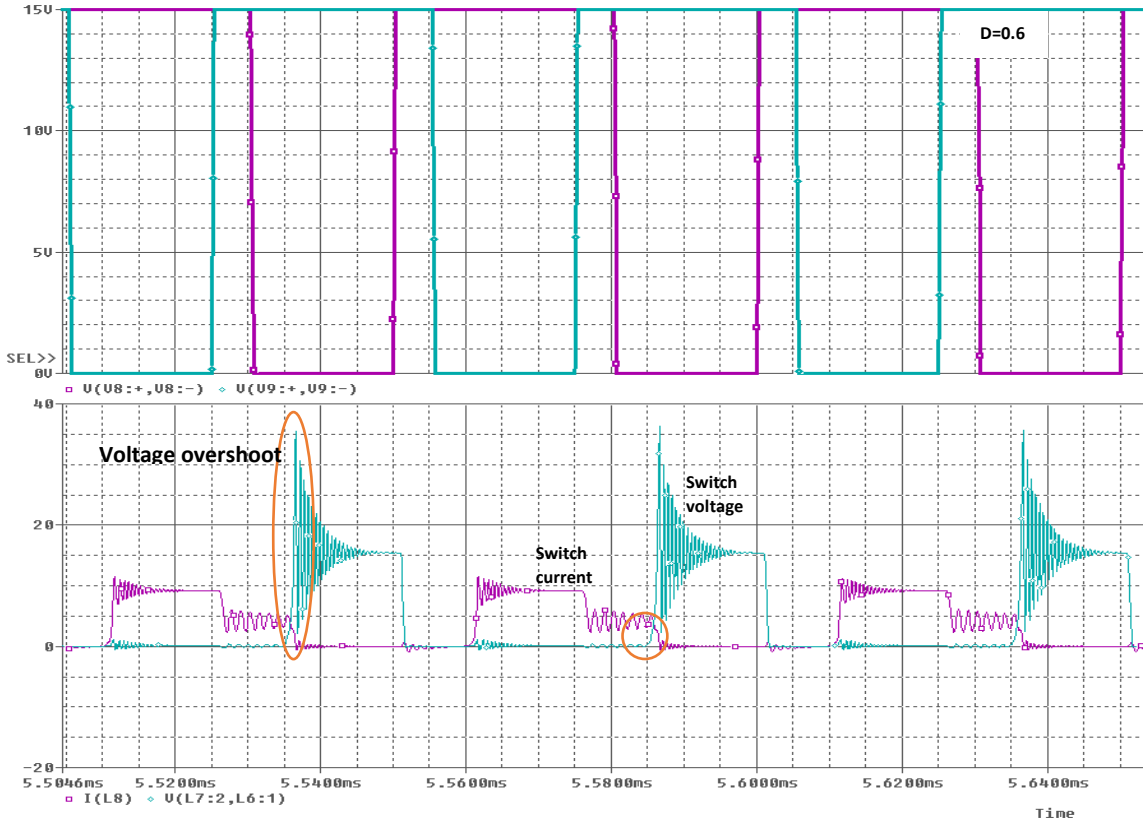


Fig.3.7 From the top: the overlap pulses with a duty ratio of 0.6, the voltage and the current of one bridge switch

Fig3.8 shows the voltage across the rectifier diode and the secondary voltage. It can be seen that a damped resonanance (approximatly 2MHz) occurs during the overlap period across the secondary winding and the rectifier diode due to the resonant circuit of the high voltage side [97].

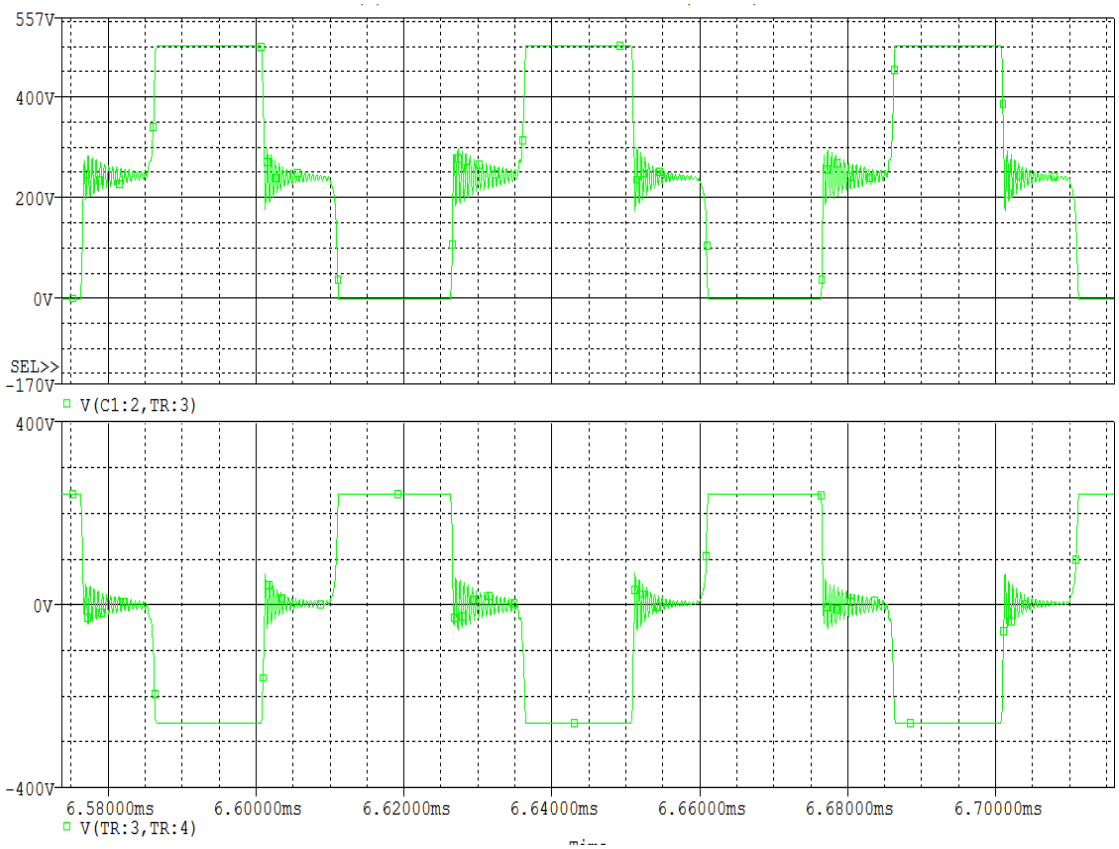
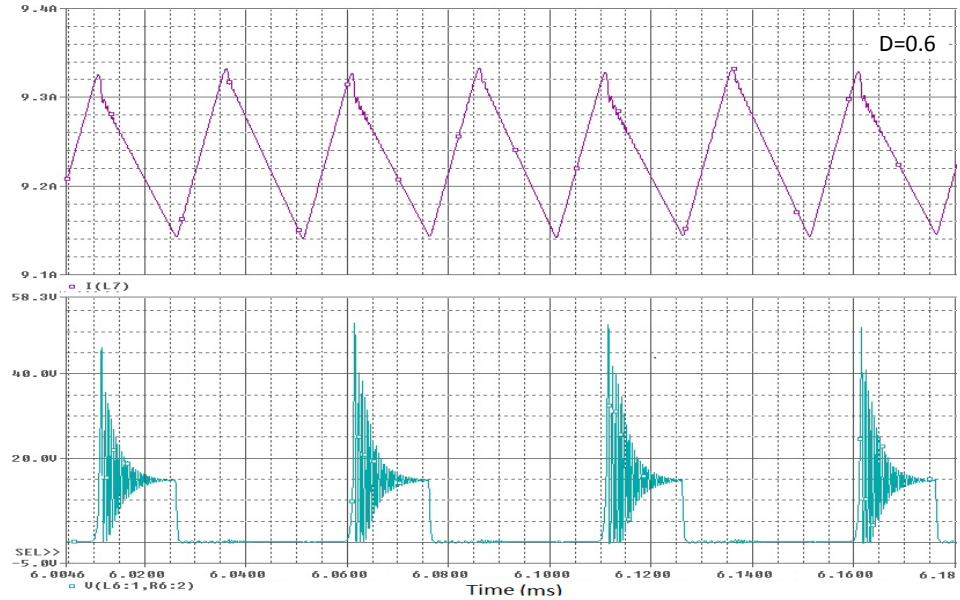
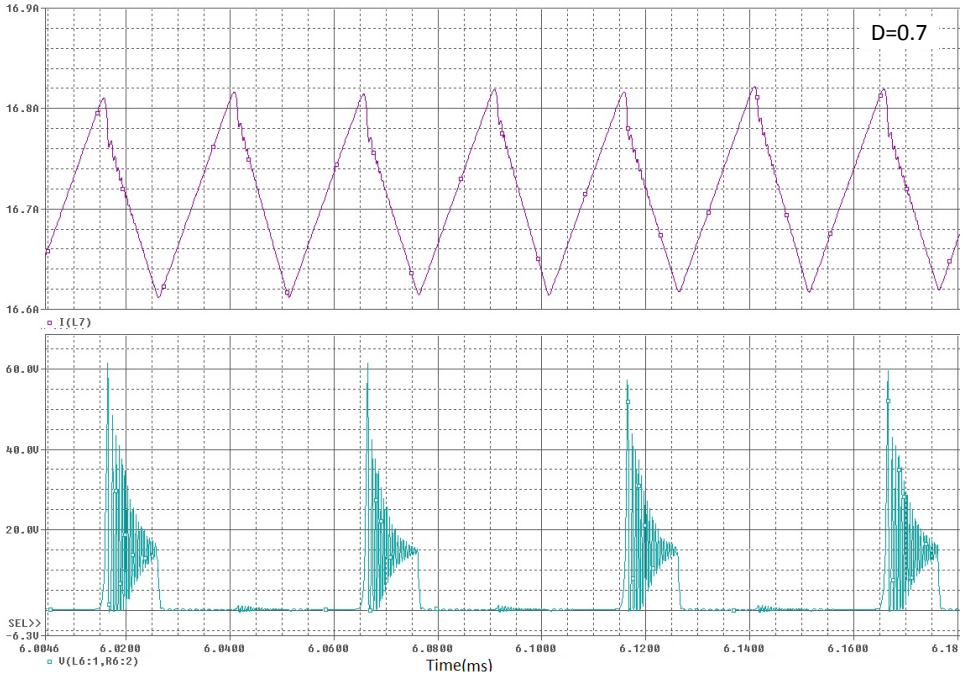


Fig3.8 From the top the voltage across the rectifier diode, and the secondary voltage

Fig.3.9 shows the boost inductor current and the voltage across the main switches for different duty ratios (D). When the value of D is changed from 0.6 to 0.7, the voltage overshoot is increased from approx. 50V to more than 60V. In the PSpice model the duty ratio can be changed to any value and the circuit can be simulated for higher input and output voltages; in the practical test D can not be varied to values that would increase the voltage overshoot, and the converter could not be tested for higher input voltages due to the increase of the voltage overshoot of the switches. The voltage overshoot should be clamped, and one solution is the use of the active clamp circuit as will explained in section 3.6.



(a)



(b)

Fig3.9 From the top the boost inductor current, and the voltage across one of the diagonal switches with: (a) D=0.6, (b) D=0.7

As can be seen from the results above (Fig.3.7 to Fig.3.9), the leakage inductance of the transformer causes a transient effect during the overlap period that could lead to overvoltage and noise which could damage the switching devices of the converter and increasing the losses. Of course, switching devices with a higher voltage rating could be used. However, this would increase the losses and decrease the efficiency of the converter

due to the higher on-state resistance R_{ds} of the MOSFET devices with a high voltage rating, reducing the efficiency of the converter. In order to reduce the voltage overshoot, an active clamp circuit has been added as will be shown in the next section.

3.6 Full Bridge CFC with an Active Clamp Circuit

As can be seen from Fig.3.6, due to the leakage inductance presence of the HF transformer, a voltage overshoots occur across the switches during the turn-off period which will increase the component stress and the losses in the circuit. In order to overcome this problem, an active clamp circuit has been added to the FBCFC circuit. Fig.3.10 shows the FBCFC with active clamp circuit as modelled in PSpice.

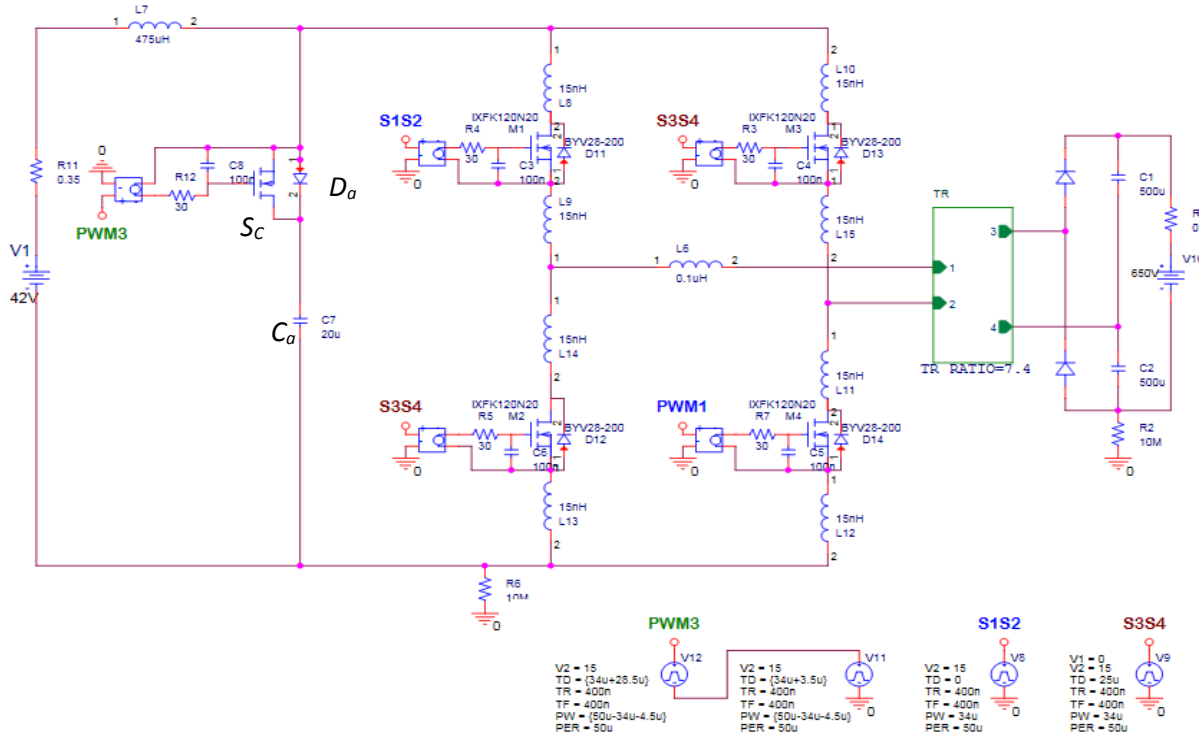


Fig.3.10 the FBCFC with active clamp circuit using PSpice

The active clamp circuit or, termed hereby the conventional active clamp circuit (CACC), is connected across the bridge to clamp the voltage and avoid high voltage stresses across the switches as shown in Fig3.10. The CACC is composed of a MOSFET switch S_c (with

anti-parallel diode), connected in series with a capacitor C_a. The capacitor of the ACC initially absorbs the current in the boost inductor L_{boost} through the diode, and this energy is subsequently released to the load through the MOSFET switch and the bridge switches. The timing of the active clamp pulse should be chosen with a dead-band time between the turn-off time of the diagonal switches and the overlap time. However, this returned current affects the shape of the current in the bridge switches, increasing its rms value and leading to additional losses and reduced efficiency. The waveforms of the gate pulses for the bridge and clamp switches, the primary voltage and current, and the capacitor current, were obtained from a simulation model of the FBCFC with a CACC in PSpice, and are shown in Fig. 3.11.

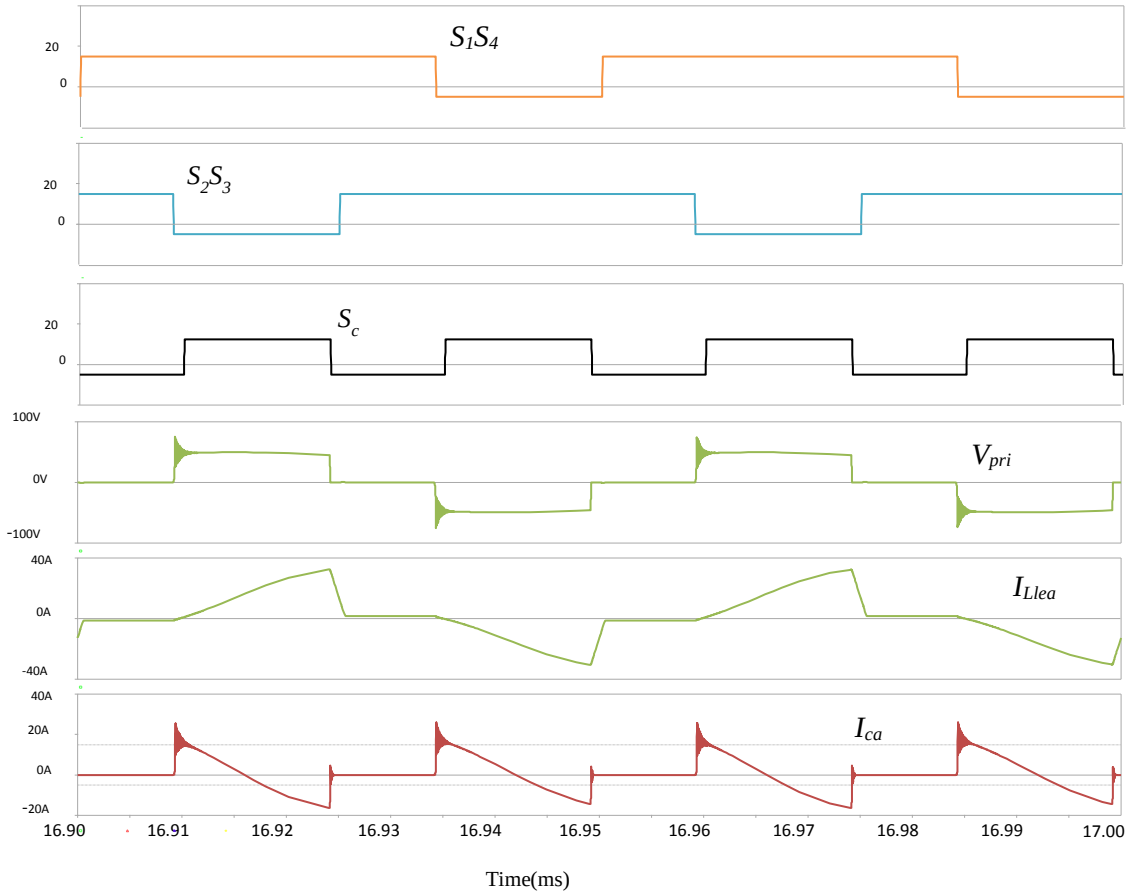


Fig. 3.11. Simulation result of the FBCFC circuit combined with CACC; from the top: the gate pulses, the primary winding voltage and current, and the clamp capacitor current

From the waveforms it can be seen that the voltage overshoot is considerably reduced, but due to the current returned from the clamp capacitor the shape of the primary transformer current has changed from a rectangular to a sawtooth form, which results in a higher rms value, leading to additional losses in the bridge and the transformer.

3.7 First Experimental Validation of the Active Clamp Circuit

In order to study and test the existing prototype FBCFC, a generator circuit for producing overlapping pulses for the bridge at 20 kHz switching frequency was designed using PSpice, which was then implemented in the lab on a breadboard. This circuit is considered as a conventional method to drive the MOSFET switches. Fig.3.12 shows the circuit block diagram. The output pulses of this circuit are applied to the MOSFET driver (SKHI 22BH4), which in turn will generate the appropriate pulses that are capable of turning on and off the MOSFETs. The circuit was implemented using an LM311 comparator and 8×dual D-flip flop IC chip (7474) which gave the required overlap delay [See Appendix B for a full circuit diagram]. Fig.3.13 shows a photograph of the test circuit with the FBCFC. The LM311 comparator is used to compare between the DC voltage (E_C), and the 20 kHz offset triangular wave. The result is a series of 20 kHz (50 µsec) pulses (OUT1) as shown in Fig.3.12, and the duty ratio of the pulses can be controlled by changing the value of E_C. A screen capture in Fig.3.14 (a) shows both the triangular wave and the LM311 comparator output (OUT1), and Fig.3.14 (b) shows the full pulses that were applied to the MOSFETs drivers. Fig.3.15 shows a screen capture of the output of the MOSFET drivers.

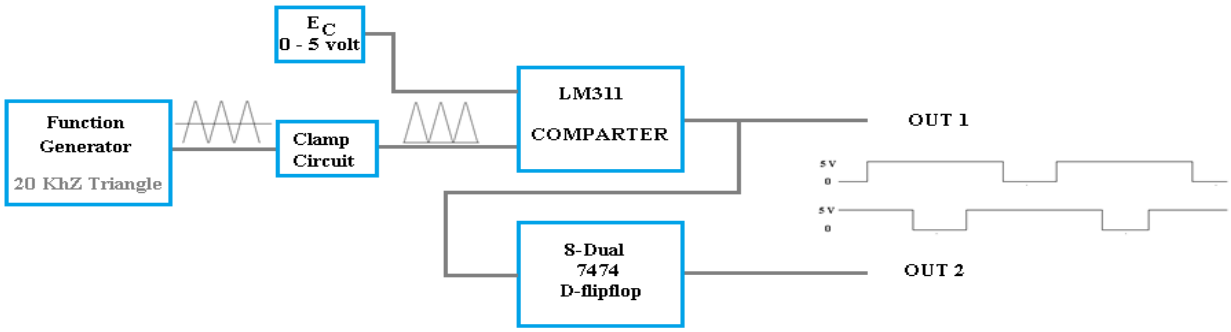


Fig.3.12 Block diagram for creating overlapping pulses

However, as can be seen from both Fig.3.14 (a) and Fig.3.15 (a) there is some uncertainty (jitter) in the output of the D flip-flops. This jitter is due to a difference in clock signal arrival times across the chip and is caused by clock skew, and it is a fundamental design principle that timing must satisfy register setup and hold time requirement. This problem was solved by adding an extra buffer in the path of the D flip-flops clock. Fig.3.15 (b) shows the overlap pulses without jitter after adding the buffer.

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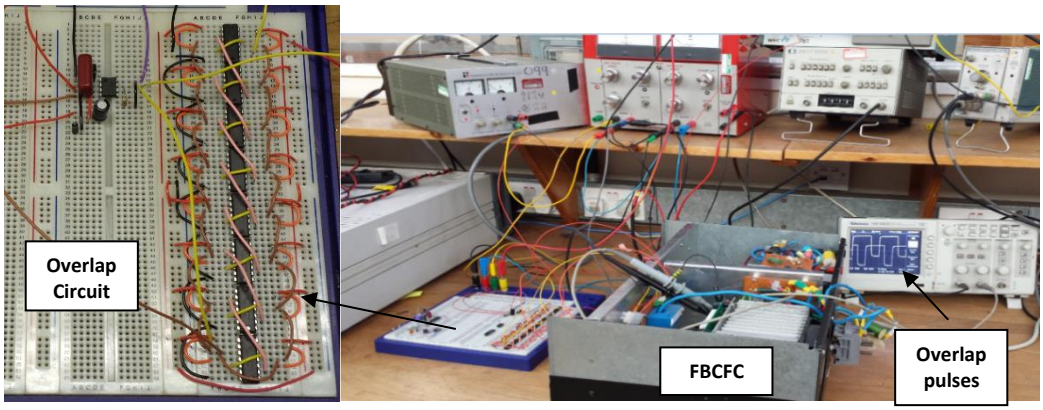
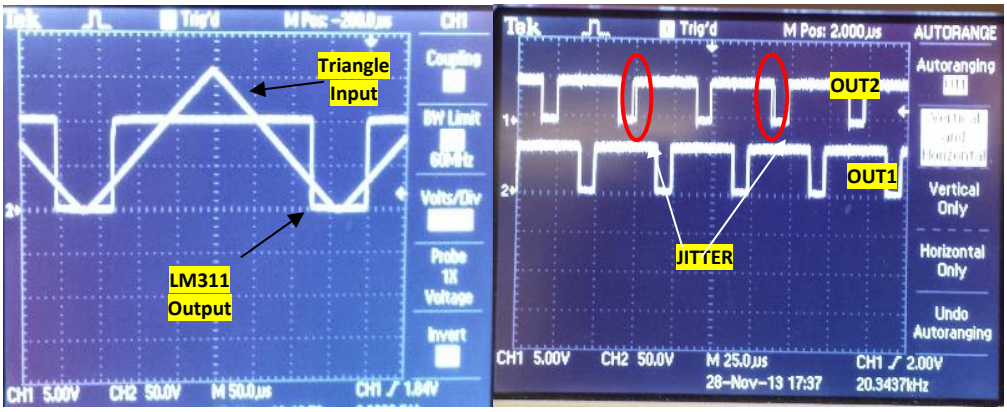
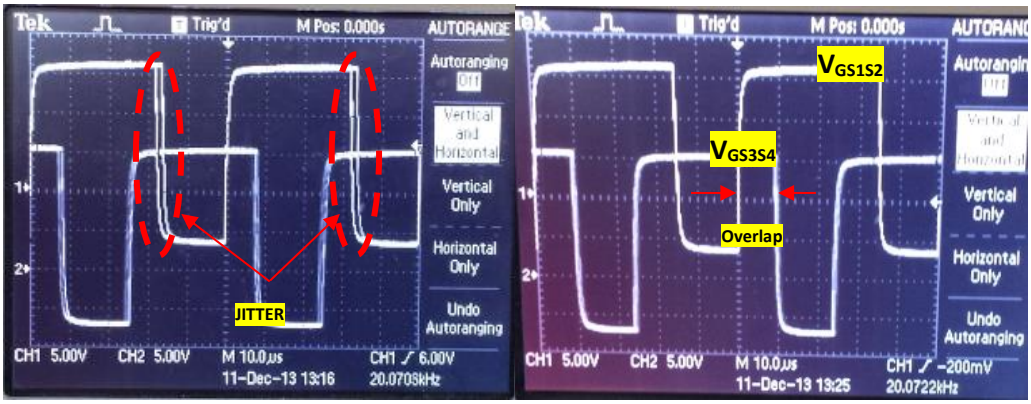


Fig.3.13 Photograph of overlap pulses circuit test on the FBCFC



(a) (b)

Fig.3.14 (a) LM311 Input/Output, (b) Overlap circuit outputs



(a) (b)

Fig.3.15 (a) overlap pulses with the jitter problem, (b) Overlap pulses without jitter

However, the conventional designed drive circuit in Fig.3.12 was only aimed to test and prepare the existing converter and its parts to be used in this research. In order to control the FBCFC and build a closed loop controller, and to control both the FC and UC system within the DC micro-grid, the dSPACE (digital signal processing and control engineering) kit was used.

3.8 dSPACE Implementation

Among the real-time systems available, dSPACE is one of the most practical to use because of its strong ties with Matlab-Simulink. In fact, the dSPACE system is very easy to integrate in Simulink and the generation of the code for its processor can be started directly in Matlab. The dSPACE system has a wide range of different hardware. The

hardware is composed from several real-time processors mounted on a PC board and a large choice of input/output boards. For the supported hardware dSPACE offers a toolbox for Simulink with the optimized drivers. dSPACE was chosen to generate the required pulses needed to drive the converter circuit including the active clamp pulses thus optimizing the time and the equipment that was used in generating the overlap pulses in the circuit of Fig.3.13. Additionally, dSPACE has the power and the ability to control more than one system. Hence, it will be used in designing and building the controller of the complete FC-UC DC micro-grid system.

Fig.3.16 shows a model in Matlab using a DS1103SL_DSP_PWM3 block to produce the required pulses to drive the power switches of the converter circuit including the active clamp. This block is a 3 phase PWM generator, with an ability to control the duty ratio of each generated pulse (duty cycle a, duty cycle b, duty cycle c). Duty cycle c was not used so it is connected to zero to be terminated. Furthermore, the frequency of the overlapping pulses could be selected with a range from 1.25 Hz to 5 MHz as shown in Fig3.16. The information of the I/O slave (CP31) real time interfacing (RTI) pin outs for this block are shown in Fig.3.17, and Fig.3.18 illustrates the full bridge pulses including the clamp switch pulses generated using the circuit of Fig.3.16. Pin 8 and pin 26 output the overlapping pulses for S_1S_2 and S_3S_4 respectively, while pin 27 with pin 7 are connected to the input of an external OR gate to produce the active clamp pulses. A setup was made as shown in Fig.3.16 to control the overall duty ratio of the pulses, while the dead-band time of the active clamp pulses is controlled by the value of the required dead-band time in the DS1103SL_DSP_PWM3 block that can be set to any value between 0 and 100 µs.

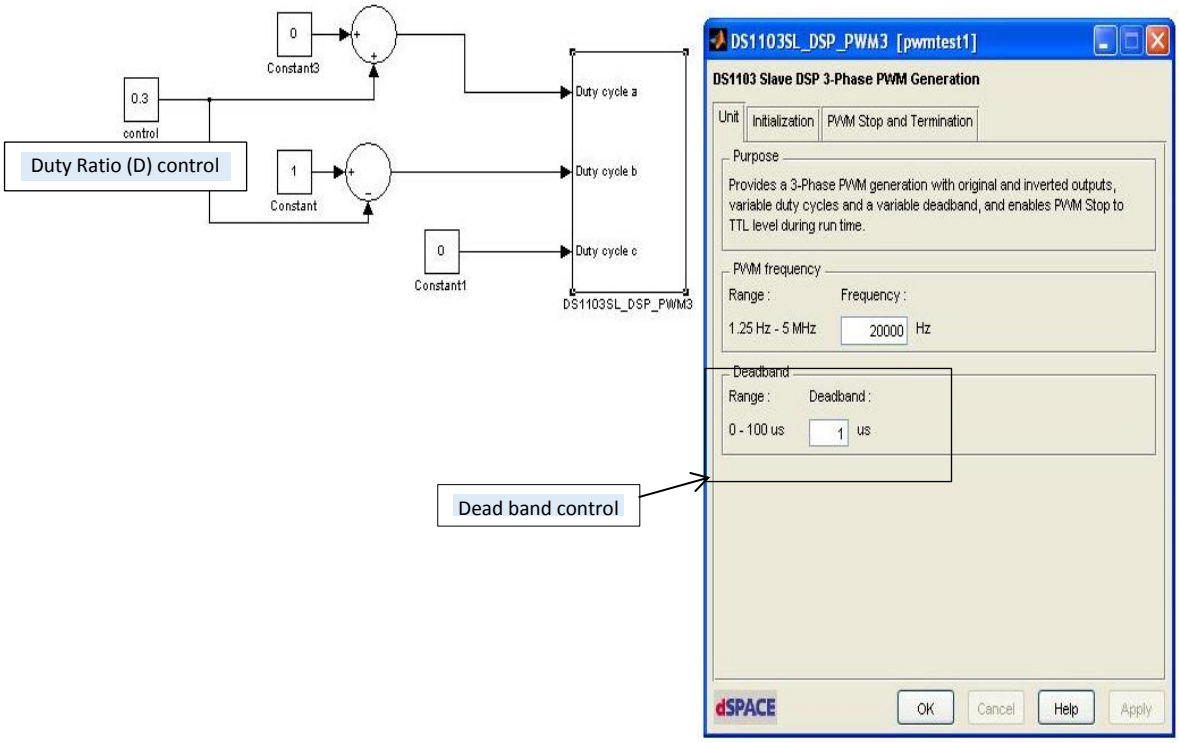


Fig.3.16 Bridge & active clamp pulses design using DS1103SL_DSP_PWM3 block

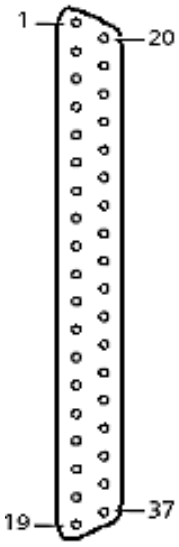
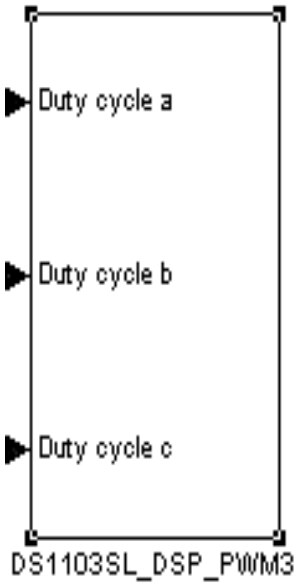
Slave I/O Connector (CP31)	Pin Number	signal	Pin Number	signal	Matlab Block
	1	GND			
	2	SCAP1	20	GND	
	3	SCAP3	21	SCAP2	
	4	GND	22	SCAP4	
	5	ST2PWM	23	ST1PWM	
	6	GND	24	ST3PWM	
	7	SPWM1	25	GND	
	8	SPWM3	26	SPWM2	
	9	SPWM5	27	SPWM4	
	10	SPWM7	28	SPWM6	
	11	SPWM9	29	SPWM8	
	12	STMRCLK	30	GND	
	13	GND	31	STMRDIR	
	14	STINT1	32	SPDPINT	
	15	GND	33	STINT2	
	16	SSIM	34	SSOMI	
	17	SCLK	35	SSTE	
	18	SXF	36	SBIO	
	19	VCC(+5V)	37	GND	

Fig.3.17 I/O salve CP31 pins configuration

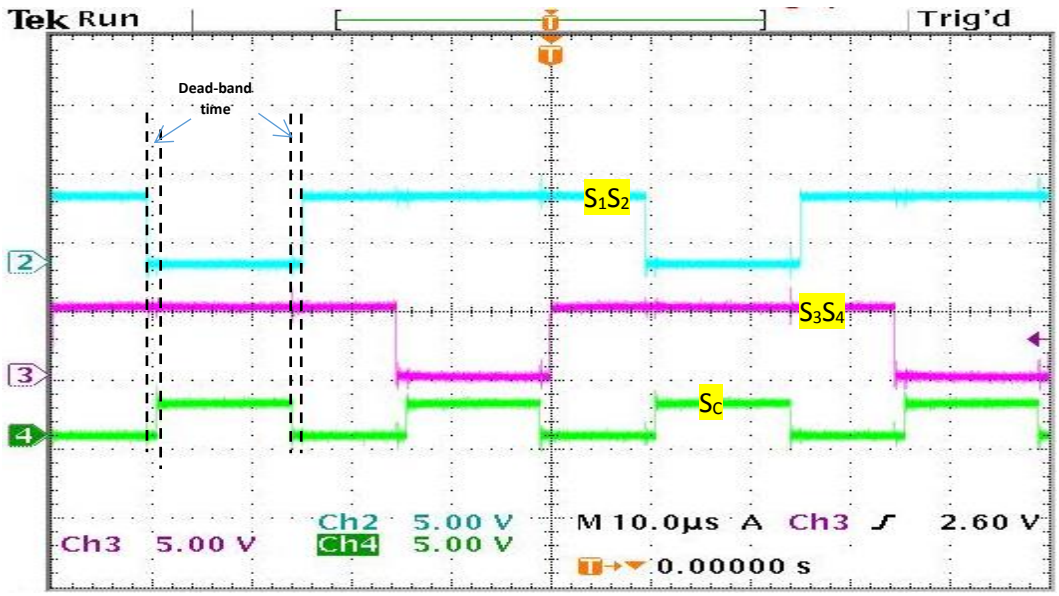


Fig.3.18 Overlap PWM signals for the bridge and clamp switches using dSPACE

The dSPACE kit offers the ControlDesk software which is installed on the dSPACE PC and has the ability to control the real time implementation outputs of the dSPACE. Fig.3.19 shows the ControlDesk layout with system running, a slider and a knob used to change the Duty Cycle of the generated pulses of Fig.3.18. The designed model in Matlab can be opened in the ControlDesk layout. The ControlDesk software has the ability to monitor, and control any part from the Matlab model. In order to control the duty ratio, the control block should be dragged to the knob block or to the slider as shown in Fig3.19. To monitor the value of the duty ratio a display block was used, and the plotter could be used to display any waveforms or signals that are generated in the Matlab model. The control desk windows contain three important modes: the edit mode, the test mode and the animation mode as shown in Fig.3.19. To use the instruments to control and monitor the actually running real-time system, the "Animation Mode" should be selected.

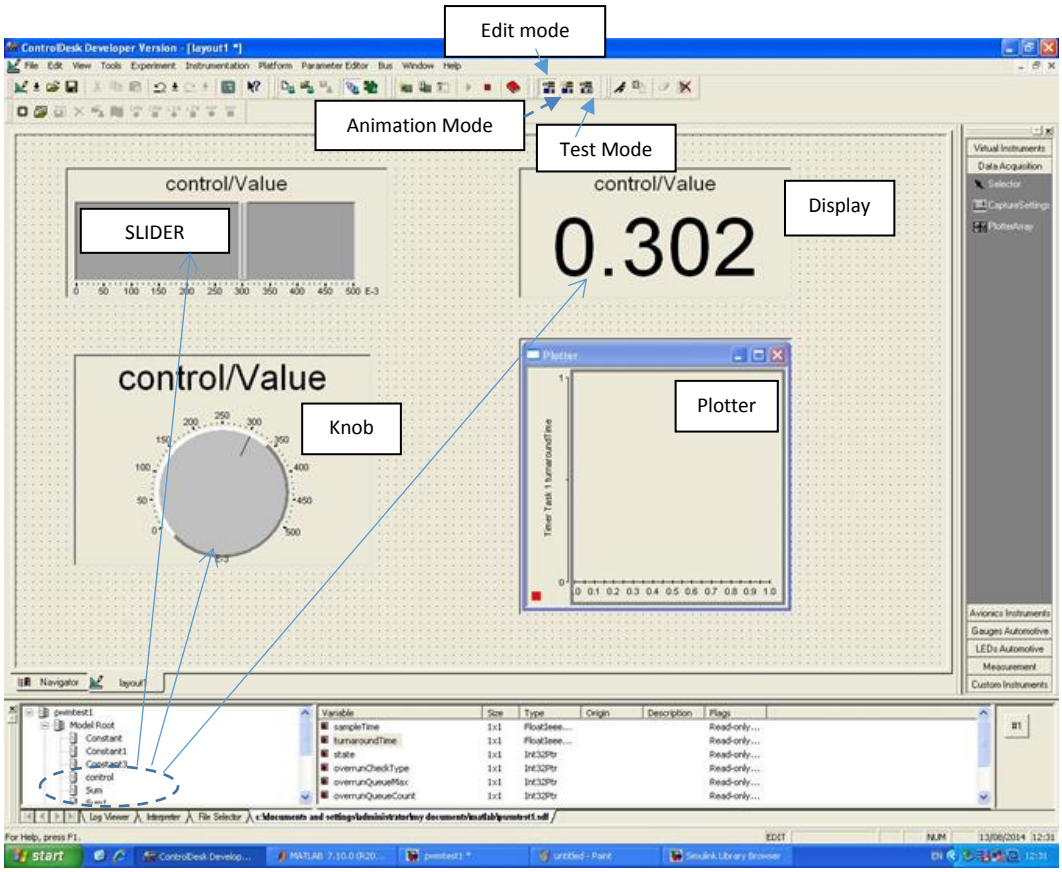


Fig. 3.19 Layout in ControlDesk with system running and slider and knob used to change the Duty Cycle

3.9 FBCFC Experimentation Setup

The FBCFC circuit was tested firstly by using the pulses of the hardware circuit in section 3.7 as shown in Fig.3.20. The tests were initially done without the active clamp circuit. Then the test was done using the dSPACE kit, and the active clamp circuit was included using the pulses of Fig.3.18. Fig.3.20 shows a block diagram of the FBCFC setup and Fig.3.21 shows a photograph of the 1.2 kW power converter. The position of the bridge switches was changed from the original arrangement for easier access for measurements. The test was done for two values of input voltage (13V and 27V) using an 800Ω rheostat load.

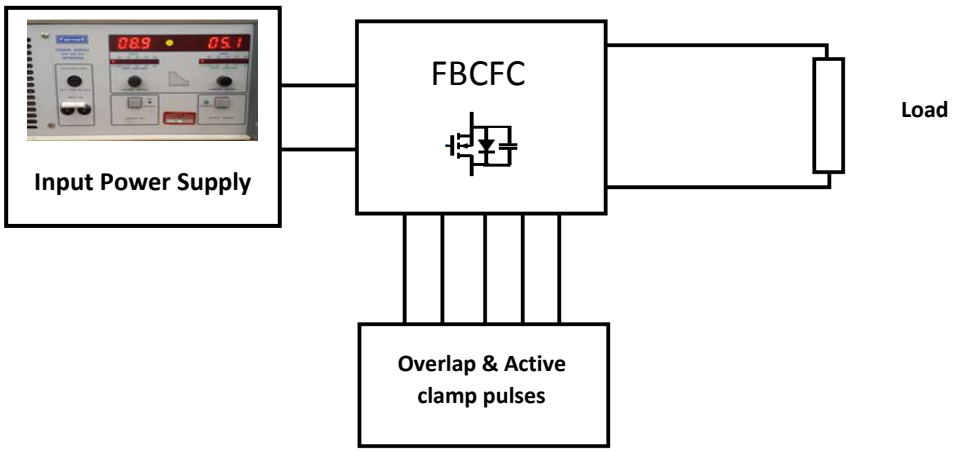


Fig. 3.20 A block diagram of the FBCFC setup

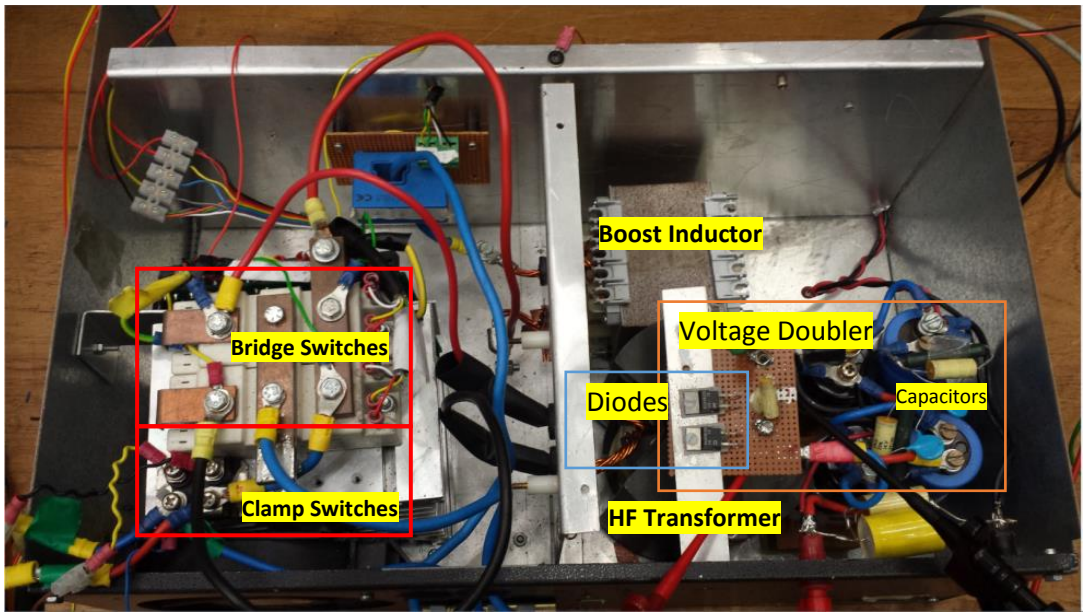


Fig.3.21 1.2 kW power converter

It was observed in the practical test that the ringing on the secondary winding also generated a high frequency noise on other waveforms which was not observed in the PSpice model. This high frequency noise was imposed on the signals that are generated by the dSPACE, and results in overshoots in the input voltage to the gate driver of the MOSFETs, as shown in Fig. 3.22. This noise could reach voltage magnitudes that could damage the gates of the power switches. These spikes could be eliminated by adding a filter.

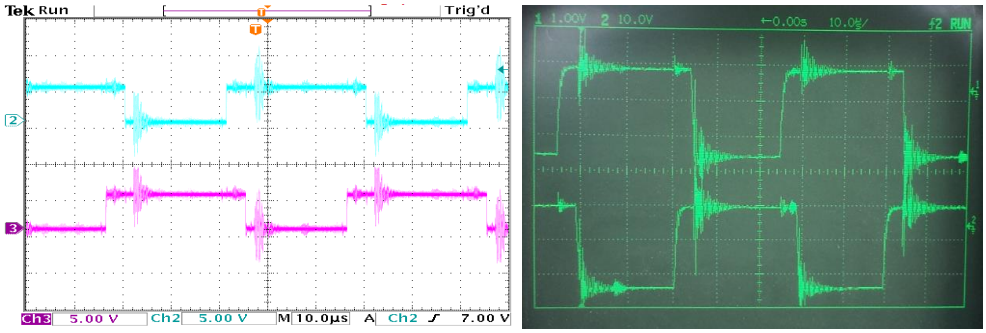
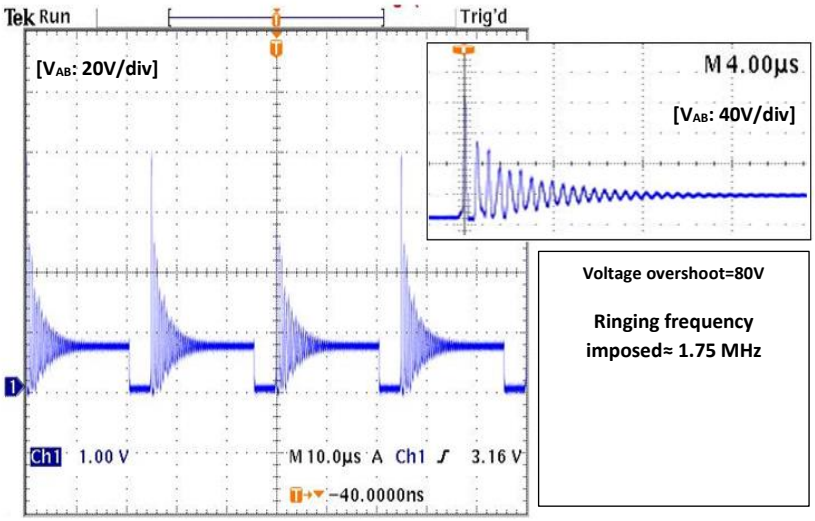
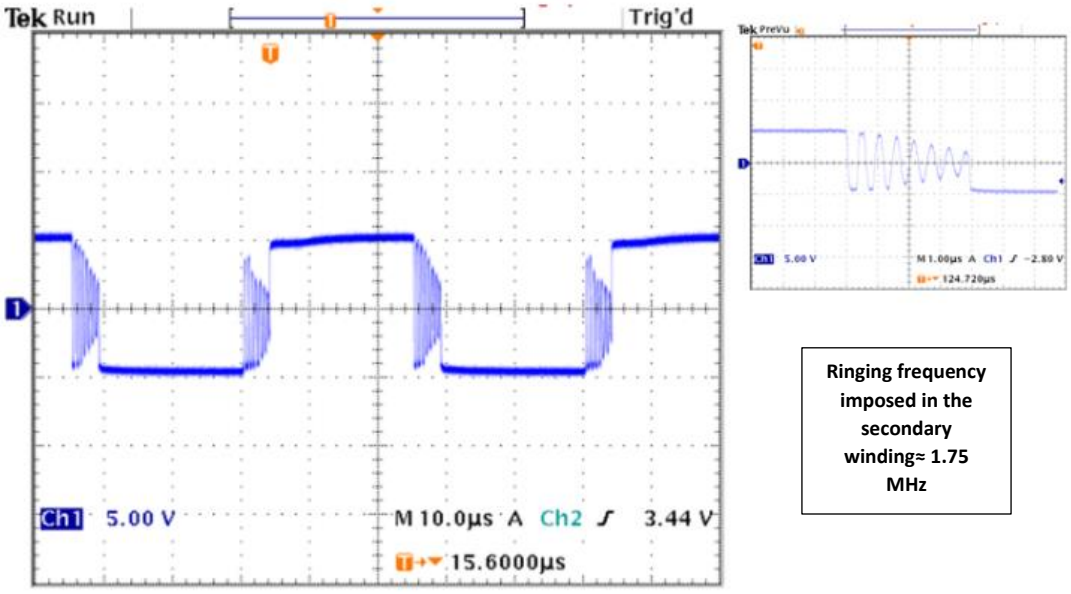


Fig. 3.22 (a) Switches drivers inputs (dSPACE output), (b) photograph for switches drivers output (gates pulses)



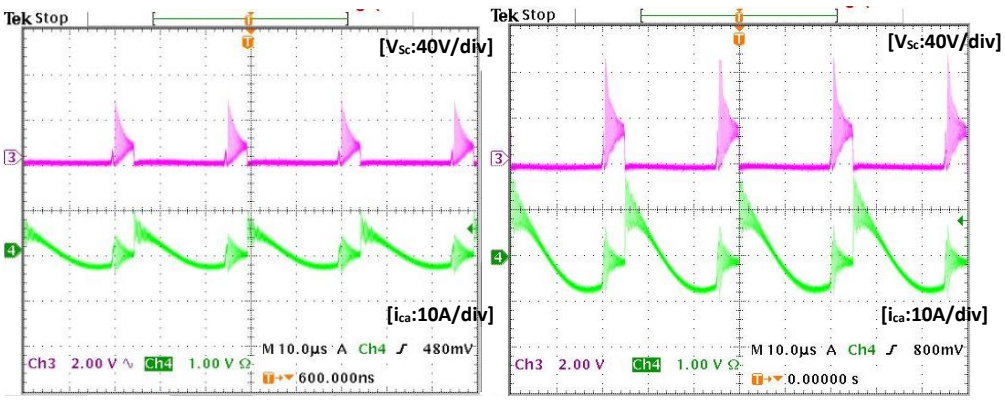
(a)



(b)

Fig.3.23 (a) Voltage across the MOSFETs, (b) secondary winding voltage

Fig.3.23 (a) above shows the voltage across the power switches. This result was taken without the active clamp connected to the converter circuit. It can be seen that the voltage overshoot across the switching devices is approximately equal to 80V, and there is a super-imposed damped voltage ringing (at 1.75 MHz) in both figures due to the resonant circuits of the low voltage side. While in Fig.3.23 (b) a high frequency ringing (1.75MHz) is super-imposed across both the secondary winding and across the rectifier diodes due to the resonant circuit on the bridge side during the overlap period. The difference in ringing frequency between the practical circuit (1.75MHz) and the PSpice simulation (2MHz, see Fig. 3.8) occurs because of the stray inductance of the wiring. The results in figures below (Fig.3.24 to Fig.3.26) were taken with the active clamp circuit added to the converter circuit.



(a) (b)

Fig.3.24 (a) Active clamp voltage (top) and active clamp current at 60 W, (b) Active clamp voltage (top) and active clamp current @ 312 W

Fig.3.24 shows the voltage across the active clamp and the current through the active clamp for the conditions of 60 W in (a), and 312 W in (b). It can be seen from Fig3.24 that there is a voltage ringing during the overlapping time across the clamp circuit caused by an energy exchange between the capacitor of the clamp circuit and the boost inductor. The overvoltage in Fig.3.24 (a) is equal to 48 V (for a 13 V input voltage) and this voltage reaches 88 V for an input voltage of 27 V as shown in Fig.3.24 (b), which means further

losses and reduced efficiency. Hence, the voltage ringing should be eliminated for an efficient converter.

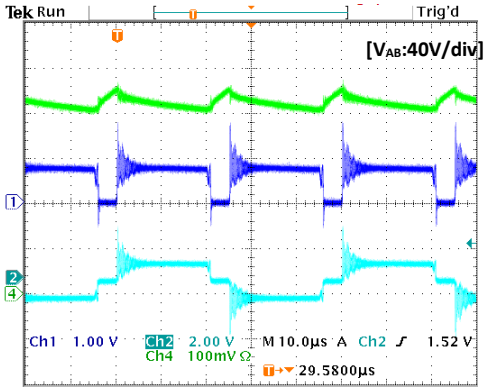
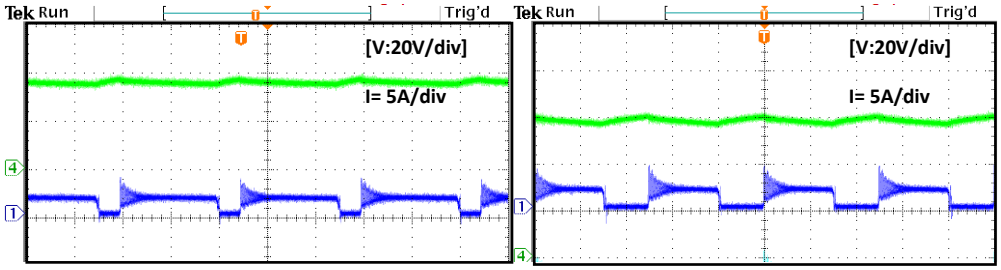


Fig.3.25 From the top: the boost current, bridge voltage, primary winding voltage when using the active clamp circuit with D=0.6.



(a) (b)

Fig.3.26 Boost current and bridge voltage [at 312 W] for (a) D=0.6, (b) D=0.7

It can be seen from Fig.3.26 that there is a slight increase in the voltage overshoot (from 80 V to 90 V) when the value of D is changed from 0.6 to 0.7 which increases the boost current from 9A to 15A.

To reduce the ringing and reduce the noise, thus improving the efficiency and the converter performance, modifications were made to the converter circuit. One of the modifications already made [97] was a redesign of the converter transformer. An earthed Faraday shield screen was included in the transformer, which was placed between the primary and secondary windings and between the outer core and the primary windings. Additionally, the transformer secondary winding was reduced. This arrangement keeps

the leakage inductance as low as possible (only 2μH) .Fig. 3.27 shows the transformer modification using Faraday shield screen.

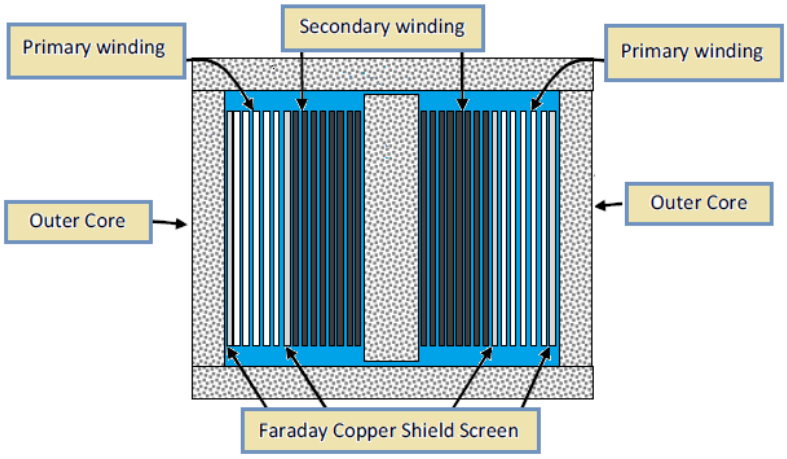
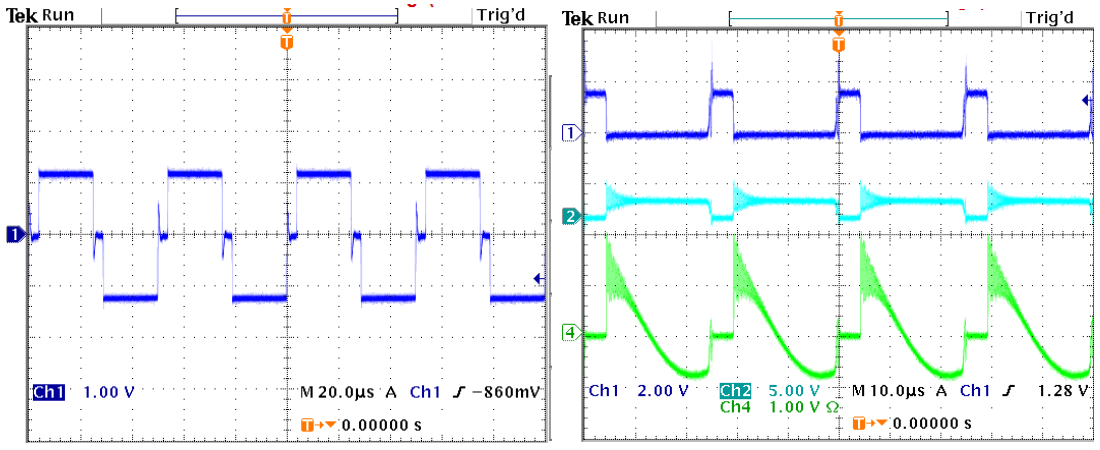


Fig. 3.27 Transformer-winding Modification

Another modification that was suggested in [97] is the use of switching devices with very low stray inductances and parasitic capacitance for the bridge and clamp circuits. This suggestion is one of the effective solutions to reduce the ringing produced by the resonant circuit and improve the converter's efficiency. New power switching devices based on Gallium Nitride (GaN) technology can also be considered instead of the existing SEMIKRON MOSFETs. Unfortunately, the cost of GaN devices is still very high and they are not readily available from suppliers.

An RC snubber circuit would be effective in reducing the ringing and therefore clamp the voltage spike across the clamp switch, by absorbing the circulating energy, thus reducing the switching losses. Unfortunately, dissipation of the circulating energy in the snubber will reduce the converter efficiency. To see the effect, an RC snubber was added across the active clamp switch and another one across the transformer secondary windings. Fig3.28 shows the results for the active clamp circuit and the secondary winding with the modification, and Fig. 3.29 shows the results in the PSpice model.



(a) (b)

Fig.3.28 Results with the RC snubber modification [312 watt, D=0.6]: (a) transformer secondary voltage, (b) From the top active clamp voltage, voltages across the bridge switches, and the active clamp current

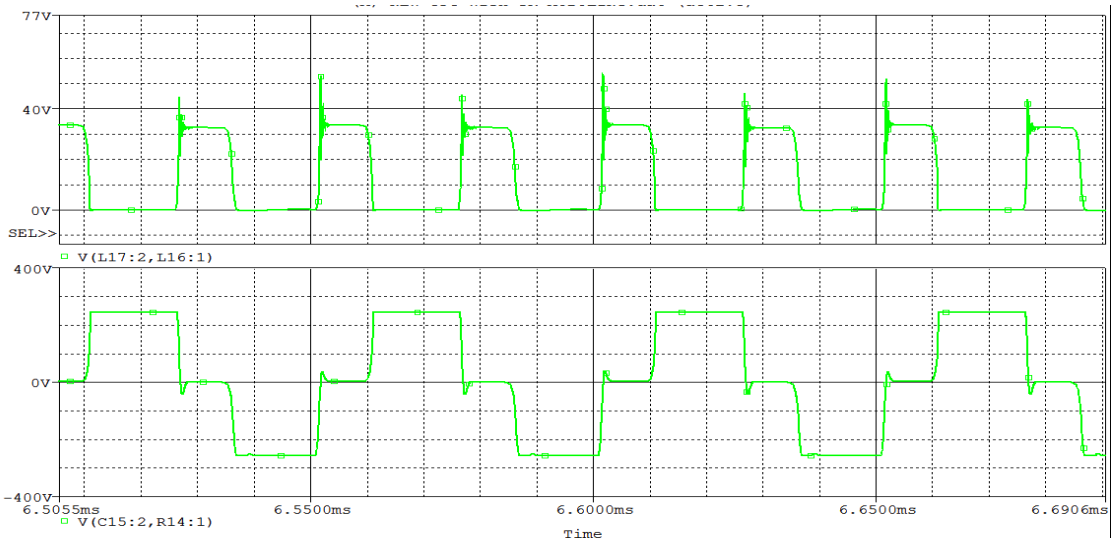


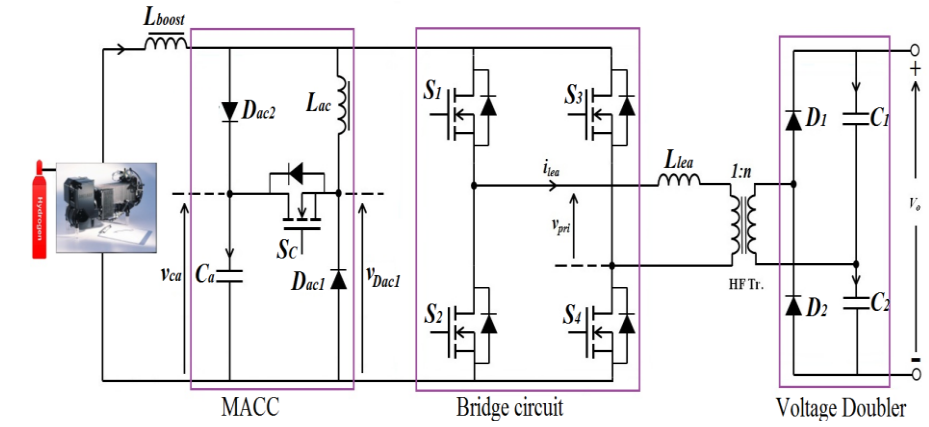
Fig. 3.29 The results in PSpice model, from the top the active clamp voltage, secondary winding voltage

By comparing the results in Fig.3.23 (b) and Fig.3.24 (b) with the results in Fig.3.28, it can be seen that the modifications have significantly reduced the effects of the voltage ringing. The overvoltage across the active clamp switch has been reduced to 54% (from 88 V to 48 V), and the ringing has been eliminated in both the active clamp (voltage and current), and the secondary winding voltage. Furthermore, the results from the PSpice model with the new modification confirm the practical results as shown in Fig.3.29, which proves the high accuracy of the PSpice software in modelling and simulation of the power electronic circuits.

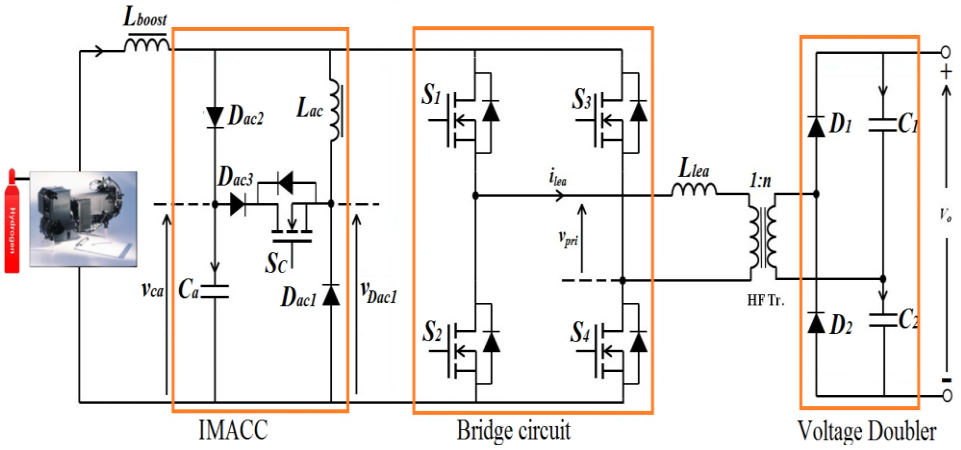
During the test it was observed that when D approached unity, the output voltage decreased rather than increased due to the resistance of the boost inductor [126, 127]. The value of D must be constrained to be less than the higher limit to prevent such a problem.

3.10 FBCFC Modification with a Modified Clamp Circuit

This section presents a FBCFC with a new modified ACC (MACC), based on a circuit suggested in [128] as shown in Fig.3.30a, to retain the desired rectangular shape of the current and improve the efficiency of the converter. A further improvement was applied to the circuit of Fig.3.30a by adding the diode D_{ac3} to overcome the unwanted behaviour of the MACC, as will be explained in the next section. Fig.2.30b shows the FBCFC with the improved modified active clamp circuit IMACC and the voltage doubling rectifier.



(a)



(b)

Fig.3.30. FBCFC with: a) MACC, b) IMACC

3.10.1 Circuit Improvement

As can be seen in Fig.3.30b, the IMACC consists of two diodes (D_{ac1}, D_{ac2}), an inductor L_{ac}, a MOSFET switch S_c and a capacitor C_a. The diode D_{ac3} has been added in series with S_c to eliminate reverse current in the regenerative clamp switch due to its intrinsic body diode, hence, improve the circuit performance. This circuit works as follows: initially all bridge switches are closed to allow the current in the input inductance L_{boost} to build up; when two diagonal switches are switched off this current is first commutated to C_a via D_{ac2}, giving the transformer current time to build up. This stage ends when the capacitor current reaches zero and diode D_{ac2} is reverse biased. By turning on S_c, C_a will discharge through L_{ac} to the primary of the transformer and to the load. When S_c is turned off, the stored energy in L_{ac} will then be released through D_{ac1} via the transformer to the load.

3.10.2 Analysis and Performance of the IMACC

In order to describe the operational process of the modified regenerative clamp circuit, the following assumptions have been made [119, 78, and 128]:

- To ensure operation in continuous current mode (CCM), the bridge switches should be turned on and off with a duty ratio greater than 0.5. Added to that, both the boost inductor (L_{boost}) and the voltage doubler capacitors are considered large enough to guarantee CCM operation.

- The magnetizing inductance of the high frequency transformer is neglected.
- The on-state resistance of the power switches is neglected.
- The power switches and the diodes are assumed to be ideal.

Fig.3.31 shows the timing waveforms that describe the operation of the IMACC during the duty cycle of one pair of diagonal bridge switches (S_1 and S_4). The timing waveforms

of the MOSFET switches during half of the switching period T_s, together with the currents in the key components, including the clamp capacitor voltage, are all obtained from a PSpice simulation. Also shown (dashed) are the equivalent currents when a CACC is employed for comparison.

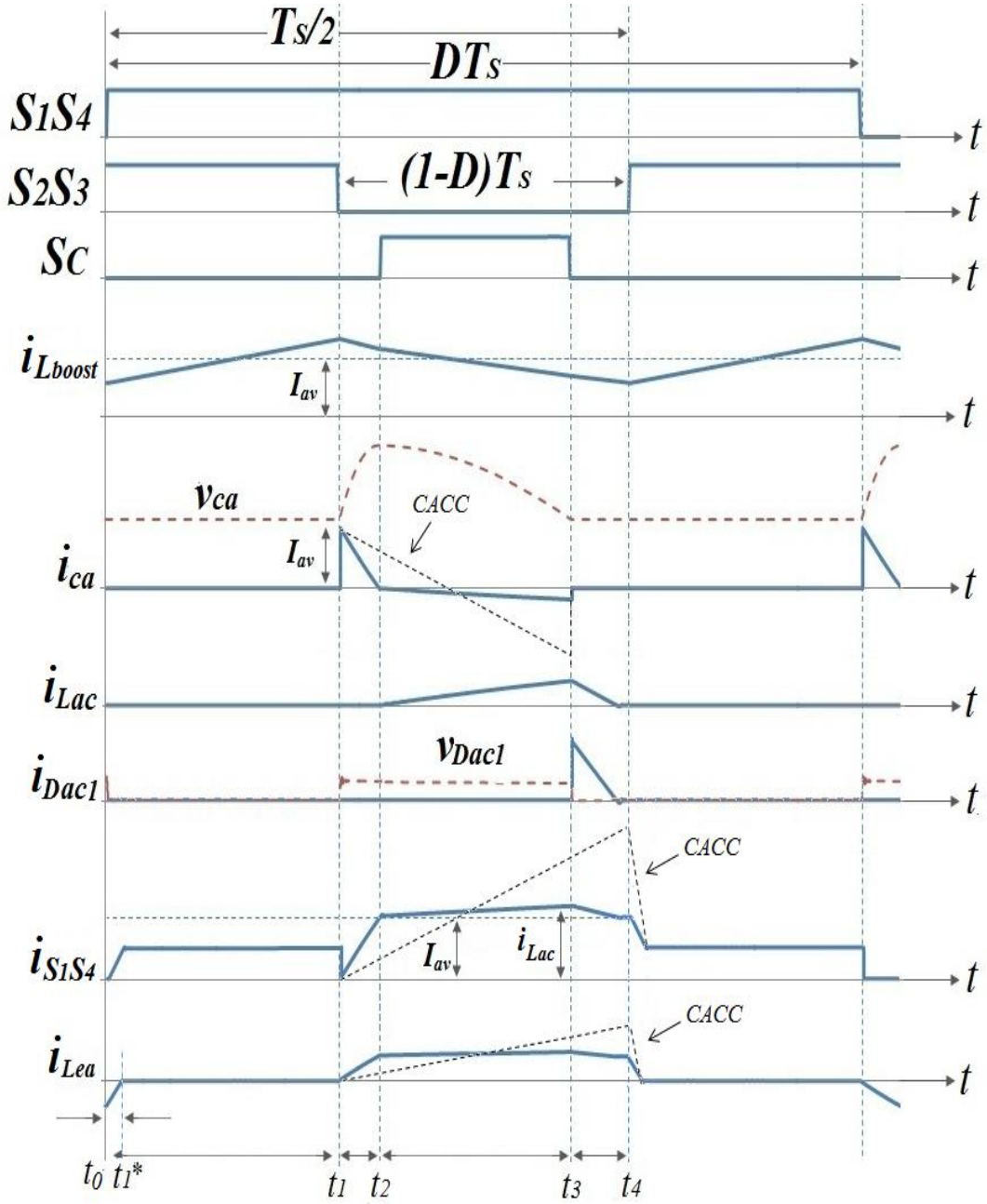


Fig. 3.31. Waveforms of the FBCFC with the modified regenerative clamp circuit

Four intervals can be distinguished during each half of the switching period T_s:

- Stage 1: $t_0<t<t_1$

During this period, all the main switches from S_1 to S_4 are turned on (the overlap period). The regenerative clamp switch S_c is turned off and the leakage inductance is shorted. The boost inductor current builds up during this stage, and the current in each leg of the main bridge switches is equal to the half of the average boost inductor current I_{av} . Because of the voltage across C_a, retained from the previous cycle, the diodes D_{ac1} and D_{ac2} are reverse biased. The boost inductor current is given by:

$$i_{L_{boost}}(t)=\frac{v_{L_{boost}(t)}}{L_{boost}}(t-t_1) \tag{3.7}$$

The leakage inductance current for the period from t_0 to t_1* is given by:

$$i_{lea}(t)=-I_{av}+\frac{V_o}{2nL_{lea}}(t-t_1) \tag{3.8}$$

and remains at zero for the remainder of this period.

- Stage 2: $t_1<t<t_2$

During this interval, two of the diagonal switches S_2S_3 are turned off. The diode D_{ac2} is forward biased due to the energy in the leakage inductance L_{lea}. The clamp capacitor C_a starts charging through D_{ac2} with the difference current equal to I_{lea} and I_{av}. Hence:

$$I_{ca}=I_{av}-I_{lea} \tag{3.9}$$

$$I_{av}=\frac{V_{ca}-V_{pri}}{L_{lea}}(t-t_2) \tag{3.10}$$

$$V_{pri}={}^{V_o}/_{2n} \tag{3.11}$$

The charging period process will continue until I_{av} is equal to I_{lea}, where the capacitor current I_{ca} reaches zero and the diode D_{ac2} becomes reverse biased.

- Stage 3: $t_2<t<t_3$

In this interval, the clamp switch S_c is turned on and the capacitor C_a starts to discharge to the load through L_{ac} and the primary winding of the HF transformer. The current I_{Lac} grows linearly according to:

$$i_{Lac}=\frac{V_{ca}-V_{pri}}{L_{lea}+L_{ac}}(t-t_3) \tag{3.12}$$

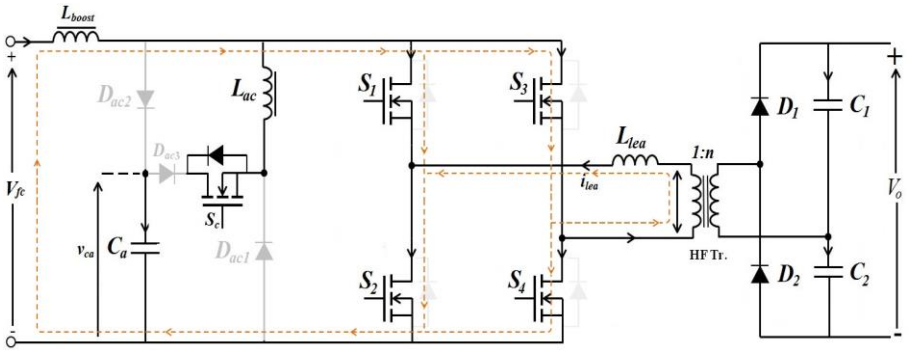
- Stage 4: $t_3<t<t_4$

During this interval, the clamp switch is turned off so that the energy in inductor L_{ac} is fully discharged to the load through the diode D_{ac1} and the HF transformer. The current during this period is given by:

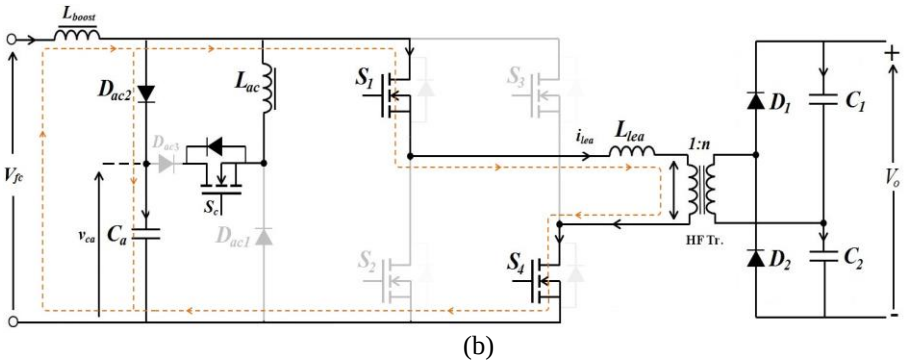
$$i_{Lac}=\frac{V_{pri}}{L_{lea}+L_{ac}}(t-t_4) \tag{3.13}$$

The energy in L_{ac} must be discharged before the start of the next overlap period.

Fig.3.32 shows the equivalent circuits of the FBCFC for each operating stage of the IMACC.



(a)



(b)

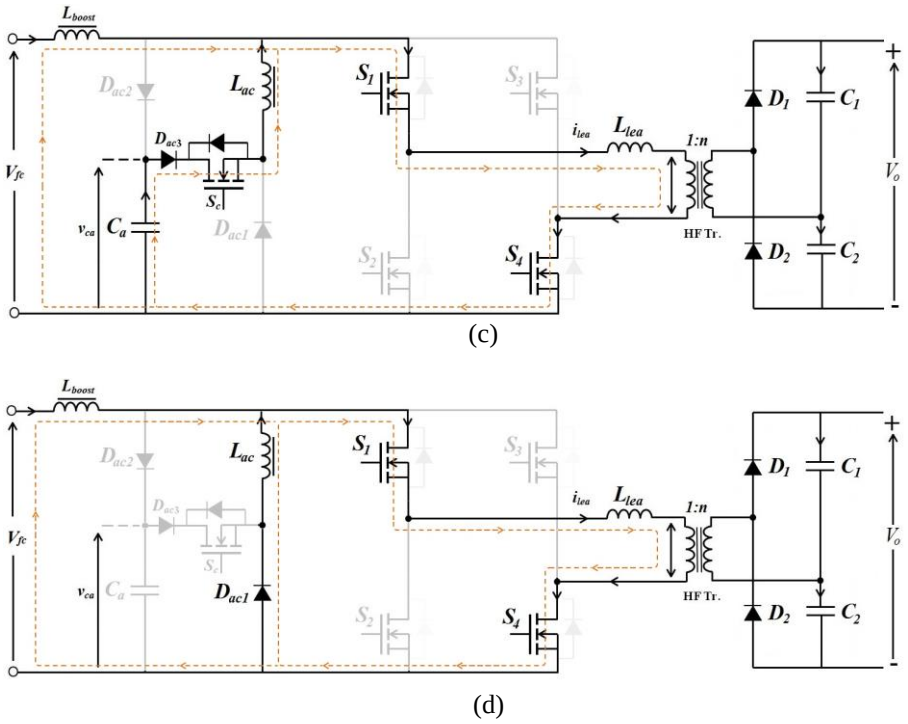


Fig. 3.32. Equivalent circuits of the FBCFC for each operating stage of the MACC according to the time intervals in Fig.3.30: (a) t_1 (b) t_2 (c) t_3 (d) t_4

3.11 FBCFC Modelling and Simulation Set up with the IMACC

In order to implement and test the IMACC in an existing FBCFC the circuit in Fig.3.30 were first modelled and simulated using PSpice to compare the performance of the FBCFC with each clamp circuits. Fig.3.33 shows the simulation results for IMACC. It can be seen that in the case of the IMACC the transformer (and bridge) currents are very nearly rectangular shaped with a considerably lower rms value than the peaky currents resulting from the CACC (Fig.3.11). And while the transformer voltages are close to square waves in both cases, a higher voltage ringing can be observed with the CACC. Furthermore, with the IMACC, there is no need to use RC snubber circuit as was required with the CACC (see section 3.9 above).

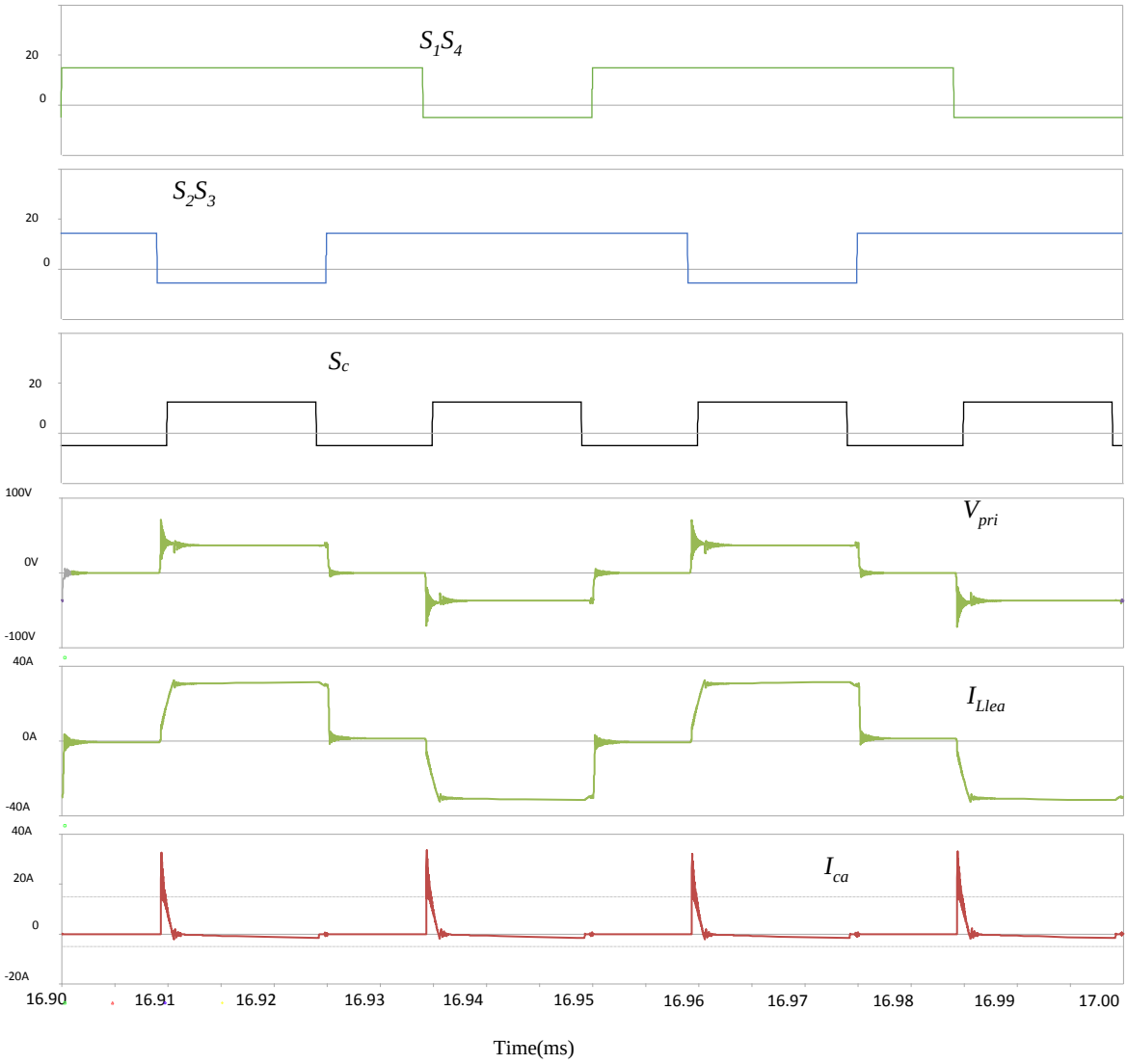


Fig. 3.33. Simulation result of the FBCFC circuit combined with IMACC; from the top: the gate pulses, the primary winding voltage and current, and the clamp capacitor current

The circuit described in [127] does not take into consideration the intrinsic (anti-parallel) diode of the active clamp MOSFET switch (S_c). This diode has an effect on the clamp circuit by providing a parasitic current path to the clamp capacitor, which results in a circulating current through S_c and hence higher losses. Fig.3.34 shows simulation results for the FBCFC circuit including the intrinsic MOSFET diode, illustrating the effect this has on the circuit currents and voltages.

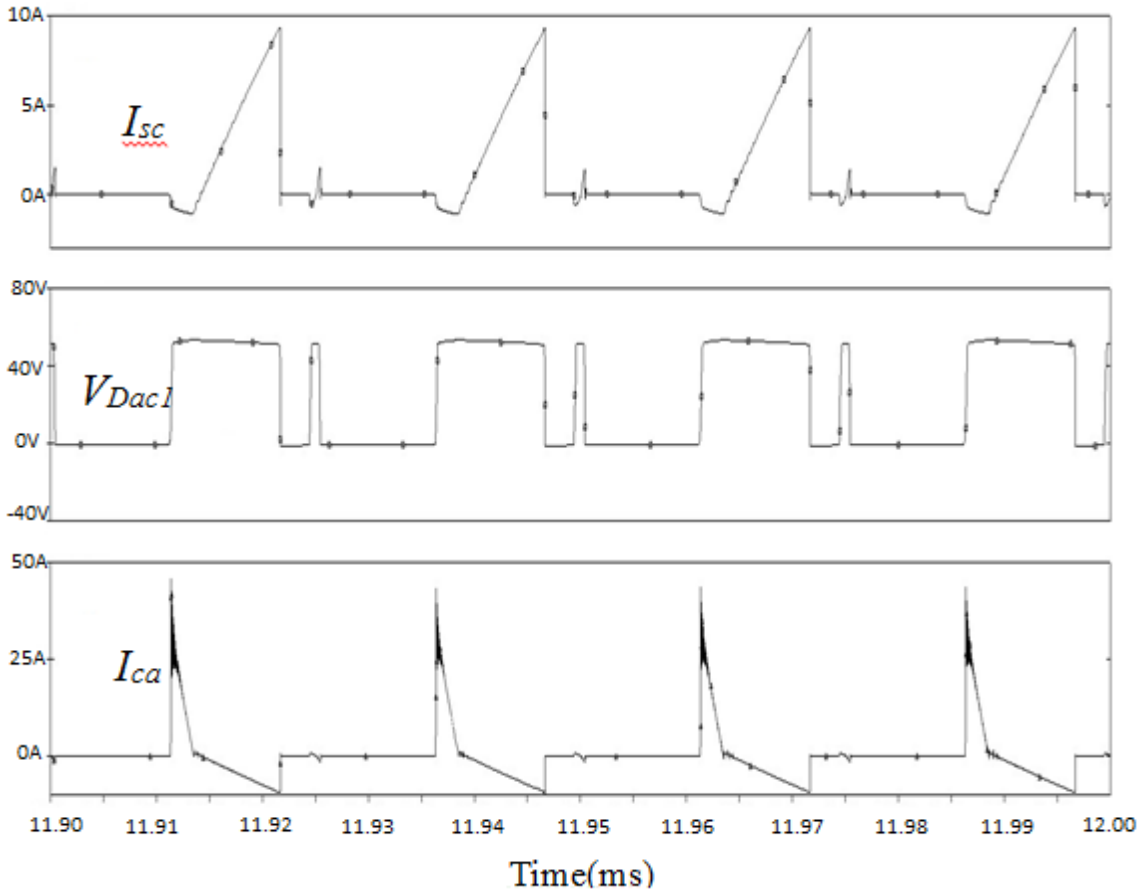


Fig.3.34 Simulation results for the FBCFC circuit showing the effect of the intrinsic diode of the active clamp MOSFET; top: clamp switch current, middle: voltage across *Dac1*, bottom: clamp capacitor current

In order to eliminate the reverse current in the active clamp switch, a diode, D_{ac3}, must be added in series with S_c as shown in Fig.3.35. Simulations including both the intrinsic MOSFET diode and the series diode D_{ac3} produce the same waveforms as shown in Fig.3.34, demonstrating that the reverse current caused by the intrinsic diode of the clamp switch has now been eliminated as shown in Fig.3.36.

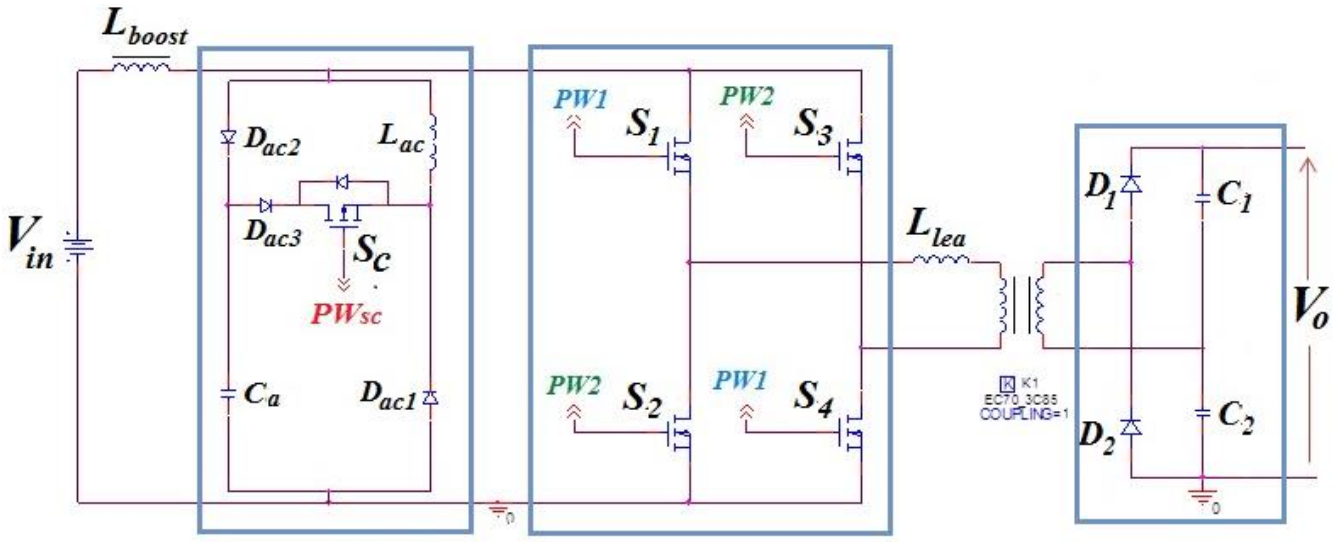


Fig. 3.35 Improved Modified active clamp circuit with series diode D_{ac3}

Fig.3.36 shows a simulation waveforms of the current in S_c, the voltage across diode Dca1 and the current in C_a for the IMACC.

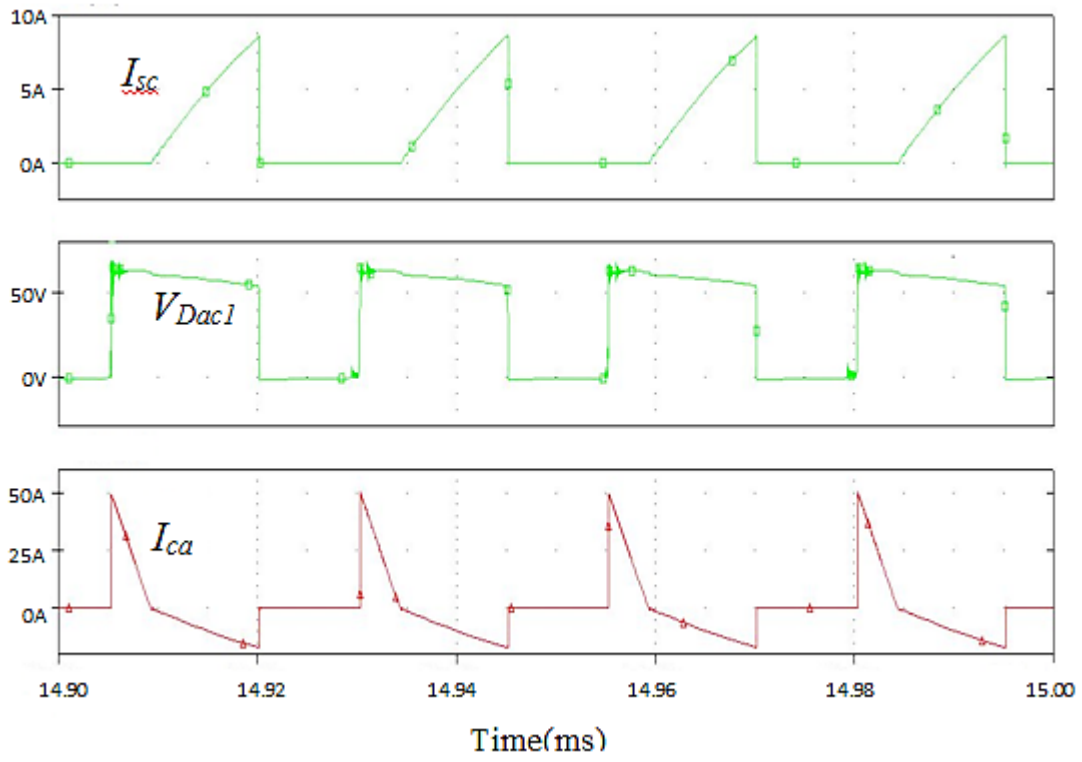


Fig. 3.36 Simulation results for the FBCFC with MACC; top: clamp switch current, middle: voltage across D_{ac1}, bottom: clamp capacitor current

Using the results of simulations over the full power range of the fuel cell, the efficiency of the converter fed from a constant voltage source was determined for both clamp circuits. The results in Fig. 3.37 demonstrates that the simulation predicts an overall improvement with the use of the IMACC of up to 2% over the CACC.

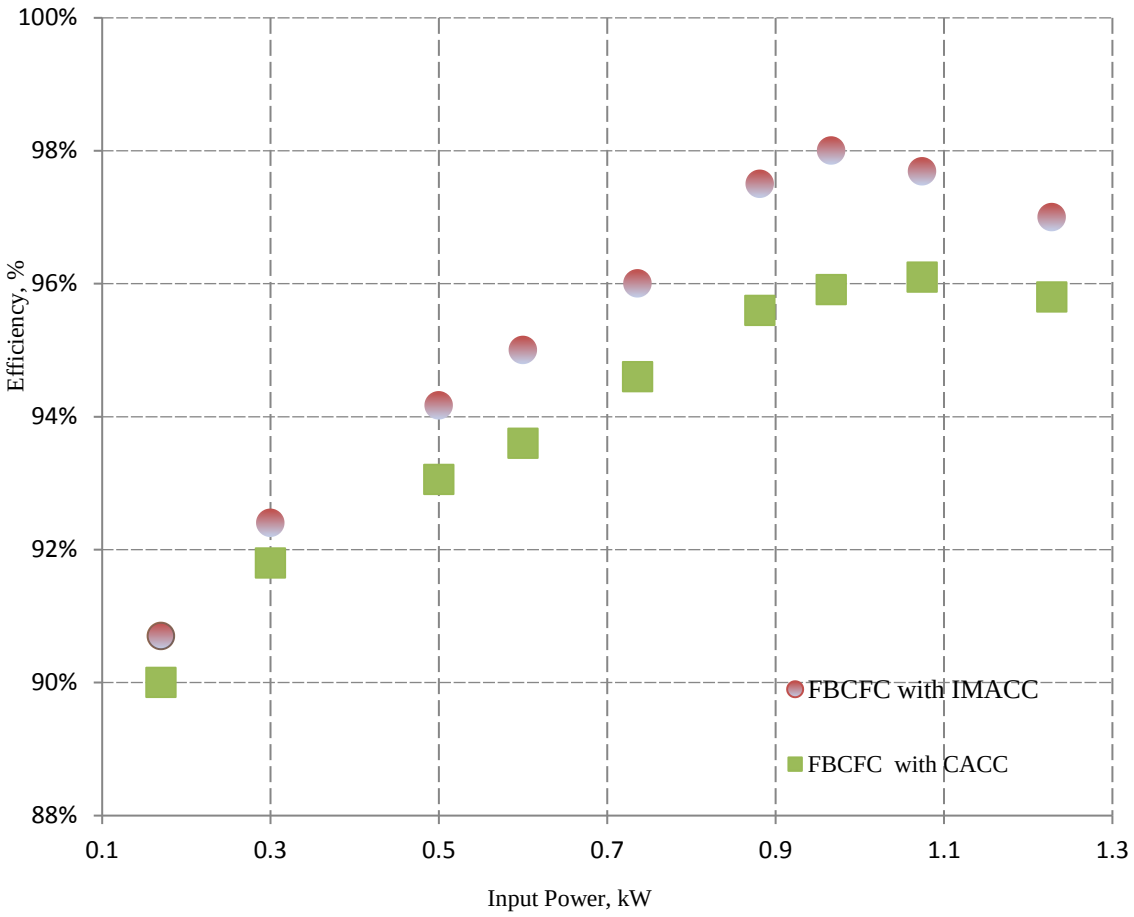


Fig. 3.37 Efficiency at constant input voltage (simulation)

3.12 Experimental Validation of the IMACC for the FBCFC

In order to verify the simulation results and the circuit improvements, an experimental setup has been built using an existing 1.2 kW FBCFC. The required gate pulses are generated using dSPACE hardware, employing the DS1103SL_DSP_PWM3 block in Matlab, which has the ability to generate pulses with a frequency up to 5MHz. Fig.3.38 shows the block diagram of the experimental set-up. The components and the parameters of the prototype converter are shown in Table 3.1.

TABLE 3.1 PARAMETERS AND COMPONENTS OF THE CONVERTER USED FOR SIMULATION & PRACTICAL TESTS

Parameters & Components	Part/Value Practical
Rated Power	1.2kW
Input voltage	42-26V DC
Output voltage	650V DC
Output capacitors C_1, C_2	2x 470µF 400V Electrolytic + 1uF 1000V polyester in parallel
Clamp capacitor C_a	10µF 250V polyester
Clamp inductor L_{ac}	10µH
Main bridge & clamp switches	IXFK120N20 (200V/120A) R_{DS}(on)=17mΩ, with SKHI21A Driver
Transformer leakage inductance L_{lea}	2µH
Transformer turns ratio n	5:37
Boost inductor L_b	475 µH
Rectifier diodes	C2D05120A
Clamp circuit diodes	STTA9012TV1
Switching Frequency f_s	20kHz

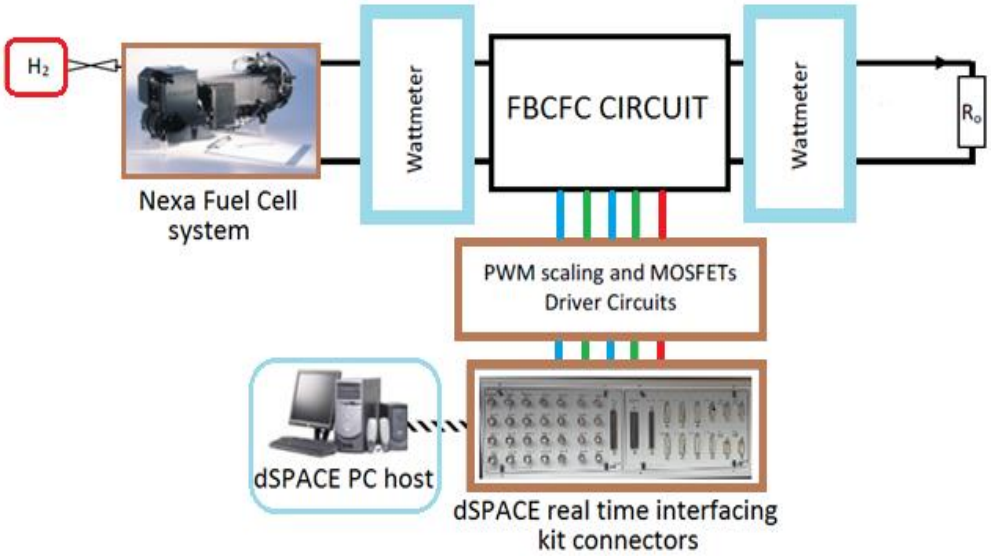


Fig. 3.38 Block diagram of experimental set-up

The value of C_a in Table I was optimised in [129]. The L_{ac} value was optimised according to equation 3.12 and by using PSpice. According to equation (3.12), the relationship between the i_{Lac} and L_{ac} is inverse which means a higher L_{ac} will reduce the effect of discharging current of the clamp capacitor on the bridge current. L_{ac} has been selected to give a more gradual increase in the bridge current, and sufficient discharge time for C_a. Fig.3.39 shows the bridge current i_{Llea} and the clamp capacitor current i_{ca} for different values of L_{ac}. As Fig.3.39 shows, the optimised value of L_{ac} is falling between 7.5µH and 20µH which gives the best gradual current shape. However, an L_{ac} higher than the selected value means a larger size design and a higher cost, with only a slight improvement over the selected value. Hence, a 10µH inductor was chosen as an optimum value for the IMACC.

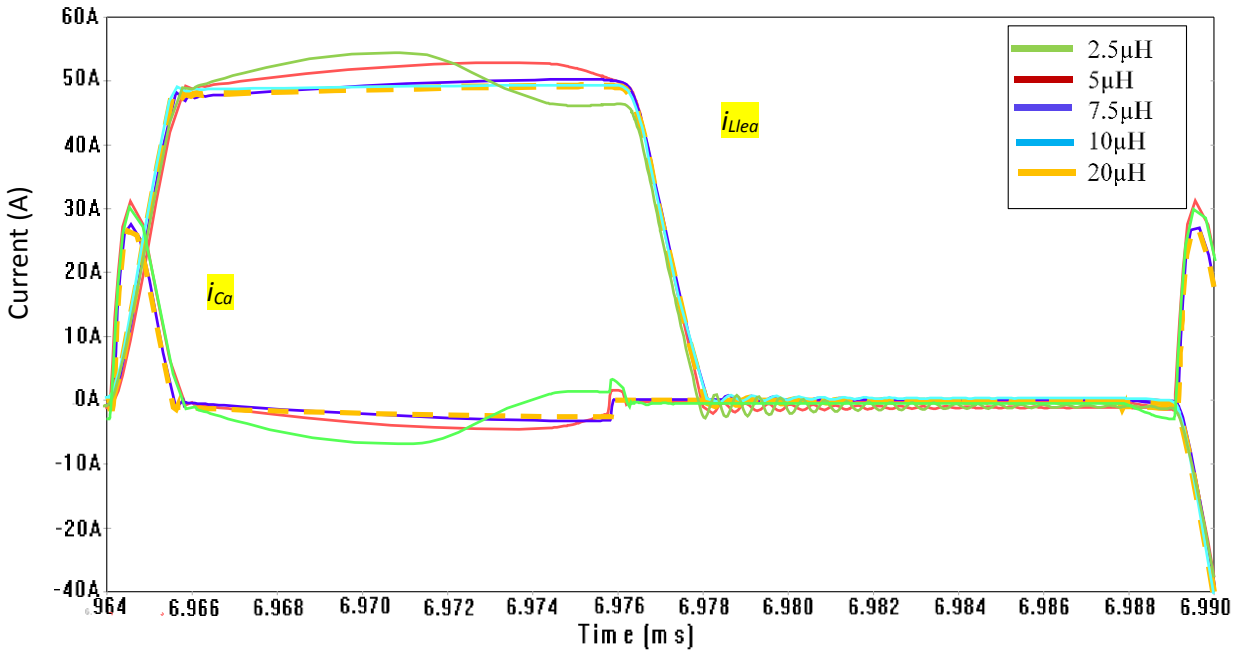


Fig.3.39 Bridge current i_{Llea} and the active clamp capacitor current i_{Ca} with a different values of L_{ac}

Fig.3.40 shows the FBCFC combined with the IMACC. Further modifications have been made to the existing converter by replacing the old dual MOSFET blocks that are no

longer produced by the manufacture with single new dual blocks. Adding to that, the drive circuit was placed away from switching devices to minimize any interference between the drivers and the power components of the converter.

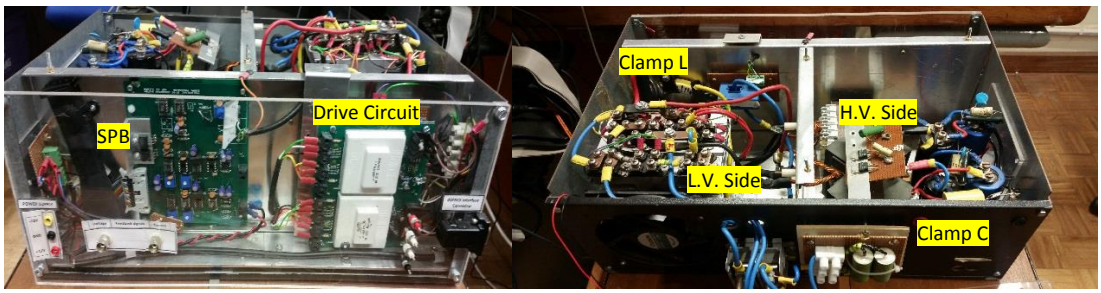
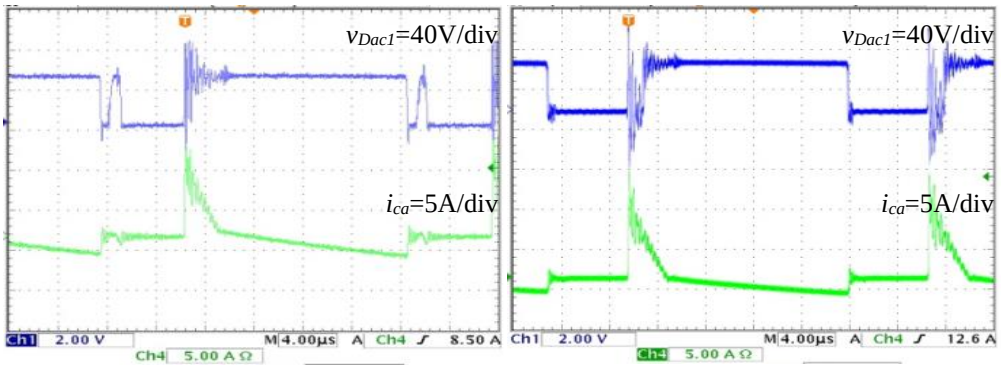


Fig.3.40 FBCFC combined with the IMACC

Fig.3.41 shows a practical result to compare some waveforms of the FBCFC circuit with the IMACC, without the series diode D_{ac3} (MACC) (a), and with (b). From Fig.3.41b it can be seen that the effect of the intrinsic diode of the clamp switch in Fig.3.41a is significantly reduced.

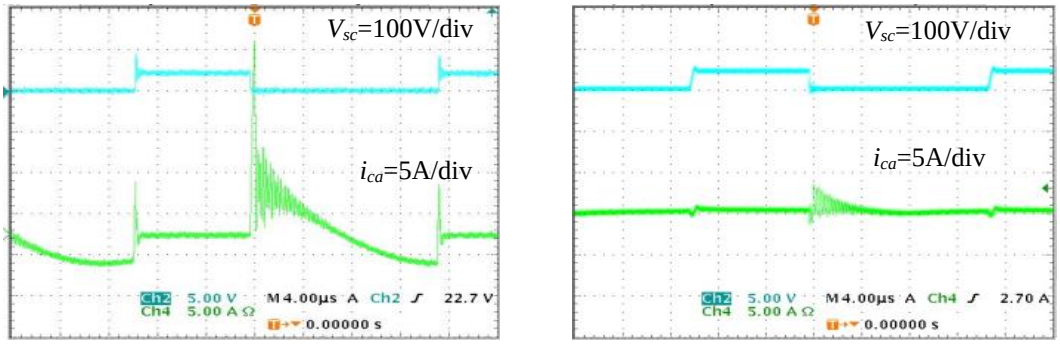


(a) (b)

Fig. 3.41 Voltage across D_{ac1}, and clamp capacitor current of the IMACC at 40% of the full load: a) without series diode D_{ac3}, b) with series diode D_{ac3}

Figures 3.42 to 3.44 below shows practical results to compare and validate the simulation for the FBCFC with CACC and the IMACC.

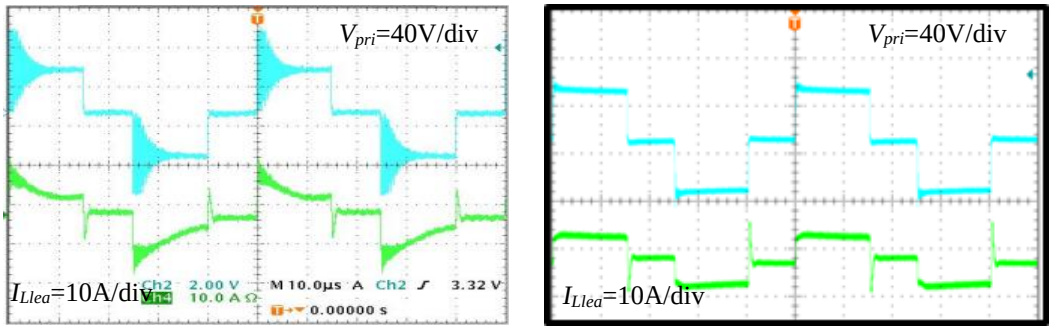
Fig.3.42 shows the clamp switch voltage and the clamp capacitor current for both the CACC (a) and the IMACC (b) at 15% of full load. By comparing these results it is obvious that the IMACC performs better than the CACC.



(a) (b)

Fig. 3.42 Clamp switch voltage (top) and clamp capacitor current (bottom) at 15% of the full load for: a) CACC, b) IMACC

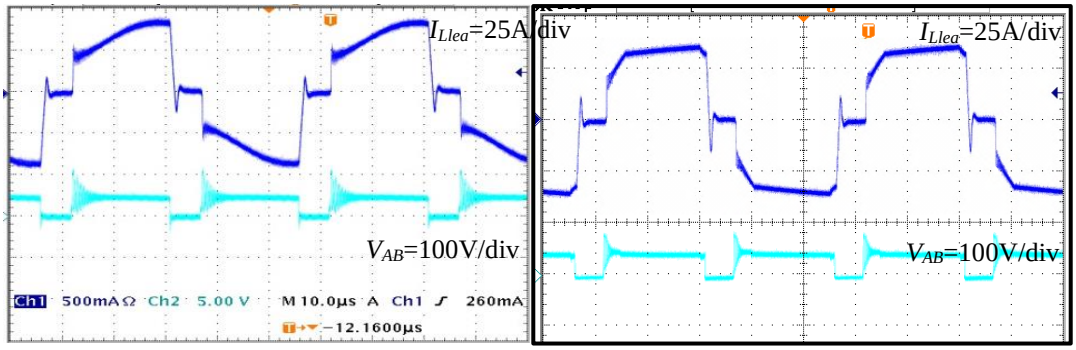
Fig.3.43 shows the primary winding voltage and current at 15% of full load. From Fig.3.43a it can be seen that there is a high ringing on the primary winding voltage which is due to a resonance between the clamp capacitor and the leakage inductance. This ringing could be reduced by adding a snubber circuit across the clamp switch, but this would result in additional losses. However, the result in Fig.3.43b shows that using the IMACC a significant reduction in the ringing can be achieved without compromising efficiency.



(a) (b)

Fig. 3.43 Primary winding voltage (top) and current (bottom) at 15% of the full load for :a) CACC, b) IMACC

Fig.3.44 depicts the primary winding current and the voltage across the main switching devices for the CACC (a) and the IMACC (b). Both Fig.3.43b and Fig.3.44b show that with the IMACC the shape of the primary winding current and voltage are much closer to the desired rectangular waveforms (with a consequently lower rms value of the current) than obtainable with the CACC (Fig.3.43a and Fig.3.44a).



(a) (b)

Fig. 3.44 Primary winding current (top) and voltage (bottom) across the main devices at 90% of full load: a) CACC, b) IMACC

When compared with the practical results, the simulation results prove the usefulness of PSpice simulations in designing modifications to the FBCFC circuit.

3.13 Converter Efficiency Measurement

In order to compare the overall performance of the FBCFC with the two clamp circuits, the efficiency was measured with various loads up to 1.2 kW. The results depicted in Fig.3.45 demonstrate an efficiency improvement with the new clamp configuration of up to 2%, with a maximum value of 98%, in close agreement with the results of the simulations.

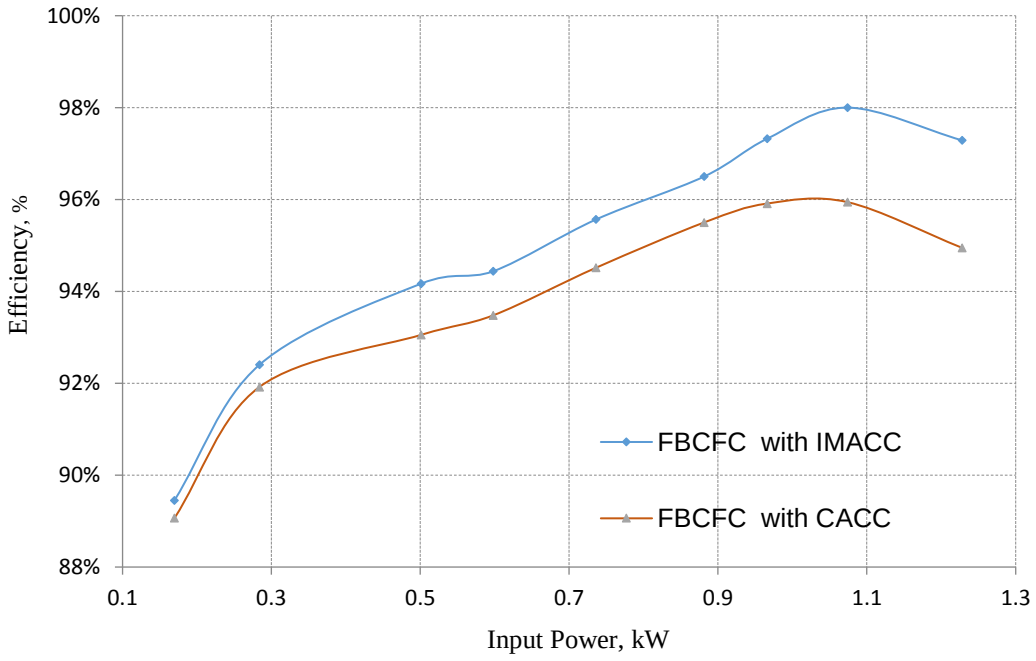


Fig. 3.45 Efficiency using a constant voltage source

It must be noted that the results in Fig.3.45 were measured using a DC power supply with constant output voltage as a source. Because the converter is designed for FC applications, another efficiency test was carried out using an actual FC, the Nexa 1.2kW. Fig.3.46 shows the efficiencies obtained under this condition. It can be seen from Fig.3.46 the efficiency at higher converter outputs reduces steadily. This is due to the drop in FC output voltage with increasing load (see chapter two), forcing the converter to work with an increasing overlap period (Cf. Fig.3.11). However, the converter efficiency remains above 90% over most of the power range, which is considerably better than with a VFC, and the IMACC still provides a better performance compared with the CACC.

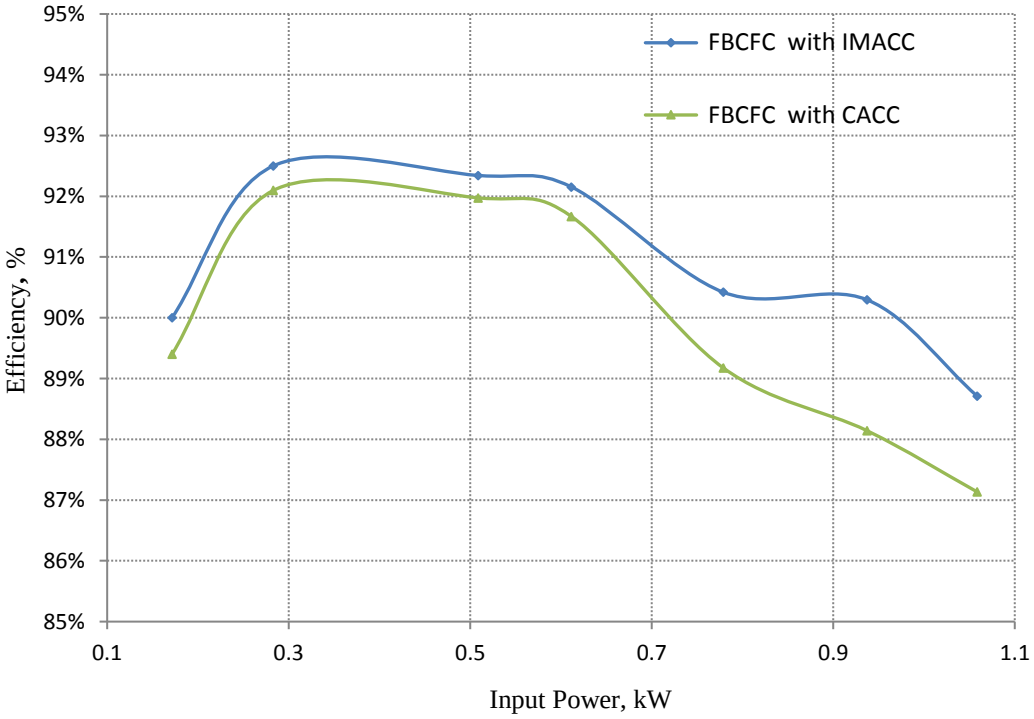


Fig. 3.46. Converter efficiency using a Nexa 1.2kW FC as source

3.14 Conclusion

An improved modified active clamp circuit (IMACC) for a full bridge current fed converter that is suitable for fuel cell applications has been investigated. Simulations using OrCAD16.6 and experimental results have shown that the new circuit provides better performance in reducing the effect of the clamp capacitor energy on the current shape, hence decreasing the losses and increasing the efficiency. The result of the converter using constant input voltage source shows an efficiency improvement with the IMACC of up to 2%, reaching 98% at full load. Efficiency tests using a fuel cell source show a reduction in efficiency of the converter at high loads due to the voltage-current characteristic of the FC. Nevertheless, the converter efficiency remains above 90% over most of the power range, and the IMACC still provides a better performance compared with the CACC.

Chapter Four

Chapter Four

Fuel Cell Converter: Control and Dynamic Performance

4.1 Introduction

In order for the FC converter to operate at the desired DC link voltage, a closed loop control system needs to be designed to regulate the converter output voltage at a specified constant value; even though when changes occur in the loads and variations of the FC output voltage[2]. A dynamic model for the FBCFC including the conventional active-clamp circuit (CACC) was developed in [97]. This model was investigated and used in designing an FBCFC controller along with its modified active clamp circuit. However, as predominantly known about most other boost converters, the transfer function of the converter exhibits a right-half- plane zero (RHPZ), or it is called the non-minimum-phase system which needs to be considered.

4.2 Minimum-Phase Systems and Non-Minimum-Phase Systems

Transfer functions which have neither poles nor zeros in the right-half S plane are called minimum-phase transfer functions, whereas those with poles and/or zeros in the right-half S plane are called non-minimum-phase transfer functions, or a right-half- plane zero (RHPZ). With systems which have similar magnitude, the range in phase angle of the minimum-phase transfer function is minimum, whereas the phase angle in any of the non-minimum-phase transfer function is higher.

For a minimum-phase system, it is easy to determine the transfer function from the magnitude curve only. Yet, for a non-minimum-phase system this function cannot be applied. There is no effect on the magnitude curve when multiplying all-pass filters by any transfer function, yet the change occurs in the phase curve.

[2] Fuel-cell voltage varies with certain parameters such as fuel flow, fuel pressure, fuel cell stack temperature etc.

For instance, consider the two systems $(G_1(j\omega), and G_2(j\omega))$ in equation (4.1) whose sinusoidal transfer functions are;

$$G_1(j\omega) = \frac{1 + j\omega T}{1 + j\omega T_1}, \quad G_2(j\omega) = \frac{1 - j\omega T}{1 + j\omega T_1}, \quad 0 < T < T_1 \tag{4.1}$$

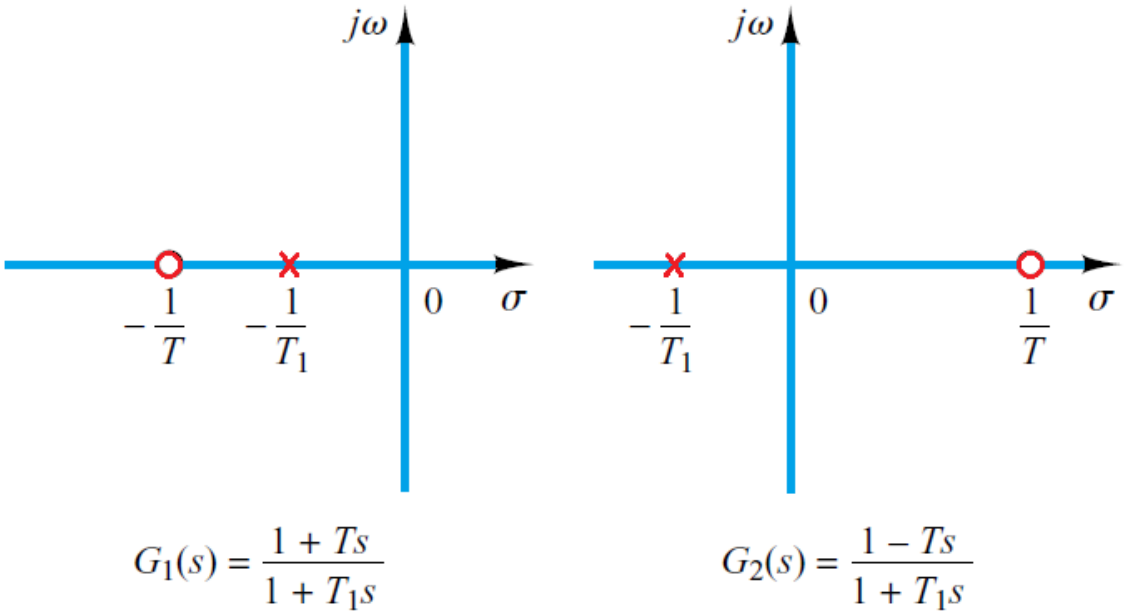


Fig.4.1 Pole–zero configurations of a minimum-phase system G1(s) and non-minimum-phase system G2(s)

Fig.4.1 shows the pole–zero configurations of these systems. As can be seen, the transfer functions have different phase-angle properties, but they have the same magnitude features. As shown in Fig. 4.2., these two systems are different from each other as follows:

$$G(j\omega) = \frac{G_2(j\omega)}{G_1(j\omega)} = \frac{1 - j\omega T}{1 + j\omega T} \tag{4.2}$$

G(jω) magnitude is always unity. But the phase angle varies from 0° to –180° as ω is increased from zero to infinity. The magnitude and phase-angle properties of a minimum-phase system are related. That is to say, the phase-angle curve is uniquely specified when the magnitude curve of a system is determined across the whole range of frequency from zero to infinity, and vice versa. However, this does not apply to a non-minimum-phase

system. Non-minimum-phase situations may appear in two different manners: first, when a system incorporates a non-minimum-phase element or elements; secondly, when the situation arises in an unstable minor-loop case.

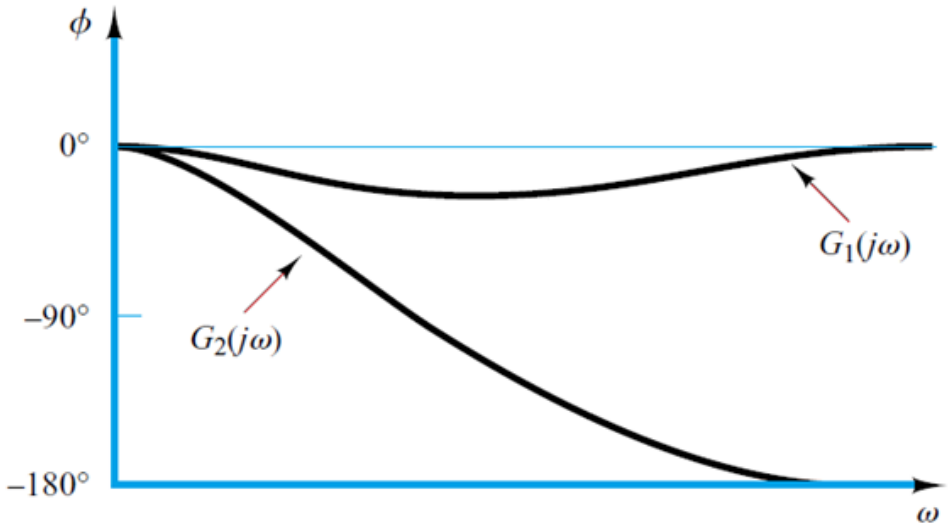


Fig.4.2 Phase-angle characteristics of the systems G1(s) and G2(s) shown in Fig.4.2

Non-minimum-phase systems are slow in responding because of their limited bandwidth (BW) behaviour at the start of a response. In most practical control systems, excessive phase lag should be carefully avoided [130].

For the CFCs, if a single-loop controller is used to control the output voltage, the RHPZ would limit the available bandwidth (BW) for stable operation of the proposed converter. Different techniques have been proposed to eliminate the RHPZ or to increase the RHPZ frequency in order to speed up the response of the system [131, 132]. However, these techniques make the input current discontinuous, which is not acceptable for a FC source. One control possibility is the use of a direct duty cycle control to govern the output voltage. However, the available bandwidth for a stable operation of the converter would be limited because of the RHPZ. For that reason, to eliminate the RHPZ effect, a two-loop controller has been used. It simplifies the design of the control loop compensators, increases the bandwidth, and can be used to limit the FC current in order to not exceed the maximum output current of the FC.

4.3 Two Loop Controller design

As mentioned earlier, since the FBCFC exhibits an RHPZ is a common feature of all current fed converters, a two-loop current mode controller is required [78,133]. This controller has two loops:

1) Inner loop: Current control loop which is a fast loop.

2) Outer loop: Voltage control loop which is a slow loop.

Setting the outer voltage loop bandwidth (BW) lower than the inner current loop makes the design of two-loop controller easier and it will be discussed when the loops are separately designed. This design method is useful in fuel cell applications. Fuel cells are very sensitive to output current ripples. For stable and continuous operation of the fuel cells and converter, the input current should be controlled to be dc, which requires that bandwidths of voltage and current loops are separated far apart with a slow voltage loop and a fast current loop.

4.3.1 Current Loop design

The design of current loop, shown in Fig. 4.3, involves defining the current loop quantitatively and should meet the design criteria of phase margin (PM) and BW or crossover frequency f_c. The inductor current is fed back to the controller with the gain of *Hi(S).* Current loop compensator output is compared with modulator to obtain the appropriate duty ratio for the gating signals of the converter devices.

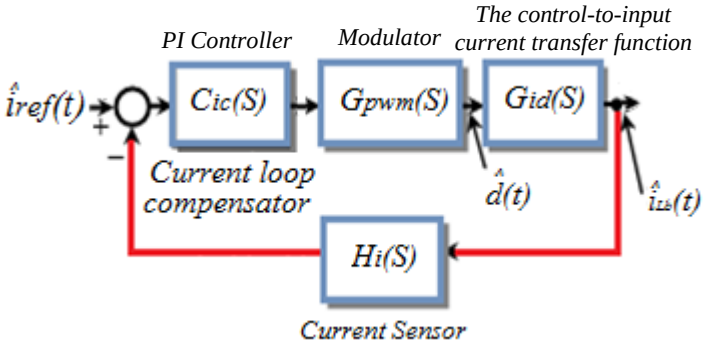


Fig. 4.3 Inner current control loop

The inner current loop (higher BW) has fast dynamics and outer voltage loop (low BW) has slow dynamics. Therefore, the inductor currents are able to change more quickly than the output voltage owing to the existence of time scale separation between the two loops or state variables. This can be exploited to simplify the controller design.

4.3.2 Voltage Loop Design

The outer voltage control loop, shown in Fig. 4.4, generates the inductor current reference i_{Lref} for the inner current control loop. Assuming 100% efficiency, the feedback gain of the voltage loop is set to 1.0. Voltage control loop provides the reference signal for the inductor current. The feedback signal is fed through the voltage gain sensor and compared with the reference voltage $v_{ref}(t)$ to produce error signal to be compensated by the voltage loop compensator to generate the inductor reference current i_{Lref}.

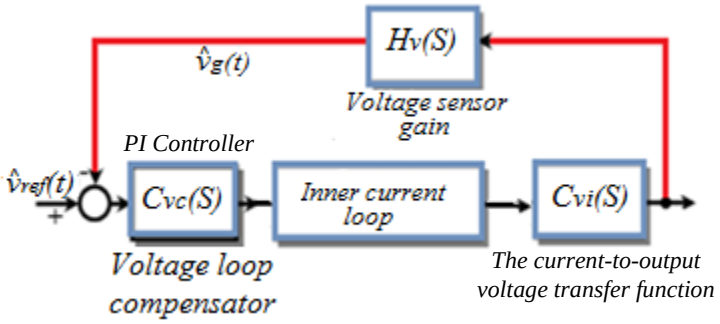


Fig.4.4 Voltage control loop using controller

The current inner loop can adapt the current errors faster than the outer loop. However, the outer loop transfer function undergoes the reference generated by voltage loop. This leads to disregarding the dynamics that govern the inner current loop when designing voltage loop. Fig. 4.5 shows the two loop average control system. Two digital PI compensators have been used and their parameters are tuned based on the transfer function derived in [97].

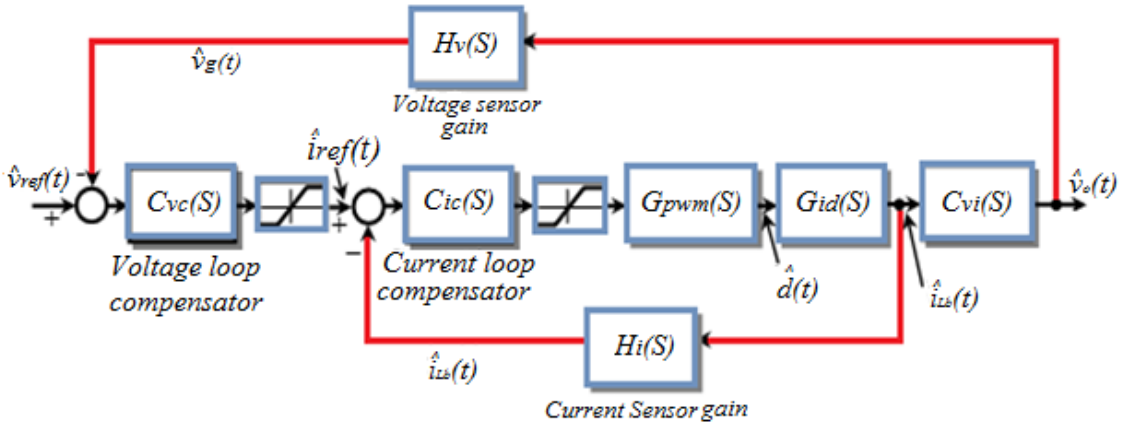


Fig. 4.5 Two loop average control system

As shown in [78], the small signal transfer functions between the boost inductor current and the duty ratio *d:*

$$G_{id}(s)=\left.\frac{\hat{i}_{Lb}(s)}{\hat{d}(s)}\right|_{\hat{v}_{fc}(s),\hat{v}_o(s)=0}=G_{io}\frac{a_o s+1}{b_1 s^2+b_2 s+1} \tag{4.3}$$

Where $G_{io}=(g_3V_{Ca}-D'g_1)/(D')^2$, $a_o=V_{Ca}.C_a/(g_3V_{Ca}-D'g_1)$, $b_1=L_bC_a/(D')^2$, and $b_2=L_bg_3/(D')^2$ [See Appendix C for full parameters description].

The transfer function between the output voltage and the boost inductor current can be obtained as follows:

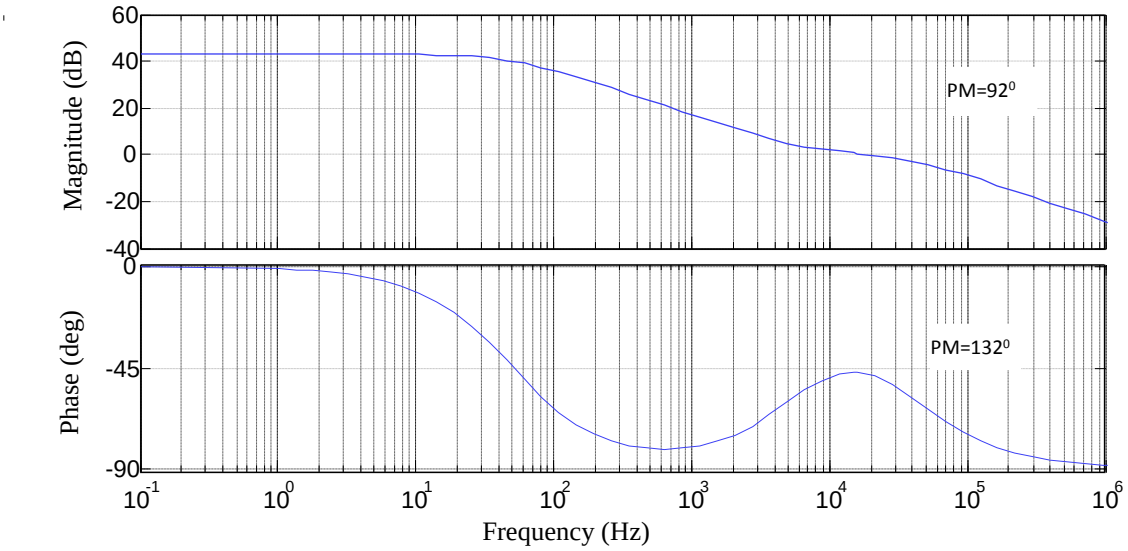
$$G_{vi}(s)=\left.\frac{\hat{v}_o(s)}{\hat{i}_L(s)}\right|_{\hat{d}(s),\hat{v}_{fc}(s)=0}=G_{vo}\frac{1}{\kappa s+1} \tag{4.4}$$

Where $G_{vo}=JR_o$ and $k=CR_o/2$

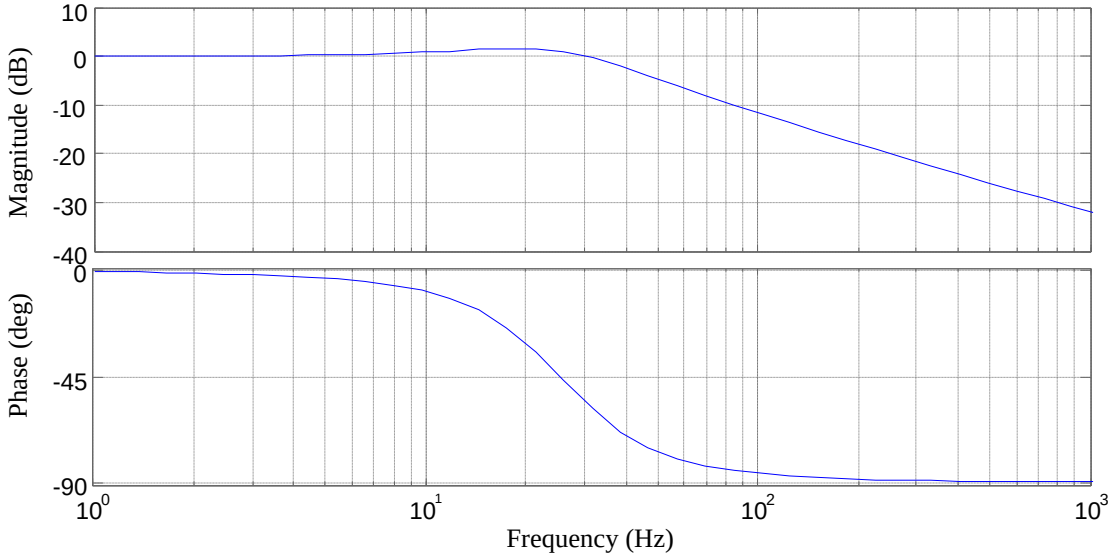
The proposed FBCFC was designed for the lowest RHPZ of 151/s, which occurs at full load. The other specifications are selected as shown in table below:

V_{fc}	V_o	L_b	$C_1=C_2$	C_a	L_{lea}	P_o	f_s	n
43-26 V	650 V	475µH	500µF	10 µF	2µH	1.2kW	20 kHz	7.4

The Bode plots of $G_{id}(s)$ and $G_{vi}(s)$ are shown in Fig. 4.6, where PM is the phase margin.



(a)



(b)

Fig. 4.6 Bode plots of the two transfer functions (a) Inner loop and (b) Outer loop

For the inner current loop, the cross-over frequency (f_c) of the open loop transfer function $T_i(s)$, was selected as one tenth of f_s which is equal to 5 kHz. The cross-over frequency for the open-loop transfer function $T_v(s)$ of the voltage controller was chosen much smaller than $T_i(s)$, since the slew rate of boost inductor current is significantly higher than the rate of i_{ref} [16]. The cross-over frequency for $T_v(s)$ is selected equal to one third of that of the RHPZ frequency. The open loop transfer functions $T_i(s)$ and $T_v(s)$ are equal to:

$$T_i(s) = H_i(s).C_{ic}(s).G_{id}(s).G_{pwm}(s) \quad (4.5)$$

$$T_v(s) = H_v(s).C_{vc}(s).G_{vi}(s) \quad (4.6)$$

The overall open loop control transfer function of circuit $T_{op}(s)$ is given by (4.7). Fig.4.7 illustrates the Bode plot of $T_{op}(s)$ where PM is equal to 57.3 at the chosen f_c.

$$T_{op}(s) = T_v(s) \times \left(\frac{C_{ic}(s).G_{id}(s).G_{pwm}(s)}{1 + T_i(s)} \right) \quad (4.7)$$

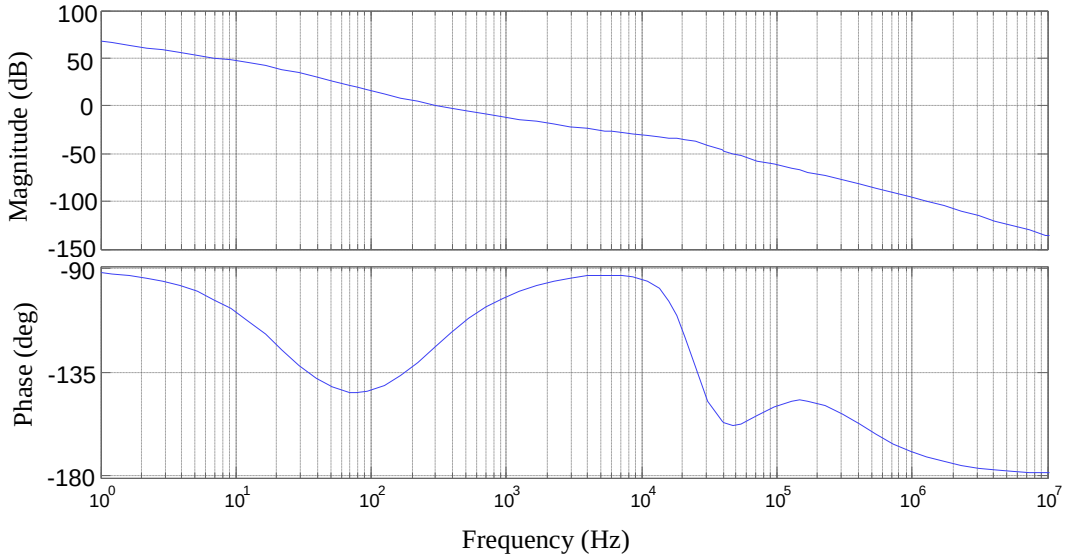


Fig. 4.7 Bode plot of open loop transfer function $T_{op}(s)$

The Control and Estimation Tools in Matlab[3] [134] were used to find the optimum structure and parameters values for the outer voltage loop compensator C_{vc} and the inner current loop compensator C_{ic}. These are given in (4.8) and (4.9) respectively:

$$TC_{ic}(s) = K_p + \frac{K_i}{s} = 4.84e\text{-}05 + \frac{0.1828}{s} \quad (4.8)$$

$$TC_{vc}(s) = K_p + \frac{K_i}{s} = 0.01895 + \frac{0.349}{s} \quad (4.9)$$

[3] The Control and Estimation Tools in Matlab provides several tools and commands for tuning PID controllers. It is automatically tunes both SISO and MIMO compensators. It can tune gain-scheduled controllers and specify multiple tuning objectives, such as reference tracking, disturbance rejection, and stability margins. The design can be validated by verifying overshoot, rise time, settling time, gain margin and phase margin [134].

The linearized system in Fig.4.5 was simulated in Matlab and step load changes were applied[4]. Fig.4.8 shows the linearized system blocks in Matlab Simulink. The time response results for both the output voltage and the input current are shown in Fig.4.9.

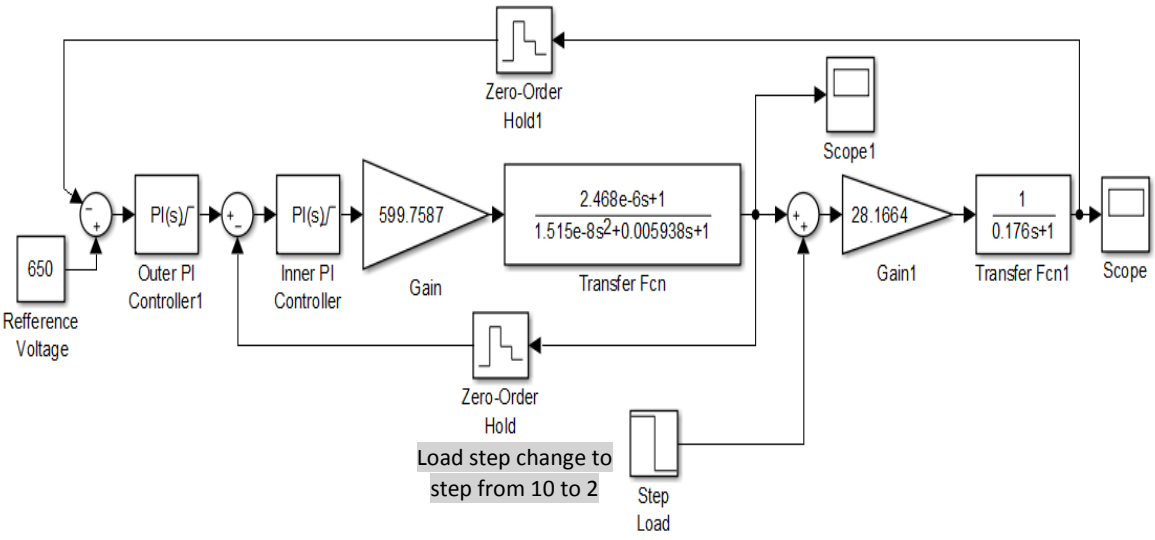


Fig. 4.8 Control block diagram of double-loop controller using Matlab Simulink

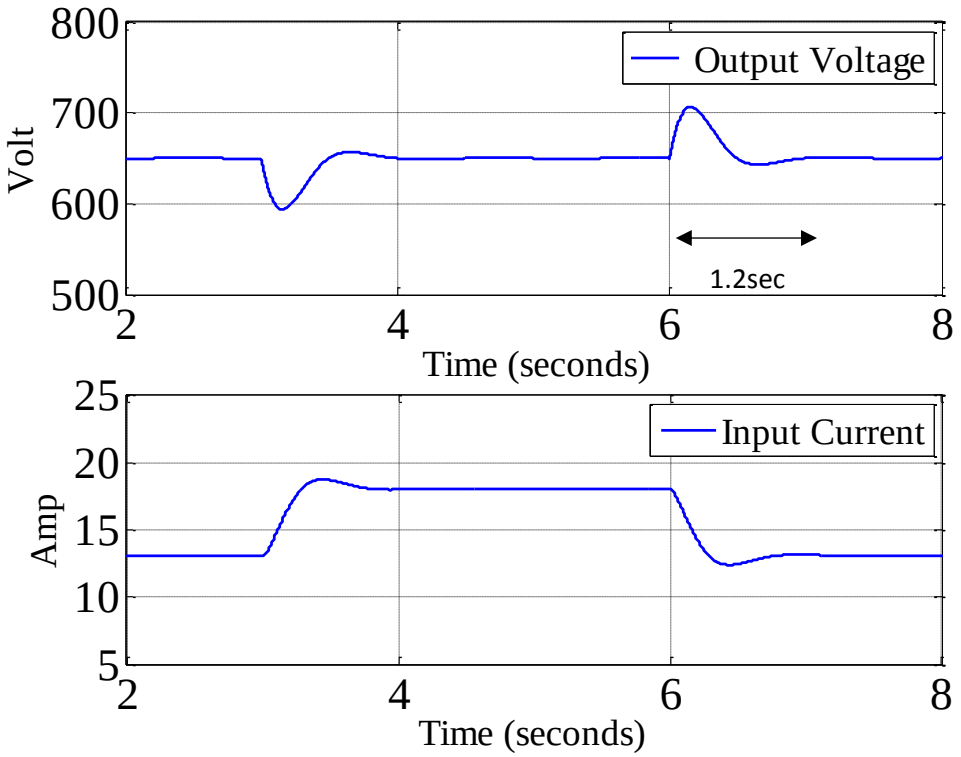


Fig. 4.9 Converter time response to load changes (applied after 3sec and removed after 6sec) using Matlab simulation of the system in Fig.4.5

[4] By using a Timer block in Fig. 4.8 to impose a load disturbance, the dynamic performance of the converter was measured.

The PI controller was designed in the S domain because the dSPACE cannot work with the discrete system (Z domain), so all the gain values were driven into the S domain. First of all, the auto tuning tool has been used in Matlab which gave the appropriate gains for the controller. By fixing the inner loop PI controller gain values (kp=0.0609, ki=154.6639) for a fast response with a settling time equal to 0.00109 sec and a rise time equal to 0.00035 sec. The PI of the outer loop controller was thus auto tuned in Matlab. Although the tuned values gave acceptable transient response, the startup current was so high that could exceed the fuel cell rated current. Fig.4.10 shows different voltages measured with different gain sets in Matlab using linearized system model.

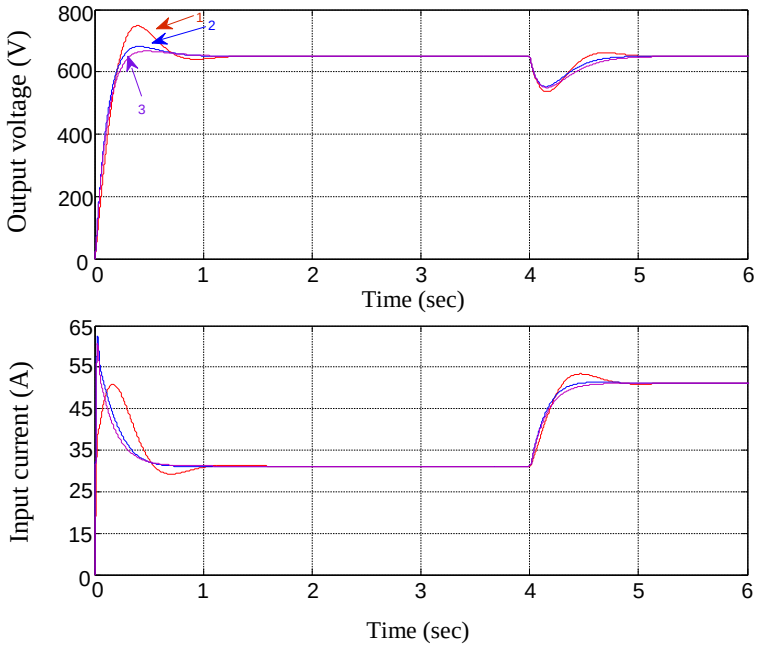


Fig. 4.10 Simulation results for different gain sets for both the output voltage and the input current: 1- Kp=0.8, ki=3.8, 2- kp=0.83, ki=5.4, 3- kp=0.8, ki=2.4

It can be seen from Fig.4.10, the gain values that give a minimum voltage overshoot at the output lead to a higher current at the input. This result is based on linearized model of the converter, and for the real system the higher current should not exceed the FC rated (60A). Fig. 4.11 shows a practical test that was carried out using a standard voltage source with the current limiter set to 60 A (FC rated).

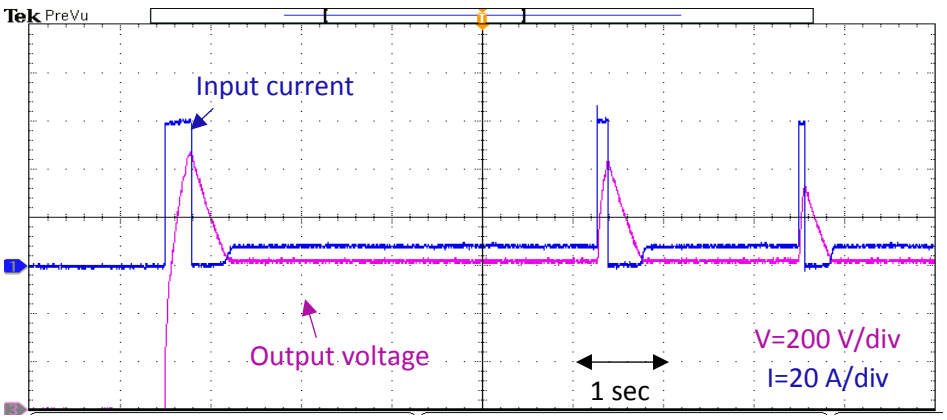


Fig. 4.11 Start-up test using a standard power supply with a current limiter (60 A) with the set gain values number (3) of the controller gains in Fig.4.10

It can be seen from Fig.4.11 that fast response of the controller causes the DC power supply to go in and out of current limit repeatedly. Hence, a new set of controller parameters leading to slower response was required. Another tuning for the outer loop PI controller setting has been carried out so that to create a state of tradeoff between the voltage overshoot and the minimum current value at the startup which should not exceed the rated current of the FC (60 A). The PI controller gain values was chosen as kp=0.04088, and ki=0.49354. Fig. 4.12a provides comparison between the previous controller gain settings and the new ones and Fig4.12b shows the transient behaviour of the system from the start-up for the PI voltage controller gains (kp, and ki) for the values in table 4.2.

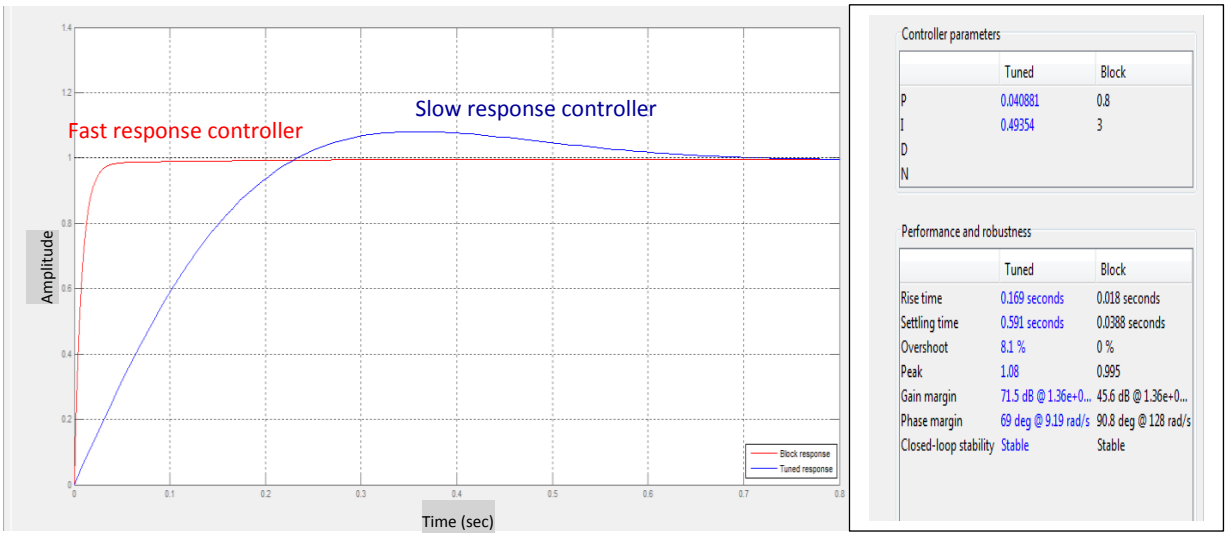


Fig. 4.12a Comparison to previous controller gain settings and the new ones

Table 4.2 comparison between different tuned gain values for the controller gain set up

	Kp_v	Ki_V	Rise time (sec)	Settling Time (sec)	Over-shoot %	Peak	Gain Margin	Phase Margin	Closed loop stability
1	0.001	0.34899	0.185	1.48	31.4	1.31	20.8DB@ 24.6rad/s	37.8 deg@ 6.48rad/s	stable
2	0.019777	0.31743	0.222	0.761	11.1	1.11	34.2db@ 132rad/s	60 deg@ 6.4rad/s	stable
3	0.040306	0.27628	0.258	0.403	0.873	1.01	28.8db@ 138rad/s	81 deg@ 7.01rad/s	stable
4	0.039535	0.22986	0.317	0.563	0	1	29.1db@ 139rad/s	86 deg@ 6.4rad/s	stable
5	0.024649	0.13846	0.562	1.01	0	0.999	76.5db@ 329rad/s	90 deg@ 3.91rad/s	stable

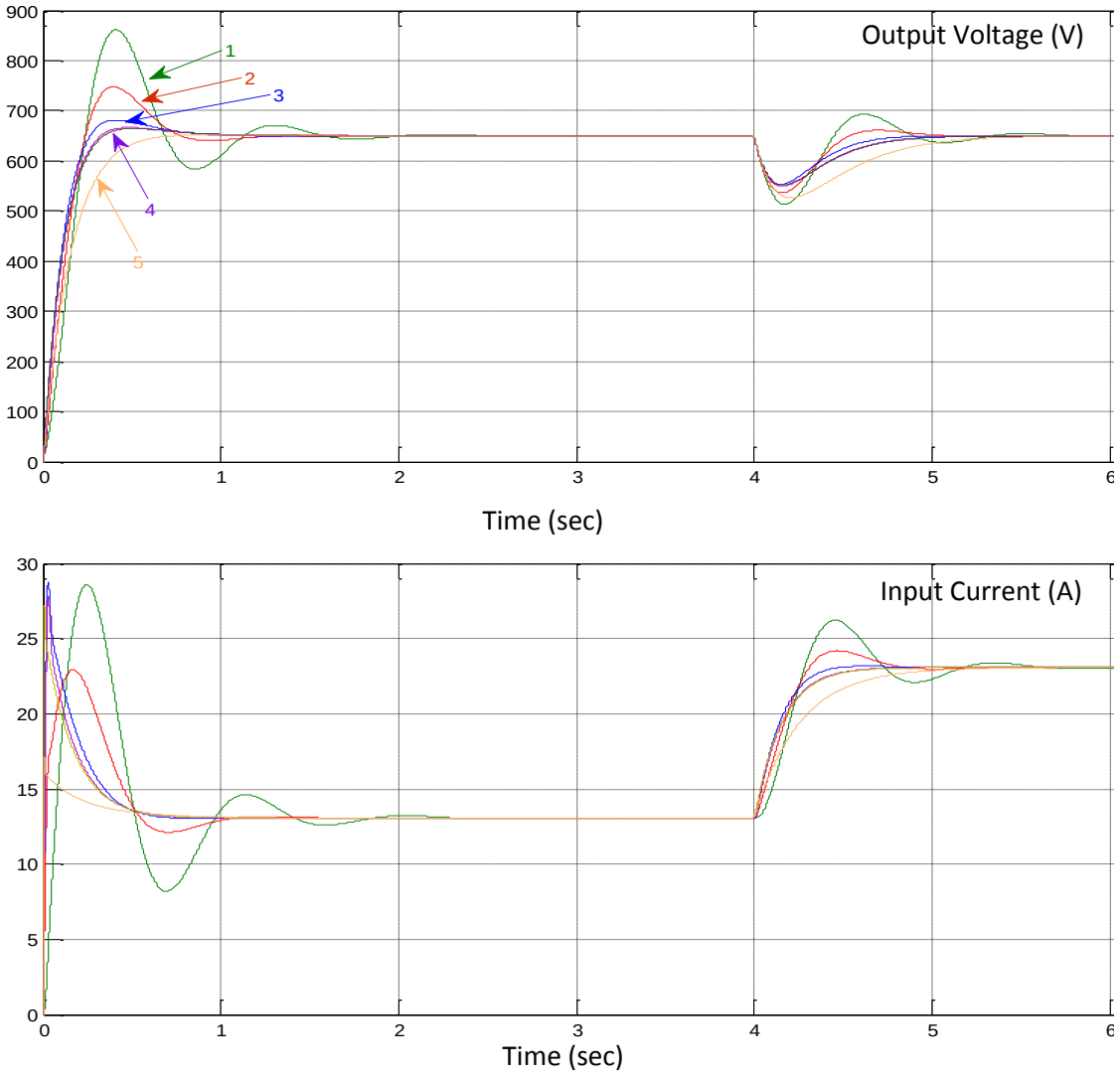


Fig.4.12b Different time response for the tuned gain values for the controller gain set up in table 4.2

By using the auto-tuning method, the gain values for the controller has been chosen. As the inner current loop is the faster in current error correction. Therefore, in the voltage loop design, the inner current loop dynamics were neglected. By tuning the values of the controller gain for better response. The appropriate gain value was selected for the faster settling time, which was a trade-off between the overshoot and the settling time, as can be seen from table 4.2. However, simulating the small-signal transfer functions does not take into account the non-linearity of the power electronic converter system. While this approach is helpful to give an indication of the performance for the converter, yet the results may not be accurate over the entire load range. Therefore, a further accurate full system modelling based on a physical components model has been carried out and described in the next section.

4.4 Controller Simulation Using Matlab/co-simulation (Physical Components Model Approach)

4.4.1 SLPS Interface

The PSpice software is very suitable for simulating power electronic circuits that contain switching devices and non-linear elements. But it is less preferable for control system simulation because of the potential convergence difficulties. In addition to this, simulating the control system in PSpice may require a large amount of time for analysis. On the other hand, Matlab/Simulink is a very powerful program for control engineering, but it is less suitable for accurate modelling of power electronic circuit characteristics. SLPS interface is used to overcome these problems.

The SLPS is an interface tool between The MathWorks' MATLAB/Simulink system simulator and the PSpice A/D electric circuit simulator. Using SLPS, a PSpice electrical circuit was inserted into Simulink models. Hence, a system model and electric circuit model were joined together, which were previously handled separately. This system provides a modelling environment that combines the advantages of each of the simulators

and ensures that the system models are very close to reality with a high level of accuracy [135].

Fig. 4.13 shows a block diagram of the basic operation of the SLPS system. This structural design explains how the data is exchanged between the PSpice model and the control system in Matlab Simulink.

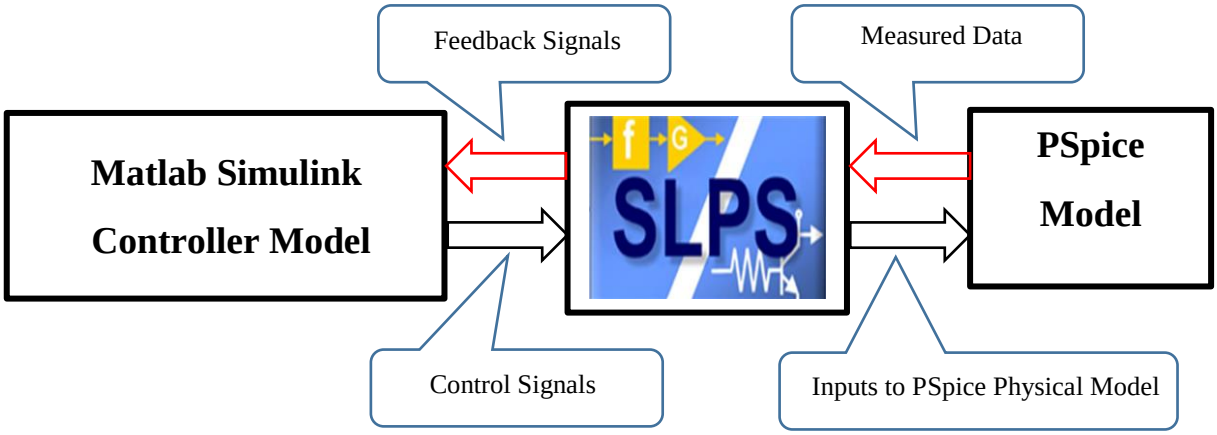


Fig. 4.13 Block diagram of the basic operation of the SLPS system

To evaluate the control algorithm before applying it to the real converter, a new validation approach has been developed based on SLPS. The complete model of the FC converter system with the digital controller structure is shown in Fig. 4.14, where it can be seen that the PCM of the converter (see Fig. 3.11) has been modelled in PSpice and embedded in the Simulink model, as a sub-circuit block via the SLPS software. A PWM generator has been designed that generates switching signals for the bridge switches as well as the clamp switch with only one modulating signal of 20 kHz as shown in Fig.4.15.

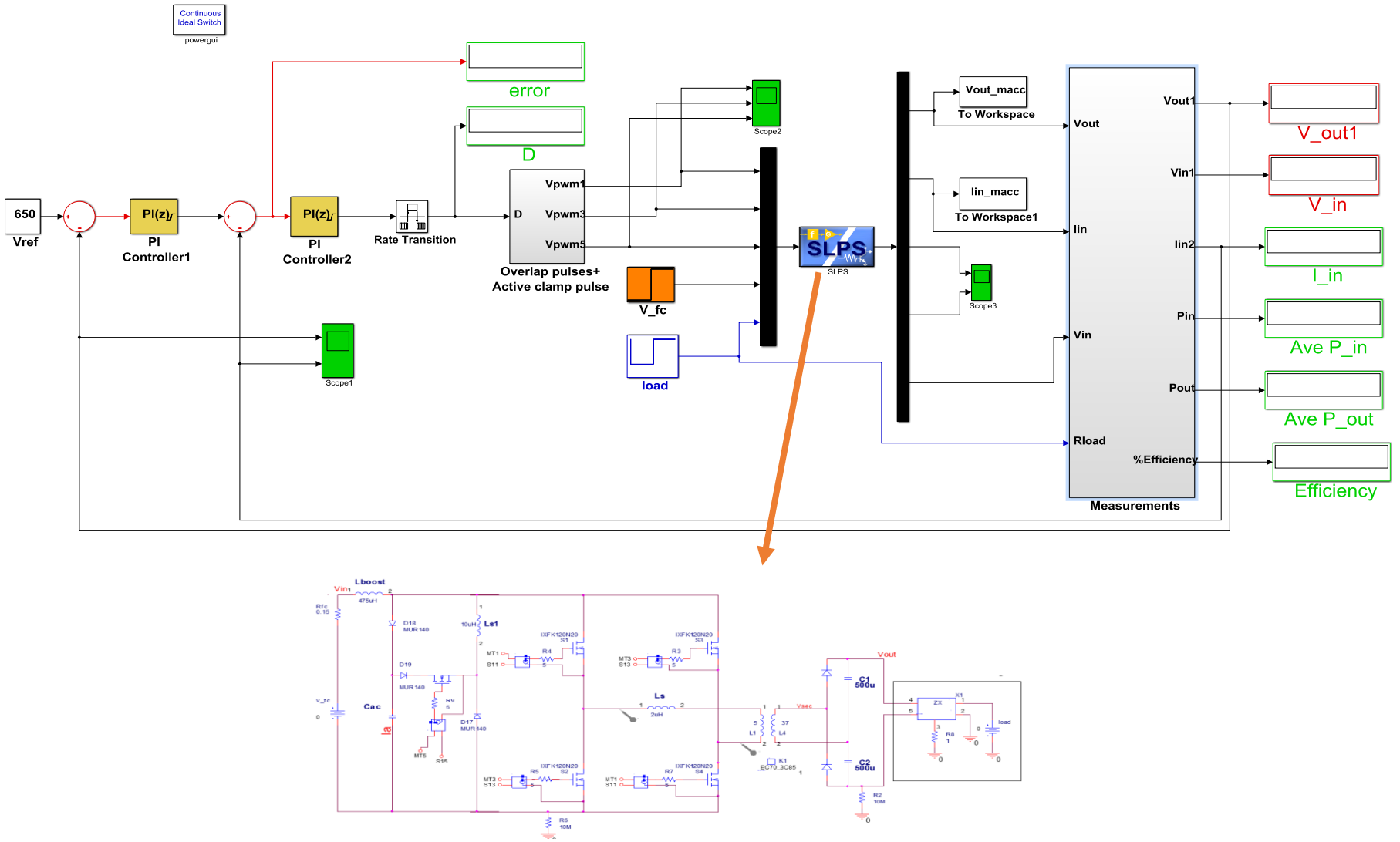


Fig. 4.14 Digital controller block diagram in Simulink integrated with the PCM of the converter via SLPS

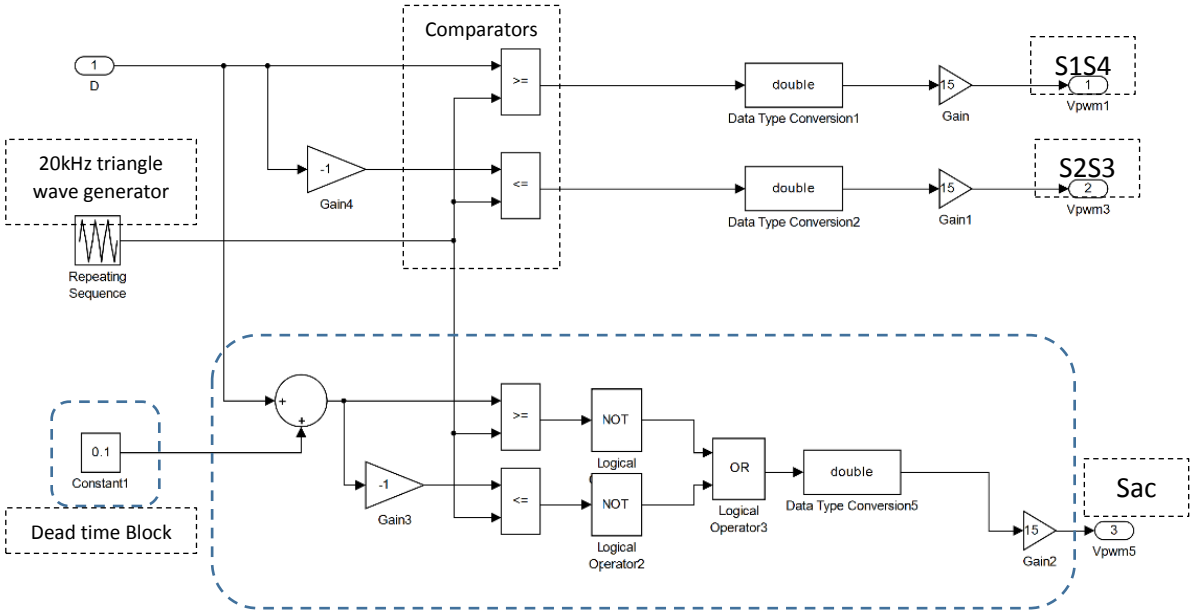


Fig. 4.15 PWM generating circuit in Simulink for the CFC devices

Fig. 4.16 shows the difference in dynamic response of the converter using the Matlab transfer function model and the co-simulation model when the output power changes from 500 W to 200 W. While the rise and fall times of the waveforms are very similar, it can be seen that the Matlab model cannot compensate for the non-linear characteristic of the physical converter, which experiences larger current changes and voltage deviations.

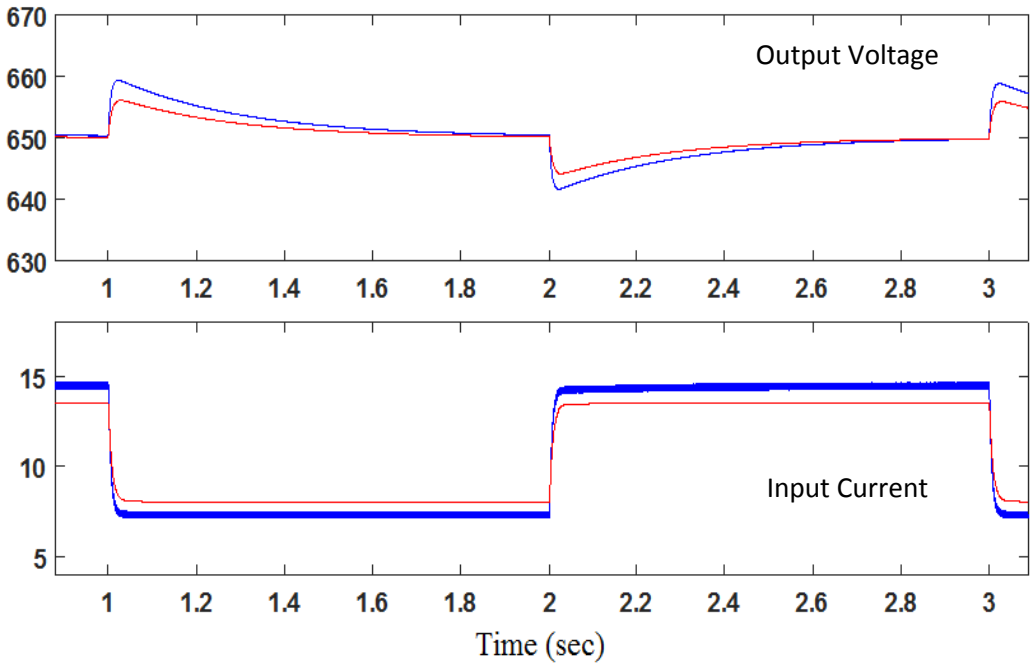


Fig. 4.16 Step response to load changes; red: transfer function model; blue: physical model

The transfer functions (4.3 and 4.4) were originally derived for the converter with a CACC, while the simulation results in Fig. 4.16 are with the MACC. It can be seen from Fig. 4.16 that the step responses obtained through SLPS co-simulation confirms those of the full system based on the small signal model with a closed-loop control approach. The latter motivates confidence that the active clamp modification has not made much impact on the converter dynamics. Furthermore, the results prove the validity of the approach in designing the closed-loop controllers. However, Fig. 4.16 show a slight difference between the simulation results of the small-signal mathematical model approach and the SLPS co-simulation approach. The main reason for this is the simulation results of the SLPS co-simulation uses accurate models of the power converter components in the PSpice model with a nonlinear behaviour of the passive components and active switching devices. The latter would be difficult to incorporate in detail in the mathematical dynamic model of the power converter. Therefore, the benefit of the SLPS co-simulation approach is that the modelled performance of the converter will closely resemble an actual converter circuit.

Fig.4.17 shows the response of the converter co-simulation model (physical model) when the output power changes with different load steps. The physical model uses accurate models of the components supplied by the manufacturers.

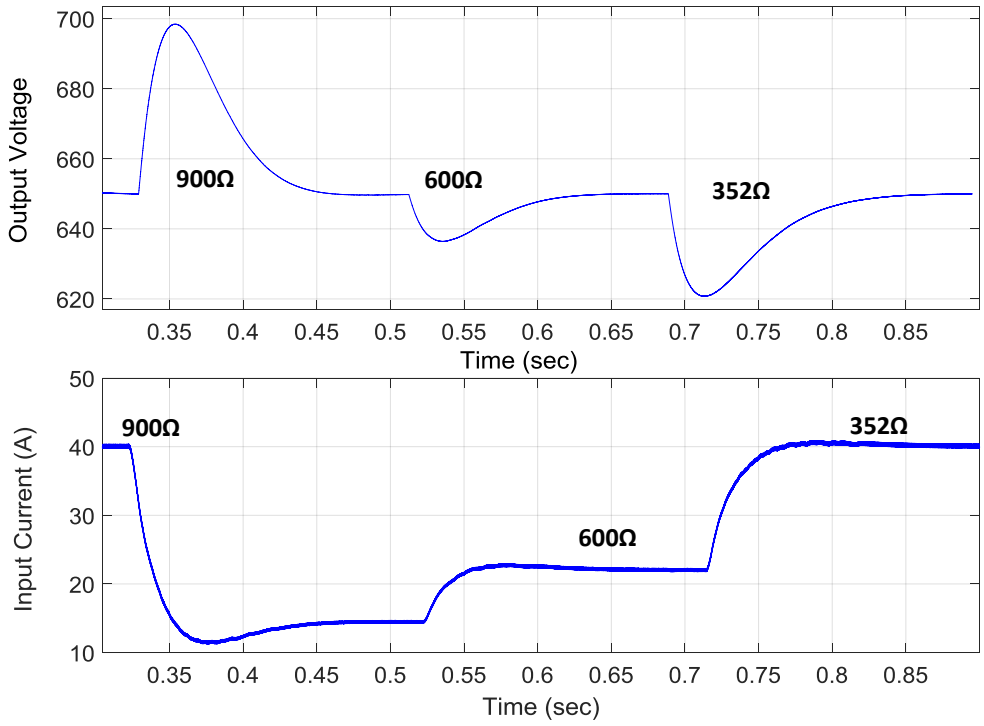


Fig. 4.17 Step response to load changes using physical model

Fig.4.18 shows the converter output voltage for different step load changes for the converter combined with the CACC (Red) and the MACC (blue).

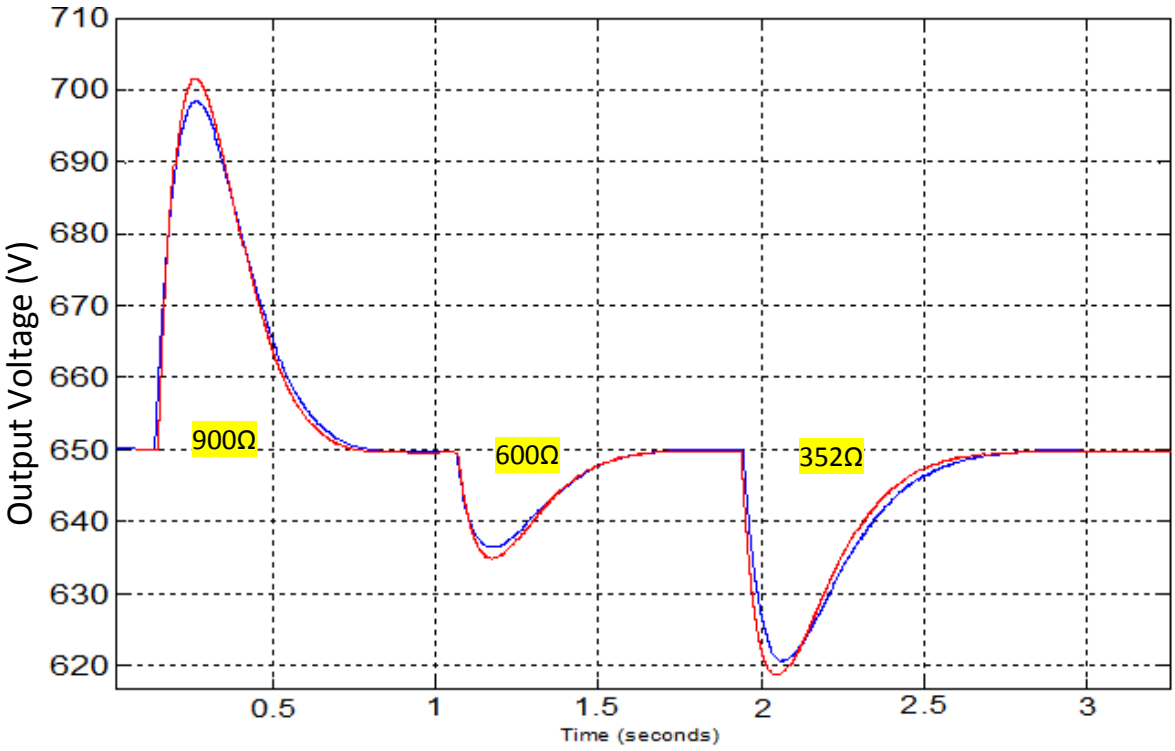


Fig.4.18 Time response comparison (the converter output voltage) between CACC (Red), and MACC (Blue) during different load change (352Ω (full load), 900Ω, 600Ω, 352Ω)

The results in Fig.4.18 were taken using the co-simulation model in Fig.4.14. It can be seen that there is a very small difference in the time response of the converter when using the both active clamp circuits. This implies that the MACC has little or no effect on the dynamics of the converter. This result enhances the confidence in using the software packages in designing the closed loop controller before the laboratory implementation.

4.5 Controller Implementation

4.5.1 Real Time Control Preparation

The closed loop controller was designed, simulated using Matlab and Pspice software, and was implemented using the dSPACE (DS1103). The dSPACE generates the PWM signal for the MOSFETs gates of the FBCFC converter. Inputs/ outputs from the DS1103 pass through the CLP1103 connector panel board to the computer. Fig. 4.19 shows the block diagram of the hardware setup.

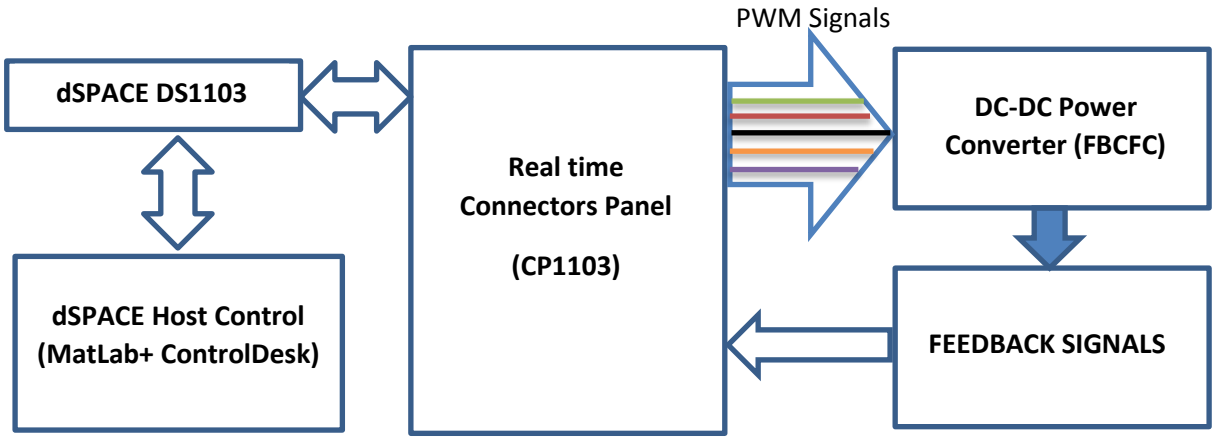


Fig.4.19 Block diagram of hardware setup

The CLP1103 serves as an interface between the DS1103 and the external hardware portion of the overall system. The CLP1103 contains connectors for twenty Analogue-to-Digital inputs, eight Digital-to-Analogue outputs, and several other connectors that can be used for Digital I/O, slave/DSP I/O, incremental encoder interfaces, Controlling Area Network (CAN) interface and serial interfaces.

In order to implement the controller, a feedback signal was required for both the input current and the output voltage. An existing Signal Processing Board (SPB) was tested to

be used with the FBCFC control system. Fig.4.20 illustrates the circuit diagram of the existing SPB. Fig.4.21a demonstrates the full printed circuit of the SPB, and Fig.4.21b depicts the signal processing board equipped with the converter circuit. As can be seen from the circuit diagram in Fig.4.20 the circuit has two voltage inputs and one current input. For the two-loop controller, the output voltage and the input current will be only controlled in such a way that one of the inputs of the circuit will not be used. The circuit in Fig.4.21a has been tested and calibrated to give 5V out for 750V which will be used with the BDC circuit in the future work.

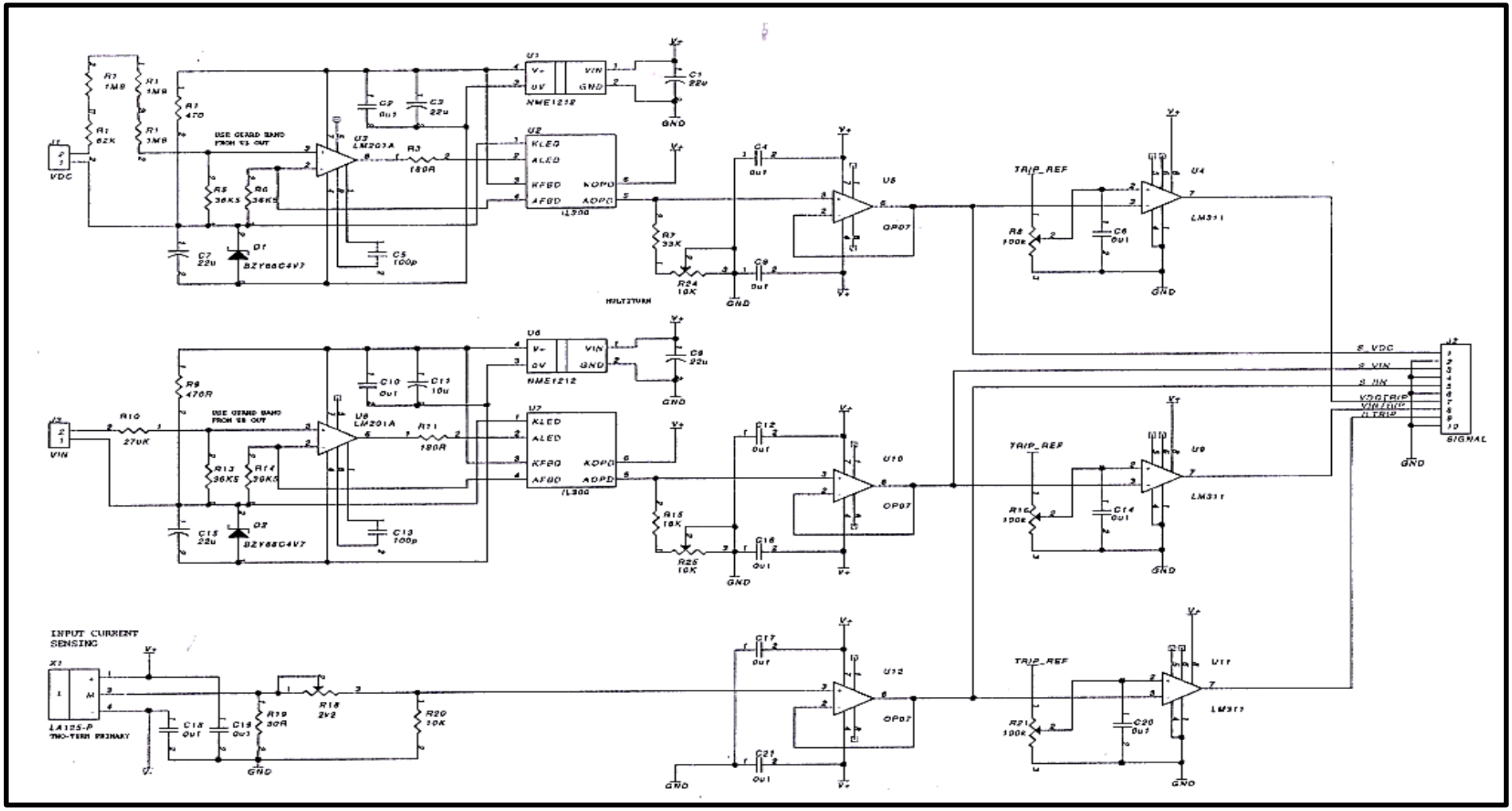
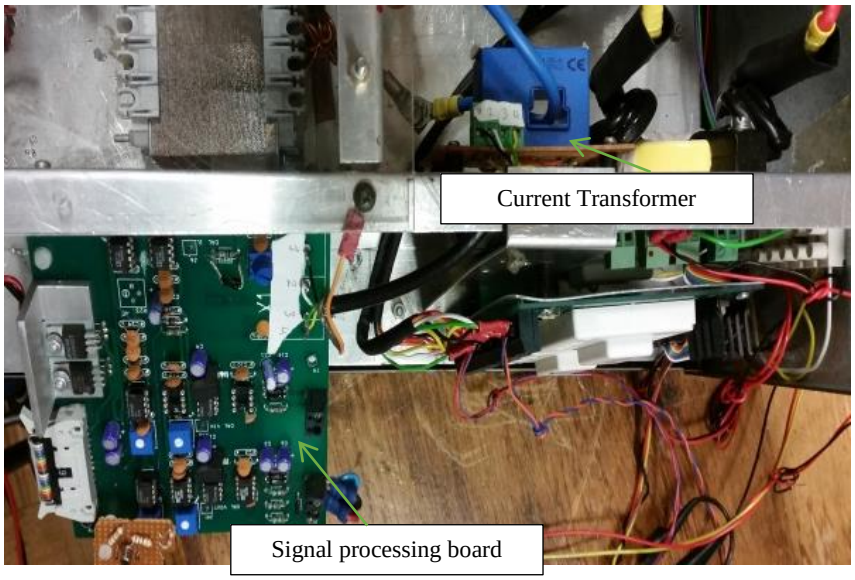


Fig.4.20 The existing signal processing measurement board

(a)



(b)

Fig.4.21 The printed circuit of the signal processing board

As the dSPACE was used to control the CFC, another test was implemented using the SPB which was already equipped with the converter circuit as shown in Fig.4.21b. The output signals were taken from the SPB to the dSPACE kit connector, then to the ADC block in Matlab Simulink. The test shows that the SPB was calibrated to give 2V of DC voltage for 650V dc output (rated voltage of the DC bus), and 3.32 volt for 60A input current (FC rated current).

4.5.2 Controller Implementation using dSPACE

The designed closed-loop controller was implemented using the dSPACE DS1103 board and interface. The dSPACE kit also generated the PWM signal for the gates of the MOSFET switches in the FBCFC converter. Fig.4.22 shows a diagram of the implementation using dSPACE [see Appendix D].

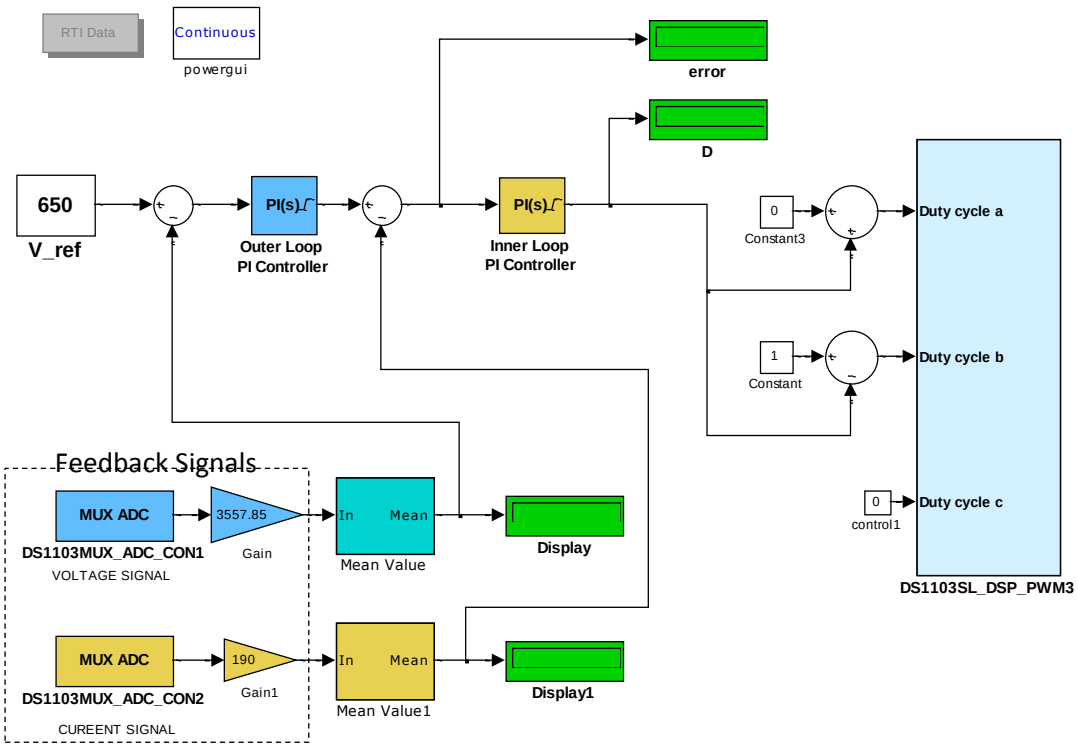


Fig.4.22 Controller Implementation using dSPACE

As can be seen from Fig.4.22, the feedback signals are fed from the converter to the dSPACE through the MUX ADC blocks (CON1 for voltage signal, CON2 for current signal). These signals were originally fed from the converter and rescaled from the converter rated voltage and current using the SPB circuit in Fig.4.21 and rescaled again using the gain blocks (Gain, and Gain1) in dSPACE. As this controller is a two loops controller, the outer loop PI controller block was used for the output voltage control and the inner loop PI block was used for the input current control. Then the output signal of

the PI inner loop block was fed to the DS1103SL_DSP_PWM block that generates the required pulses for the converter devices. The controller circuit runs by activating the Build command in Matlab which generate the c code required to control the converter [Appendix E].

The experimental set-up in the laboratory is depicted in Fig.4.23 which shows the FC connected to the converter and controlled by dSPACE.

Fig. 4.23 Experimental set-up of the FC and the FBCFC in the laboratory (see Fig.3.38 for the block diagram of the test arrangement)

4.6 Dynamic Response

Fig.4.24 shows the time response of the converter for both a constant voltage source and an FC. It clearly shows that the dynamics in both sources are somewhat different. With the FC, there is less damping and a longer settling time. The higher current of the FC compared with the current of the constant voltage source is due to the voltage drop of the FC as a result of the FC internal resistance. At load application, the FC system output

voltage recovers within 1sec., but at load rejection the response of the FC system is oscillatory and takes several seconds to die away.

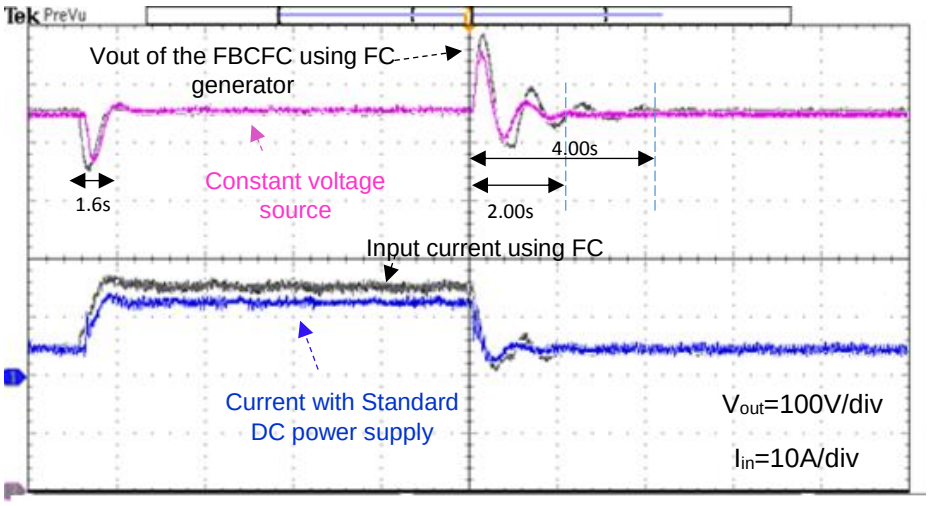


Fig.4.24 Time response for both the FC and the constant voltage source

The ripple of the input current is calculated from Fig.4.25 and it is of the order of 10% of the FC rated current which is acceptable for the FC according to the FC specification mentioned in chapter two.

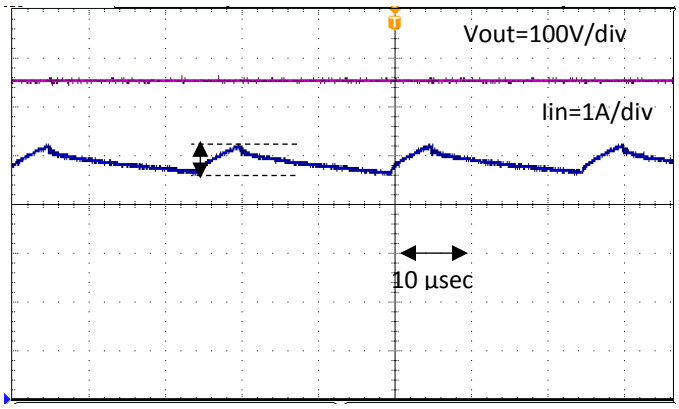


Fig.4.25 Output voltage and the input current of the converter

Fig.4.26 shows the response time of the FC converter system for a number of step changes in load. The FC output voltage changes as the load is changed because of the internal resistance of the FC (see Fig.2.3). It can be seen that the feedback controller of the converter can maintain a steady - state output voltage, but transients do occur during sudden load changes. If such deviations are not acceptable, the use of a fast-response

energy buffer (such as an ultra-capacitor) with an appropriate converter should be considered.

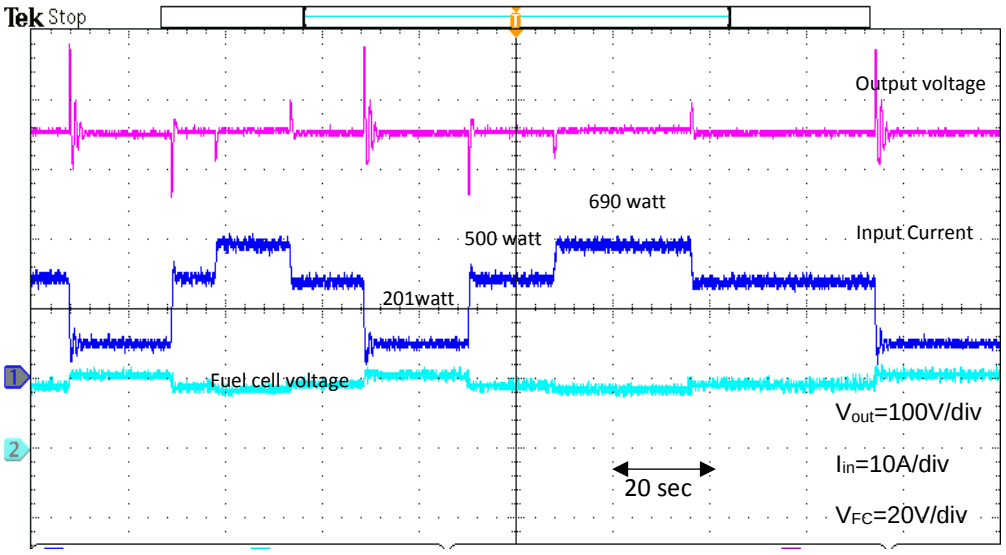


Fig.4.26 Time response for different loads set: from the top: converter output voltage, input current, and fuel cell voltage

4.7 dSPACE Control-Desk Environment

The main advantage of a real time system is the fact that the parameters of the system can be controlled during operation. In order to measure and/or modify the parameters of a model, dSPACE offers the Control-Desk program. This program reads and writes in the memory block reserved for the dSPACE processor and is able to show or change the value of every variable due to a memory map generated during the compilation of the program. Control-Desk software offers a wide range of visualization and editing tools, as for instance gauges, displays, radio buttons, graphs, level bars, etc. Fig.4.27 shows Control-Desk layout with different instruments.

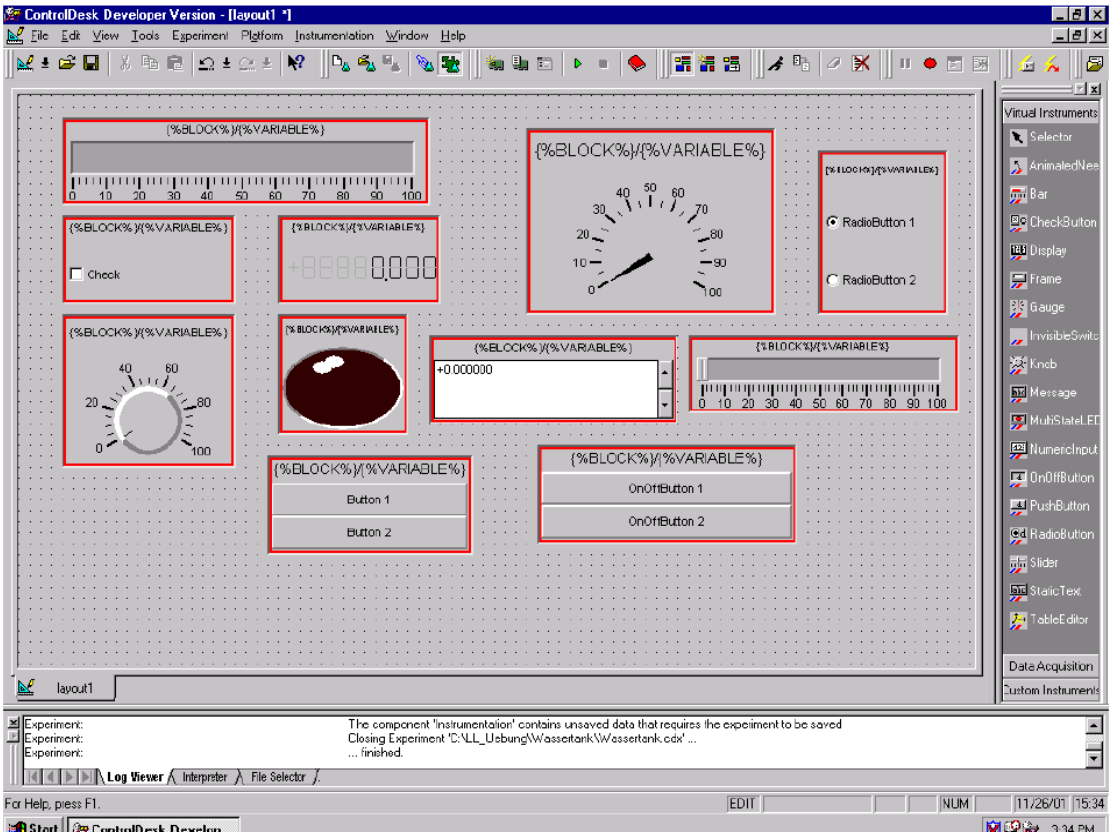


Fig.4.27 Control-desk layout with different instrument

4.8 Capture Settings Instrument

The *Capture-Settings* instrument found in the Control-Desk program which allows data output on "Plotter-Array" instruments to be saved/recorded for later analysis/use in MATLAB. For our system, the Control-Desk was used to monitor and record the converter output voltage, input current, controller error, and duty ratio. Besides, it has the ability to display the dynamic response of the converter during the load steps by using the capture instrument as shown in Fig.4.28 [136].

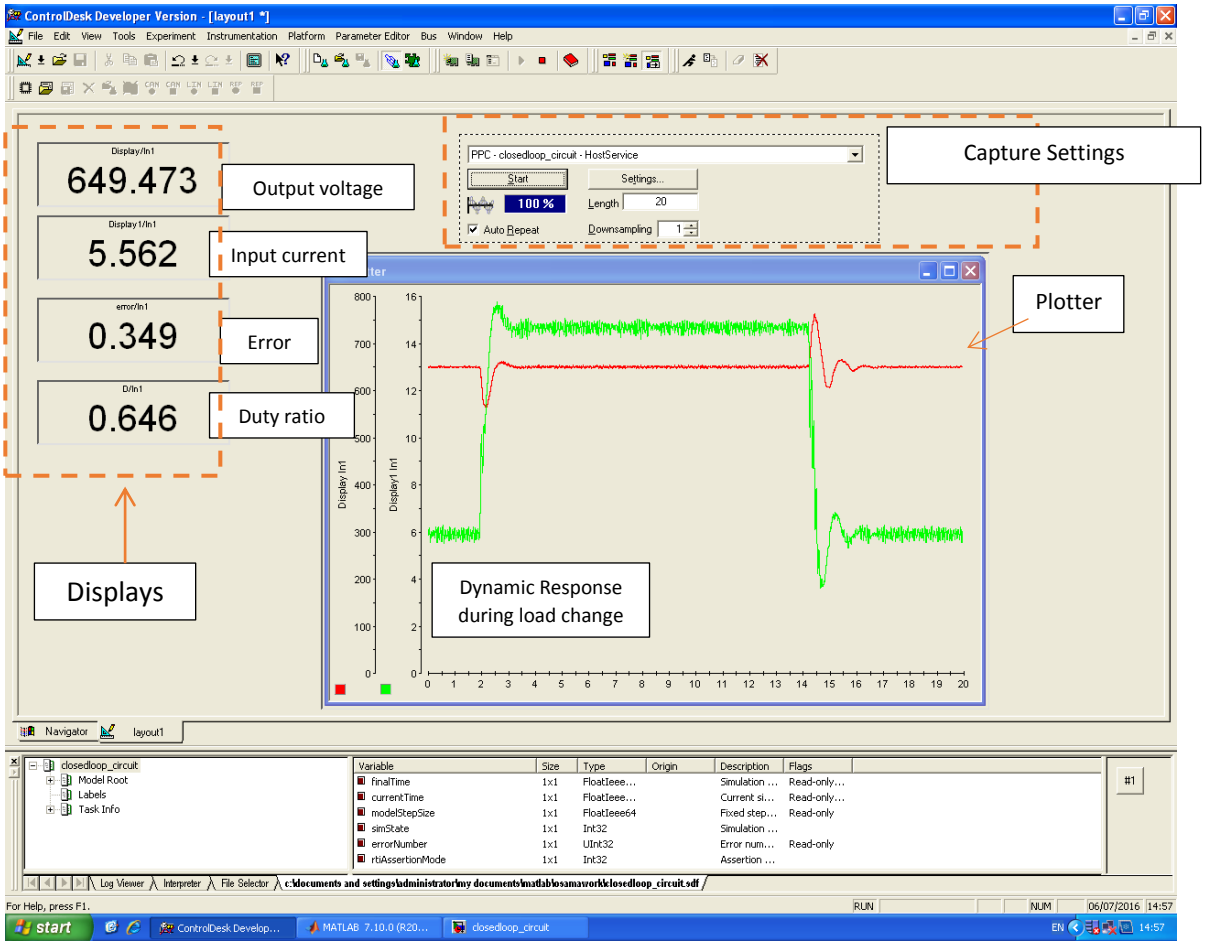


Fig.4.28 Control-Desk layout on the dSPACE PC

Fig.4.28 shows the Control-Desk windows software on the dSPACE PC host. It was especially designed for dSPACE applications. The software enables the user to record and monitor the real time variables of the converter.

The control-desk was used for monitoring and recording the converter output voltage, the input current, the controller error, and the duty ratio. Besides, it has the ability to draw the dynamic response of the converter during the load steps as shown in Fig.4.28.

4.9 Conclusion

In this chapter, a controller was designed and implemented using dSPACE. This has been confirmed by tests on a prototype converter. The results from the converter controller obtained through simulations have demonstrated the consistency of the dynamic model and the effectiveness of the SLPS co-simulation in providing an optimum method for bridging the gap between the simulation model and the final FC converter system implementation.

Time response tests have shown that the current-fed converter response to load changes is slower than the FC response. Even with a standard voltage source the response is rather sluggish. This is because of the common non-minimum-phase characteristic of this kind of converter. The non-minimum-phase phenomenon causes a phase lag at low frequencies which limits the available bandwidth for the CFC resulting in a slower dynamic response for the CFC. Based on this, it can be concluded that while the CFC is more suited for application with an FC, its slow response due to the non-minimum phase characteristic makes it less suitable for input sources with a fast–dynamic response such as the ultra-capacitor. In applications such as DC micro-grids, this slow response may not be acceptable. Therefore, a fast response energy buffer (such as an ultra-capacitor) may be required to back up the FC and improve the whole performance of the system.

Chapter Five

Chapter Five

Ultra-Capacitor Converter, Design and Control

5.1 Introduction

According to the dynamic response results of the FC/converter system (see chapter four), the FC system has a limited response to sudden load changes due to the FC and the FBCFC dynamics [26, 88]. To improve the dynamic response of a DC micro-grid and to increase the system efficiency, a fast response energy storage system such as an ultra-capacitor or battery bank is required. The latter will be responsible for supplying energy to the DC grid during short periods of time. A DC-DC converter is required to interface between the energy storage system and the micro-grid DC bus. The converter should be designed for both charging and discharging of the energy store.

A bi-directional converter (BDC) is generally needed to control the power flow between energy storage and the load while regulating the bus voltage during source and load power changes [89]. As mentioned in chapter two, an investigation is being carried out on a proposed modulation scheme that was developed (but not implemented) in [101] on a bidirectional DC-DC voltage fed converter as shown in Fig.5.1. This converter is a combination of a low voltage MOSFET H-Bridge, and a bi-directional high voltage IGBT voltage doubler circuit connected to an ultra-capacitor operating from 50% to 100% of its rated voltage (from 24V to 48V). This converter has a galvanic isolation with a high boost ratio, and bidirectional power flow. Moreover, it has a lower number of active devices at the lowest voltage rating. In this chapter, the BDC proposed in [101] will be validated by both modelling and practical implementation. The proposed modulation scheme will be verified by PSpice/Simulink using SLPS co-simulation software.

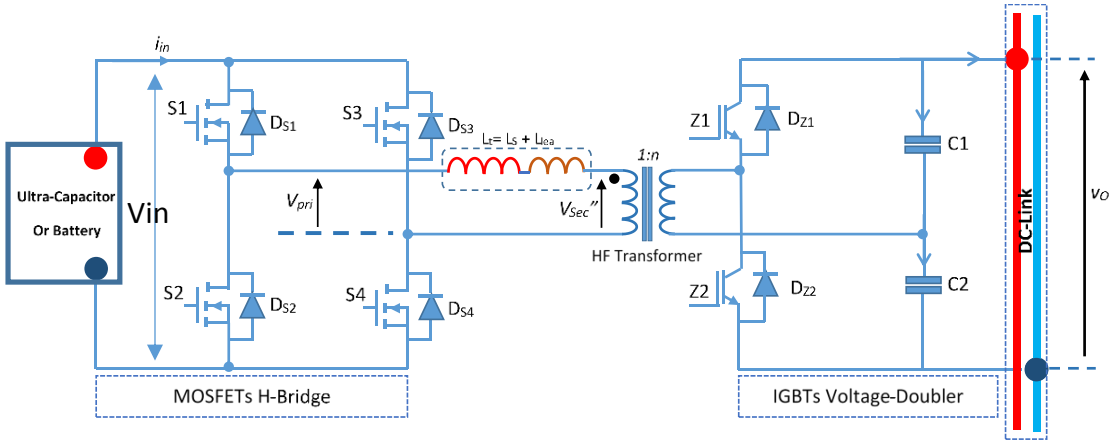


Fig.5.1. Proposed BDC

5.2 Target of the BDC Control

The UC controller was based on two main voltage levels inside the micro-grid system;

1- The bus voltage (650V)

2- The UC voltage (24-48V)

The main controller function was to control the power flow between the dc bus and the ultra-capacitor, assuring a regulated dc bus voltage on the dc grid side and managing the charging and discharging algorithm of the UC.

The controller monitors the bus voltage of the micro-grid. For any disturbance, when the grid voltage becomes greater than 650V the BDC will drain current from the dc bus to the ultra-capacitor. When the bus voltage drops below 650V the converter will deliver current to the bus, and the UC will be used as a power source.

5.3 Bidirectional DC-DC Converter Modelling & Simulation

In this section the BDC configuration of Fig.5.1 has been modelled in PSpice as shown in Fig.5.2. Fig.5.3 illustrates the required timing pulses for the converter. The firing pulses to a single bridge leg are a pair of a 50% duty cycle square wave signals that are 180^{o} offset from each other. Both the UC and the DC buses have been modelled as voltage sources.

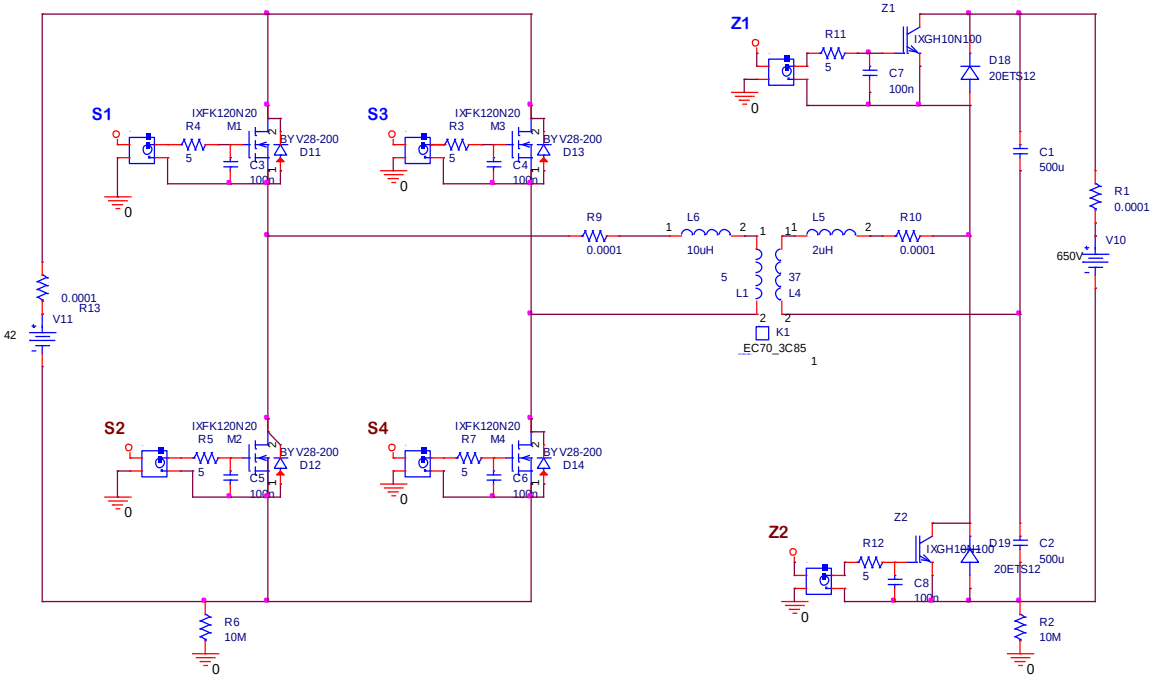


Fig 5.2. Bidirectional Voltage Fed Converter (VFC)

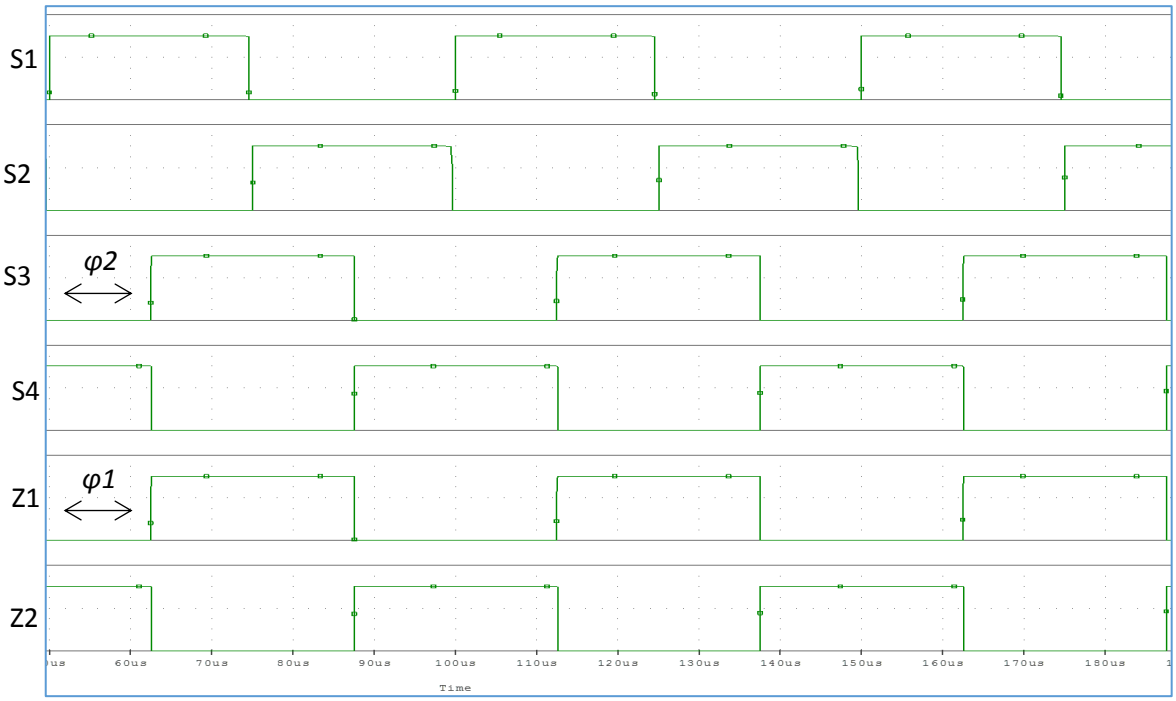


Fig.5.3. VFC timing pulses with 50% duty ratio

One of the requirements that needs to be taken into consideration for the VFC is the dead time between the timing signals of the same leg switches, because switching devices cannot be turned off with zero time due to the parasitic elements of these devices. The dead time must be set to prevent shorting the two switches in the same leg for both the

low voltage side and the high voltage side; otherwise high current spikes up to 1.8 kA can occur as shown in Fig.5.4 that will destroy the devices. However, the high current spikes can be eliminated when a suitable dead time is introduced as shown in Fig.5.5.

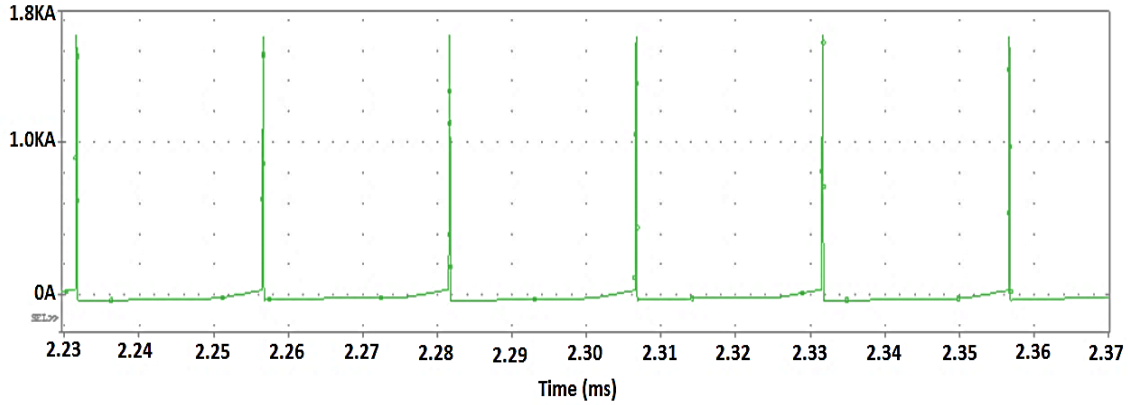


Fig.5.4. Input current spikes due to the zero-dead time

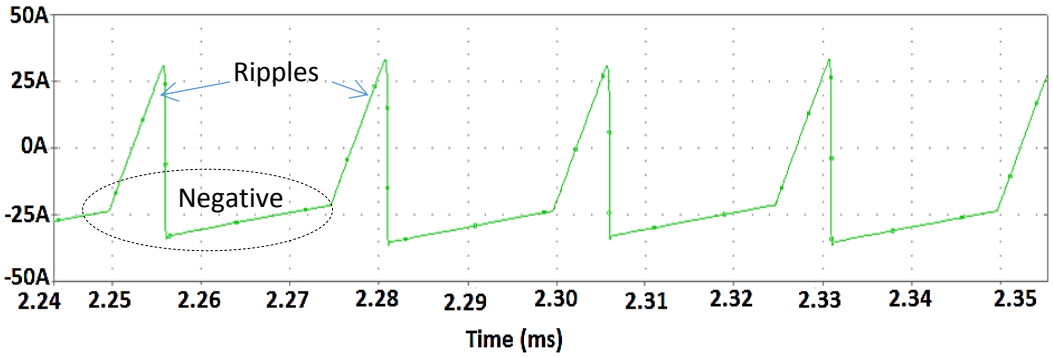


Fig.5.5 Input current due to 0.5 µSec dead time

In Fig.5.5 the input current contains a considerable ripple with a negative part which means that the current is reversed[5]. Applying the timing pulses to the primary and secondary bridges, with a phase shift between firing pulses, two square-voltage waveforms are generated at the outputs of each bridge as shown in Fig.5.6.

[5] The FC is sensitive to any current ripple since it decreases the service life of the stack and effects on the diffusion layer of the FC stack. In addition, the FC cannot accept power in the reverse direction [18]. For use with the FC the VFC, it would be necessary to use a series diode and a large capacitor at the input of the converter which will have a negative effect at the converter efficiency. Therefore, the VFC is not suitable for FC applications.

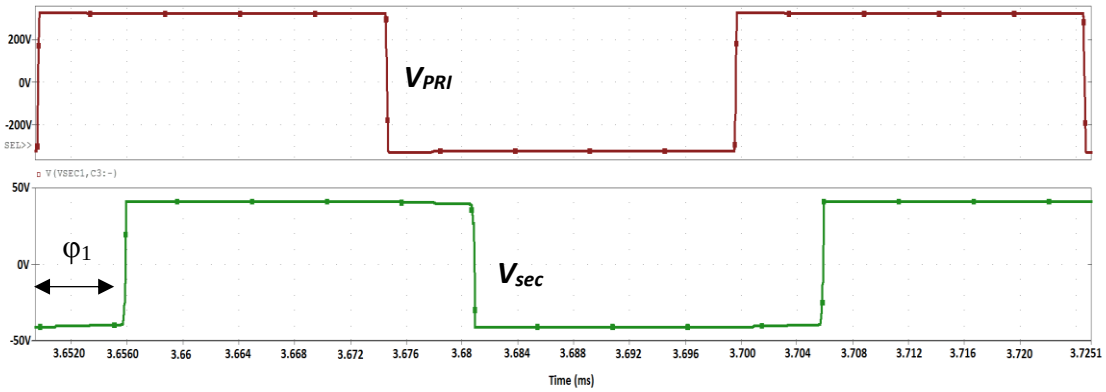


Fig.5.6 VFC voltages, from the top: primary voltage, secondary voltage

These two phase-shifted voltage waveforms in Fig.5.6, generate a non-zero net voltage V_{Lt} across the inductor L_t, resulting in a current i_{Lt} flowing through it as shown in Fig.5.7. The shape of the inductor current depends on the magnitudes of the voltages across its terminals. As can be seen from Fig. 5.7 the waveform of the primary current i_{Lt} is symmetrical, hence only the first half-cycle needs to be considered for analysis.

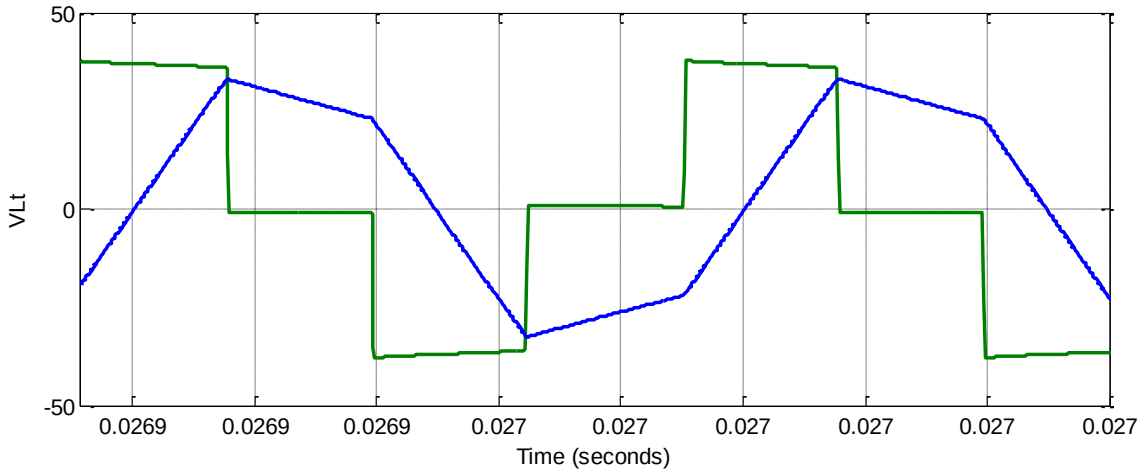


Fig.5.7 Voltage across the Inductor *Lt* (green), and the Current through *Lt* i_{Lt} (blue)

The circuit diagram of Fig.5.1 can be can be simplified in Fig.5.8. In this model, the two sides of the converter (Bridge side, and H.V. side) have been replaced by two square voltage sources. The inductor L_t represent the series inductor that is responsible for the power transferred in both directions plus the leakage inductance of the High frequency transformer. Where,

$$L_t = L_{series} + L_{lea} \tag{5.1}$$

Where, L_{lea} is the leakage inductance of the HF transformer.

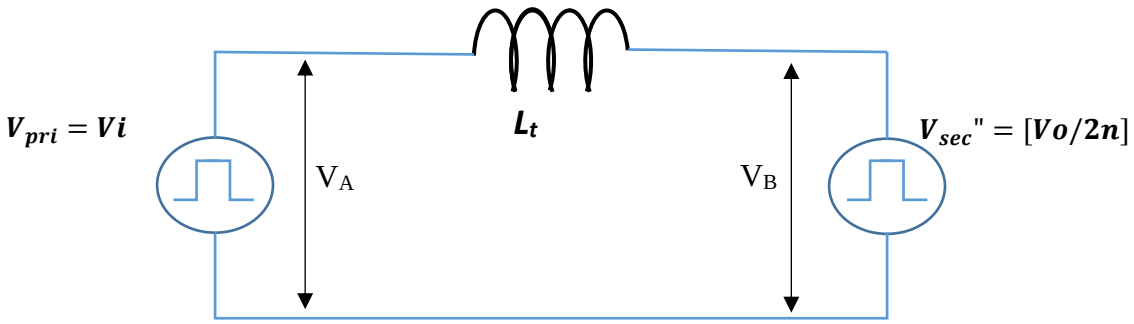


Fig.5.8 Simplified IBDC equivalent scheme

V_A represent the voltage generated by the bridge, Where,

$$V_{pri} = \begin{cases} +V_{in} \\ -V_{in} \end{cases} \tag{5.2}$$

V_B refer to the transformer secondary voltage, Where,

$$V_{sec}" = \begin{cases} +V_O/2n \\ -V_O/2n \end{cases} \tag{5.3}$$

Where, n is the transformer ratio.

The bridge side runs with a constant duty ratio of 50%. The pulses of each leg are complementary with a dead time to prevent shorting the power supply on each side of the converter. Fig. 5.9 shows the main waveforms of the BDC.

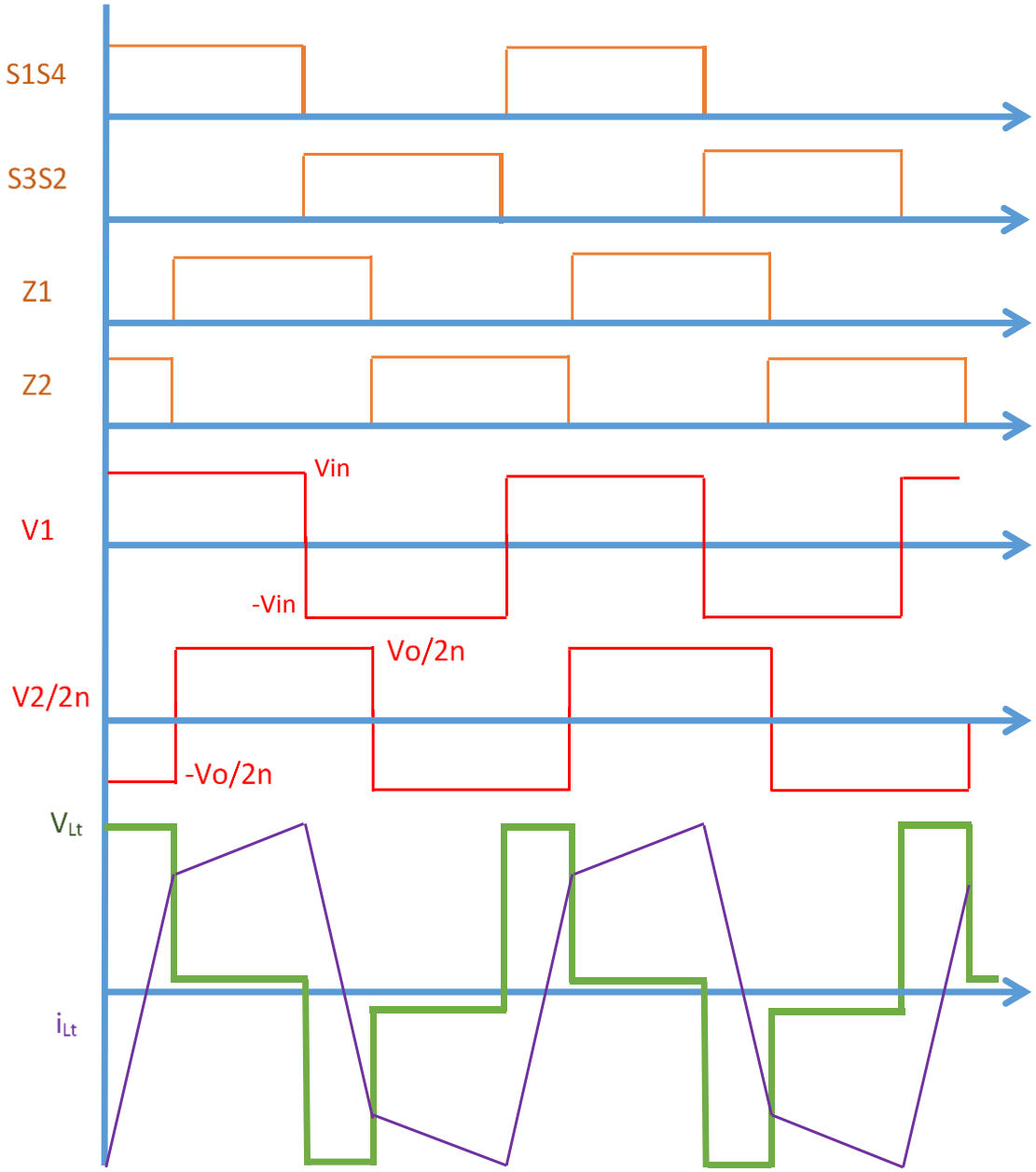


Fig.5.9 Main IBDC waveforms

From Fig.5.9, The voltage difference V_{Lt} results in a rising and falling current i_{Lt} which reverses each half period. Due to the symmetry of the circuit, a half switching period will be analysed. Fig 5.10 shows the primary winding current i_{Lt} .

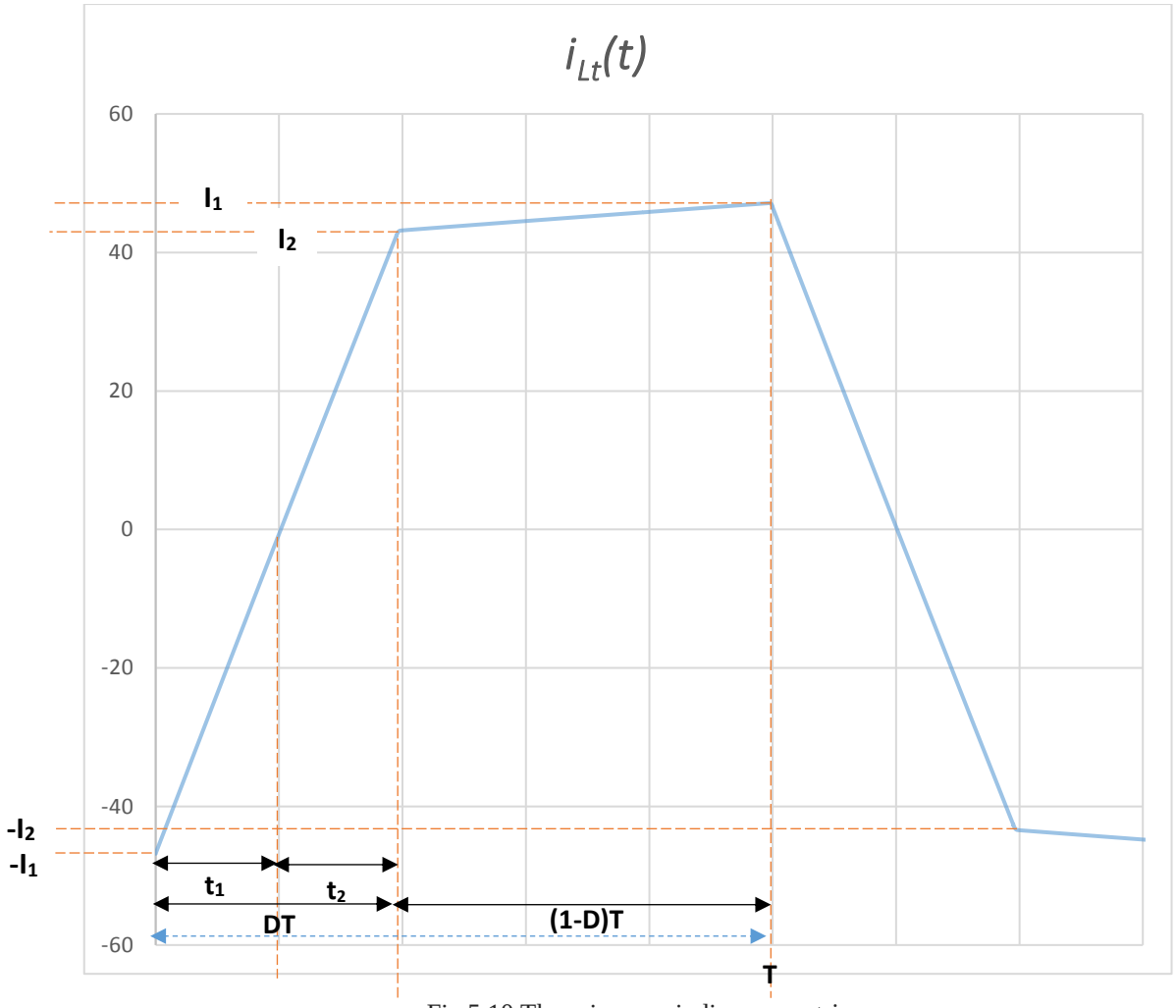


Fig.5.10 The primary winding current i_{Lt}

The current in the series inductor L_t can be expressed as,

$$\frac{di_{Lt}(t)}{dt} = \frac{V_A(t) - V_B(t)}{L_t} \tag{5.4}$$

Solving equation above,

$$i_{Lt}(t) = I_1(t) + I_2(t) \qquad 0 < t < DT \tag{5.5}$$

$$i_{Lt}(t) = I_1(t) - I_2(t) \qquad DT < t < T \tag{5.6}$$

$$i_{Lt}(t) = \frac{v_{in} + \frac{v_o}{2n}}{L_t} DT \qquad 0 < t < DT \tag{5.7}$$

$$i_{Lt}(t) = \frac{v_{in} - \frac{v_o}{2n}}{L_t}(1-D)T \qquad DT < t < T \tag{5.8}$$

Solving equations from 5.4 to 5.8 yields,

$$I_1 = \frac{T}{2L_t}\left[\frac{v_o}{n}\left(D - \frac{1}{2}\right) + v_{in}\right] \tag{5.9}$$

$$I_2 = \frac{T}{L_t}\left[v_{in}\left(D - \frac{1}{2}\right) + \frac{v_o}{4n}\right] \tag{5.10}$$

By the same way, from Fig.5.10,

$$t_1 = DT - t_2 \tag{5.11}$$

$$t_2 = t_1\frac{I_2}{I_1} \tag{5.12}$$

From equations 5.11, and 5.12;

$$t_1 = \left(\frac{I_1}{I_1 + I_2}\right)DT \tag{5.13}$$

Using equations 5.9, 5.10 and 5.13 yields,

$$t_2 = \left(\frac{v_{in}\left(D - \frac{1}{2}\right) + \frac{v_o}{4n}}{v_i + \frac{v_o}{2n}}\right)T \tag{5.14}$$

$$t_1 = \left(\frac{\frac{v_o}{n}\left(D - \frac{1}{2}\right) + v_{in}}{2\left[\frac{v_o}{2n} + v_{in}\right]}\right)T \tag{5.15}$$

5.4 BDCs Control Strategies

Typically, BDCs use a phase-shift control strategy to control the transfer of power in both directions. However, the BDC operation with a phase-shift control cannot maintain soft-switching (SSW) for a wide variation of the UC voltage and exhibits a higher circulating

power flow with a higher RMS current, and higher conduction losses as a consequence [97]. Therefore, alternative modulation methods for the BDC are necessary.

5.4.1 Conventional Modulation in BDC

The BDC uses the phase-shift between the voltages across both sides of the isolation transformer to control the transfer of power through the series inductance L_t in both directions. This type of modulation is called conventional phase-shift control (CPC) modulation [137, 138].

According to the power transmission directions of the BDC, there are two operational modes:

- Ultra-capacitor charging mode (UCCM) in which power is transferred to the UC, where the average power P_{uc} transfers from the DC link side to the UC side and $P_{uc} < 0$, $\varphi < 0$
- Ultra-capacitor discharging mode (UCDM) in which the power is transferred from the UC, where the average power P_{uc} transfers from the UC side to the DC link side and $P_{uc} > 0$, $\varphi > 0$

Within the CPC, all BDC switches are driven at 50% duty cycle and the transferred power is controlled by only the phase-shift angle φ.

$$Puc = \frac{V_o V_{uc}}{2n\pi\omega L_t}(\pi - \varphi)\varphi \tag{5.16}$$

Fig.5.11 shows the BDC power Puc with a different phase shift angle and under different input voltages Vuc.

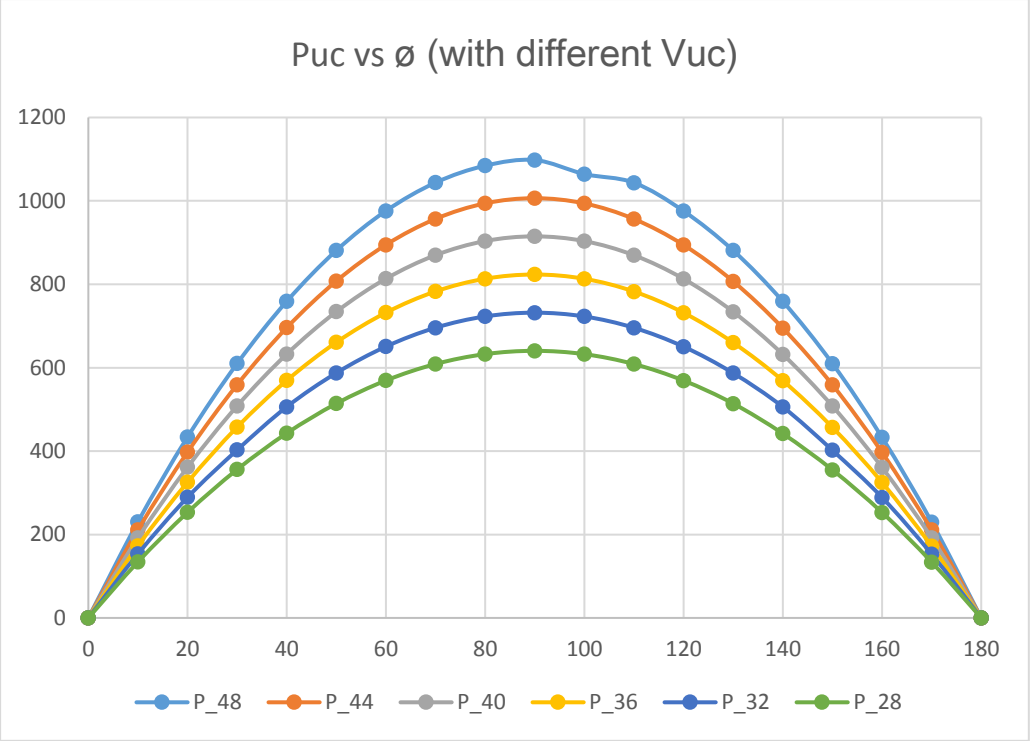


Fig. 5.11 BDC power flow under CPC modulation (L_t=10 μH, n=7.4, V_o=650V, and f_s=20kHz)

As Fig. 5.11 illustrates, the power of the BDC under CPC can be controlled by varying φ only, and for that reason as well as being simple to implement, the CPC modulation method has been widely applied [137, 138, 139]. Moreover, the BDC under CPC has the highest power transfer capability of any modulation scheme [140]. Also, one of the CPC advantages is that the switching devices on both BDC sides can operate with zero-voltage switching (ZVS) for the entire phase-shift angle range [141].

The relationships between the primary RMS current and the phase shift φ for different UC voltages are shown in. Fig. 5.12. It is clear that the RMS current of the BDC under CPC increases at higher φ values and that the BDC has a higher RMS current when the UC voltage increases (i.e. $2nV_{uc} > V_o$). Thus, from the view of higher efficiency it is desirable for the BDC under CPC to operate: with a smallest phase-shiftφ. However, this is at the detriment of the power transfer capability of the BDC and its use in UC applications.

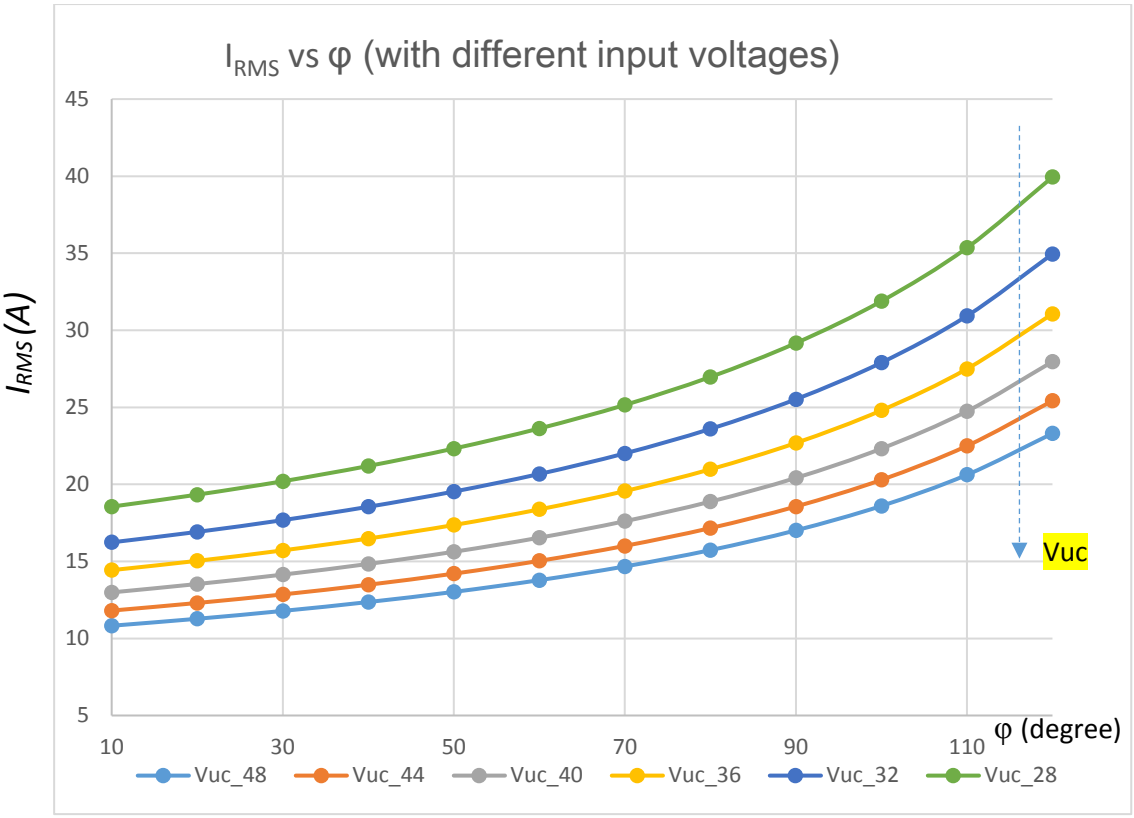


Fig.5.12 Relationship between Iin_RMS and φ_{outer} under CPC

Fig.5.12 shows the relation between the RMS input current and the phase shift under different UC voltages. As can be seen in the figure, the RMS current value decreases with a higher UC voltage, and it increases when the phase shift varies from 10 to 120 degrees. The highest RMS means higher losses so a phase shift limitation should be considered. Because of the high switching and conduction losses, the CPC modulation is disadvantageous, and therefore, the CPC is not the preferable modulation strategy for the BDC circuit when it is incorporated with a wide input/output voltage range source. Alternatively, modulation topologies should be considered to reduce the losses and enhance the BDC performance. This brought the researchers' attention to find a new alternative modulation scheme which focuses on the soft switching for a wide input voltage source variation SSW range expansion for optimum performance and higher efficiency of the BDC as will be shown in the next section.

5.4.2 Design Considerations of the Series Inductance (L_t)

The aim of the BDC is to control the power flow between the DC link and the UC within the DC micro-grid. Although the BDC is applied for short operational time periods compared to the FC system, it enhances the DC micro-grid efficiency. To ensure that a high operating efficiency is achieved, the converter parameters should be selected accurately. The series inductance L_t is the vital component that affects the BDC efficiency. Fig. 5.13 shows the power of the BDC for a different series inductance L_t under CPC modulation that was calculated according to equation (5.16).

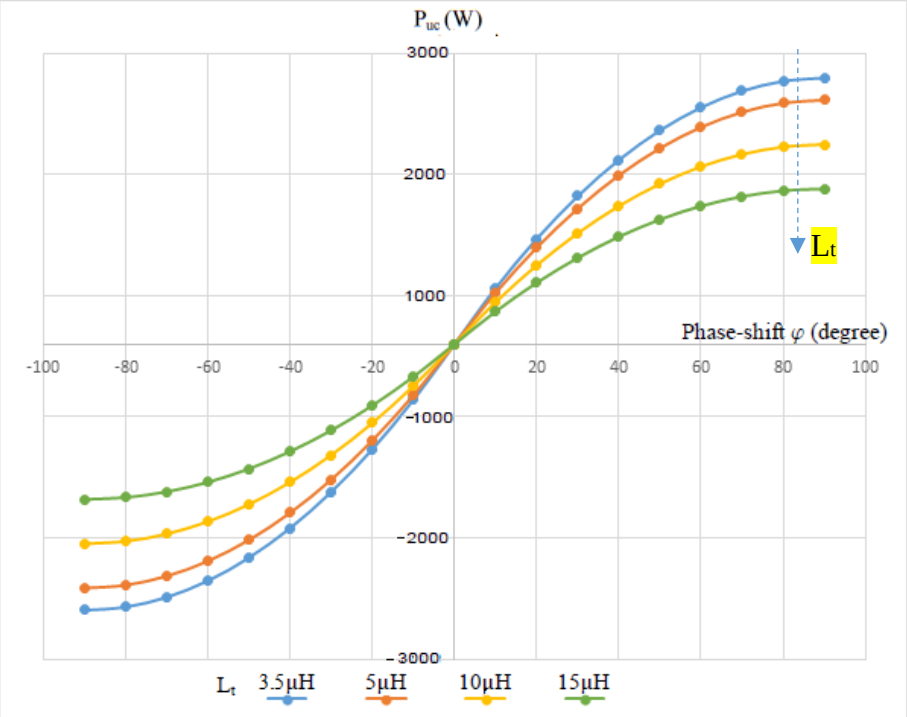


Fig. 5.13 Relationship between power and phase shift under various leakage inductance (V_{uc}=48V, f_s=20kHz, V_o=650V, n=7.4)

As illustrated in Fig. 5.13, the BDC can transfer more power with a smaller series inductance L_t. Also, it is can be seen that a smaller L_t reduces the required phase-shift angle for the same power P_{uc}. Thus, the smaller the series inductance L_t becomes, the more power the BDC can transfer. On the other hand, a smaller L_t limits the phase-shift angle range for the same power. Therefore, the selection of the series inductance L_t is a trade-off between the required power and phase-shift angle.

5.5 Reviewing the Alternative Modulation Schemes

To control the power flow of the ultra-capacitor bidirectional converter a phase-shift between the voltages across both sides of the converter transformer is required. Despite the simplicity of implementation of this method, it causes degradation in the performance and operating efficiency of the converter. Therefore, an alternative modulation method to improve the converter performance is required. A number of modulation methods have been proposed in the literature to control the power flow of the BDC with extended soft-switching operation and lower conduction losses [97], such as triangular current modulation (TRM), modified triangular current modulation (MTRM), and trapezoidal current modulation (TZM). Table.1 summarises the main features of different Alternative Modulation Schemes.

Table.5.1. Comparison of different Alternative Modulation Schemes [97]

APM Scheme	RMS Current in the BDC	SSW Status	Power transfer Capability P_{uc_max}	Switching Controller Complexity	Limits
TZM	Lower than CPC within same operating range Higher than TRM	ZVS and ZCS for all switches	High but $<P_{uc\_max}^{CPC}$	High (Variable duty cycle with phase-shift)	
TRM	Low (if operating with power rating less than TZM range)	ZVS and ZCS for all switches	Low (less than the achievable power of TZM), where the maximum power $P_{uc\_max}^{TRM}$ that can be transferred is $P_{uc\_max}^{TRM} = \frac{\pi V_B^2}{2\omega L_t V_A}(V_A - V_B)$	Very high (Variable duty cycle with phase-shift) (rising-edge and falling edge alignment required)	Doesn't work if $V_A = V_B$ and $V_A < V_B$ High n required
MTRM	Medium (at the light load) High (for the high power transfer)	ZCS for all switches when BDC operating under light load only	Medium	Medium (Variable duty cycle with fixed phase-shift)	
CPC	High	ZVS for all switches (only if $V_A = V_B$)	High (under the BDC power rating)	Very Low (Fixed duty cycle with variable phase-shift)	

5.6 Switching Control Strategy (Dual Phase Shift Control)

A number of a dual phase shift topologies have been presented in [142-145]. However, these strategies were designed for dual active bridge bidirectional converter. That make it more difficult when controlling the phase shifts of the same bridges and the phase shifts between the two side bridges, which will complicate the controller. In the BDC proposed in this thesis, and because of the full bridge and the half bridge side, the number of active devices is reduced. This gave the advantage for a less complex controller.

In [97] a new control algorithm has been proposed, that circumvents the disadvantages of the listed methods in table.5.1. Fig.5.14 shows the proposed switching control algorithm for the BDC. The switch control modifies the primary voltage only by overlap of the top/bottom switches of the UC bridge side for a specific period, by inserting a phase-shift angle (φ_2) between S_1 and S_3 (or S_2 and S_4) whilst maintaining a fixed 50% duty cycle. The phase shift φ_1 is an important parameter which determines the direction and amount of power transfer between the two sides of the converter [146]. Hence, by controlling the overlap between the bridge switches as well as the phase shift between the low-voltage and high-voltage side bridges, the amount and the direction of the power flow for the BDC can be controlled.

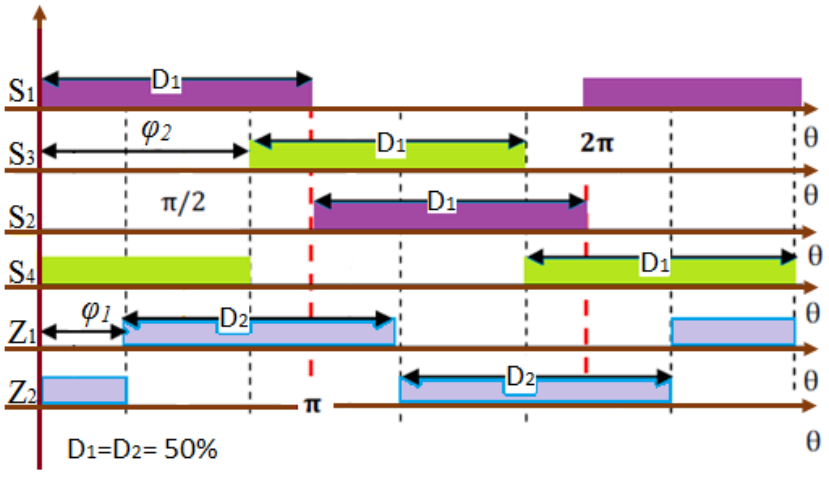


Fig. 5.14 Switching control algorithm for the BDC

The switching of S2 and S4 is complementary to that of S1 and S3 respectively. Switch Z1 lags or leads the switch S1 by a phase-shift $\varphi 1$ depending on the power flow direction. This method will facilitate implementation of the switching controller since no duty cycle variation is required. Five possible operating modes can be distinguished in respect to the phase-shift angles $\varphi 1$ and $\varphi 2$ when the BDC is operating under UC discharging mode (UCDM) [97]:

- Mode I: $0^0 \leq \varphi_1 \leq 90^0$ and $0^0 \leq \varphi_2 \leq 90^0$ with condition $\varphi_1 = \varphi_2$
- Mode II: $0^0 \leq \varphi_1 \leq 90^0$ and $0^0 \leq \varphi_2 \leq 90^0$ with condition $\varphi_1 \leq \varphi_2/2$
- Mode III: $90^0 \leq \varphi_1 \leq 180^0$ and $90^0 \leq \varphi_2 \leq 180^0$
- Mode IV: $90^0 \leq \varphi_1 \leq 180^0$ and $0^0 \leq \varphi_2 \leq 90^0$
- Mode V: $0^0 \leq \varphi_1 \leq 90^0$ and $90^0 \leq \varphi_2 \leq 180^0$ with condition $\varphi_1 \leq \varphi_2/2$.

In order to determine the optimum phase-shift range that results in the lowest RMS currents and switching losses, the performance of the BDC need to be examined for each mode after which the selected operating range was used to implement the proposed optimal modulation scheme. A further investigation with those modes is included in section 5.14.

5.7 Converter Construction and Implementation

The converter has been fully built with the driver circuits mounted and a signal processing board that was used for the control process of the converter [see Appendix F for the parameters and components of the BDC]. Fig.5.15 shows a photograph of the practical VFC. In order to implement a practical test on the converter, timing pulses for 6 devices need to be generated. These pulses were created using dSPACE.

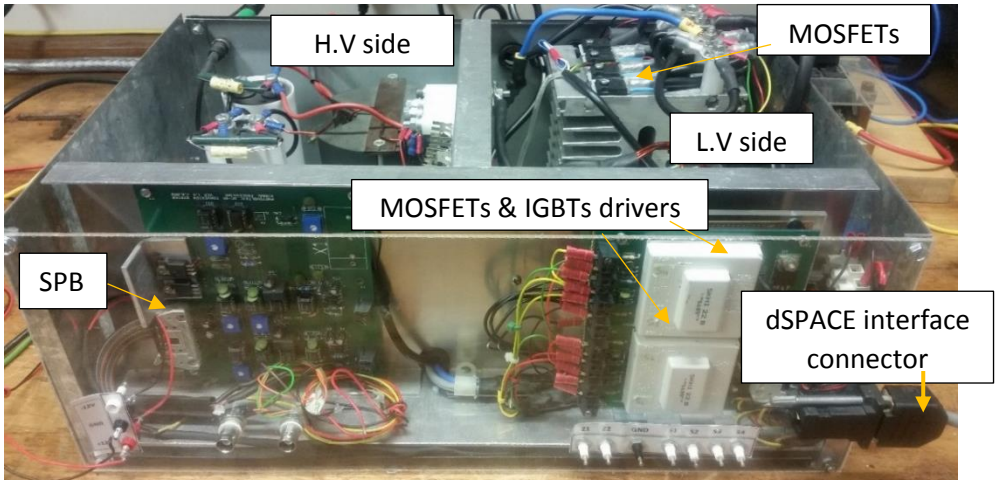


Fig.5.15 Voltage fed converter

The Signal Processing Board (SPB) used with the BDC control system was test in the following way. The SPB has two voltage inputs and one current input. A test was carried out on the SPB and it was found that the circuit was calibrated to give 5V out for a 750V bus voltage, 0.5V out for 50V input voltage, and 1.1V for 20A input current. The output signals of the SPB were connected to the dSPACE kit connector, then to the ADC block in Matlab Simulink. The ADC block modifies the input signal with a built-in gain of 0.1. This means that the 5V signal is represented as 0.5V in dSPACE.

5.8 Timing pulses using dSPACE

Six timing pulses are required for the VFC. These pulses are generated using dSPACE. For this, the PWM blocks in dSPACE/Matlab are used. As both the fuel cell system and the ultra-capacitor system will work together, all the pwm blocks that need to be used should work simultaneously without any interaction. The two PWM blocks have the ability to work simultaneously using the same I/O pins connector. The 4-channel block was used to generate the phase shifted pulses (S3, and Z1), and an external logic circuit was used to generate the complementary pulses S4 and Z2. In this stage of the work, the phase shift of the generated pulses is manually controlled through the Control-Desk

software on the host PC of dSPACE. Fig.5.16 shows the Matlab/dSPACE pwm block, and the Control-Desk blocks.

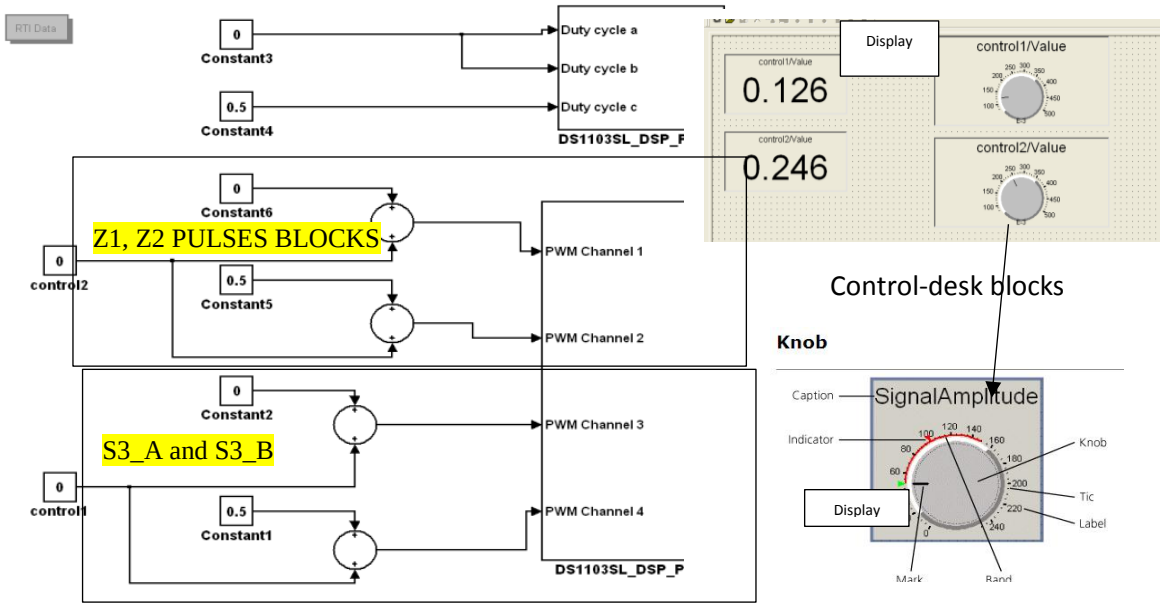


Fig.5.16 Matlab/dSPACE pwm blocks, and the Control-Desk layout

The dial instrument is used to control the values of the connected numeric variable blocks in the Matlab page (control1 and control2), so the phase shift of the generated pulses will be controlled, and the value of these blocks is displayed by using display blocks. Fig.5.17 shows the generated steps of the phase shifted pulses for the bridge side of the converter.

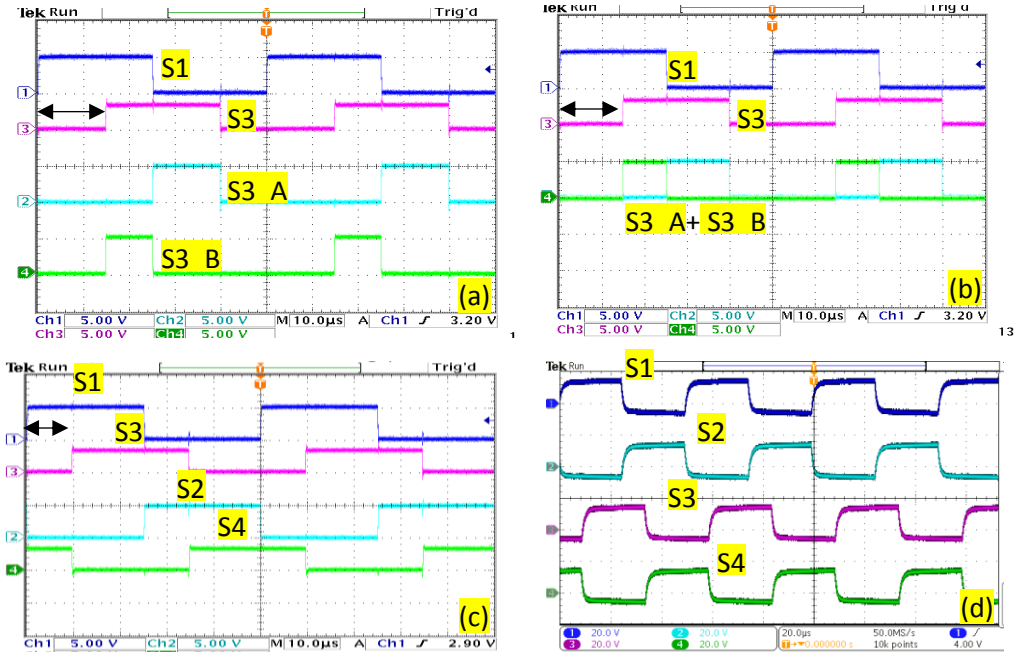
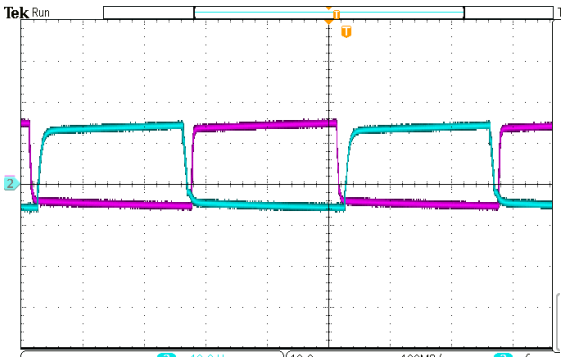


Fig.5.17 Steps for generating phase shifted timing pulses for the VFC

As can be seen from Fig.5.17a, the two pulses S3_A and S3_B are generated from pwm channel4 and pwm channel3 (see Fig5.16). These two pulses are combined in a "C*onstant*" block and controlled from block (control1) the value of these blocks are set for each channel to control the width in an opposite direction for each pulse (so every increase in the width of one of the pulses leads to a decrease of the width of the other pulse) in order to maintain a constant 50% duty ratio as shown in Fig. 5.17b. The final phase-shifted controlled signal S3 is generated by using an external or gate chip to combine S3_A and S3_B. S2 and S4 are the inverse of S1 and S3 respectively and they are generated by using an external NOT gate. Fig.5.17c shows the timing signals for the full bridge devices, and Fig.5.17d shows the final signals across the MOSFETs' gates. The same procedure has been followed to generate the IGBTs' timing signals. Fig.5.18a shows the timing signals across the IGBTs.



(a)

P6 ; SELECT	P5 ; TDT1	P9 ; TDT2	interlock time t_{TD}/µs
open / 5V	GND	GND	1,3
open / 5V	GND	open / 5V	2,3
open / 5V	open / 5V	GND	3,3
open / 5V	open / 5V	open / 5V	4,3
GND	X	X	no interlock

(b)

Fig.5.18 IGBTs timing signals and dead time selection

The dead time between the same leg devices to avoid shorting the power supply and/or the dc-grid side of the converter, can be adjusted using specific pins on the driver circuit as shown in Fig.5.18b. The selected interlock time is 1.3 µsec.

5.9 Converter Efficiency Test and Results

An experimental set-up has been carried out for the VFC. This test was made to measure the converter efficiency at different load levels. Table 5.2 shows the efficiency test results. Fig.5.19 shows the converter wave forms during the test.

Table 5.2. VFC efficiency test results

R_{load} (Ω)	V_{in} (V)	I_{in} (A)	P_{in} (KW)	V_{out} (V)	I_{out} (A)	P_{out} (KW)	Efficiency%
1785	48	3.729	0.15378	593.38	0.2122	0.12589	81.863
1400	48	4.96	0.19806	509	0.2995	0.15255	77.020
1000	48.317	6.030	0.22603	398.75	0.3782	0.15082	66.725
858	48.412	6.34	0.23060	357.31	0.4024	0.14381	62.363
691	48.571	6.669	0.23197	305.92	0.4295	0.13142	56.653
507	48.764	6.985	0.22527	235.88	0.4588	0.10787	47.885
300	48.899	7.3	0.2112	148.14	0.4888	0.072429	34.294

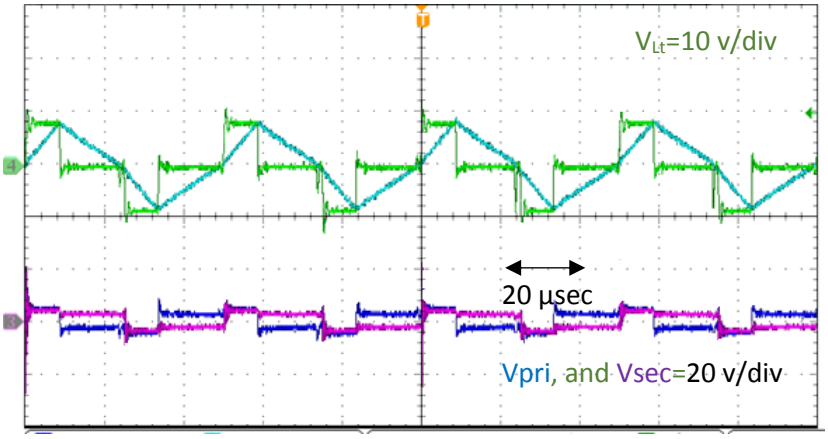


Fig.5.19 Converter wave forms during the test: from the top: inductor Lt Voltage (green), inductor Lt Current (light blue), primary winding voltage (dark blue), secondary winding voltage (purple)

During this test, two significant points were noted; first, the efficiency of the converter was not very high, dropping to less than 40% at higher load levels. Secondly, the temperature of the inductor was very high (more than 120^0C) as a result of its internal losses. The inductor had the same specification as that used for the current fed converter with the MACC (see chapter three). The conclusion was that the material and cross-sectional area of the core were not suitable for use with the VFC, as the inductor operated with higher currents. The inductor core loss is related to the material chosen and the core cross sectional area as well as to the ripple current, switching frequency, and inductance associated with the circuit. An inductor dissipates power both in the material of the core and in the windings. Additionally, a ringing in the inductor voltage was noted and minimized using a snubber circuit which adds more losses to the converter. A new inductor design was carried out as explained in section 5.10.

5.10 Inductor Design

Table.5.3 shows a comparison between the original inductor for the VFC and the newly designed one. This step has been made because core overheating issue of the existing inductor was also affecting the converter efficiency. A new core selection has been made regarding the material type[6] and the cross-sectional area. The new inductor has shown a better performance in terms of heating and efficiency. Table 5.3 also shows a comparison between the two inductors that was measured using the precision component analyzer in the Engineering Lab.

Table.5.3. Precision Component Analyzer measurements for the inductors

inductor	**Original**	**New Designed one**	PRECISION COMPONENT ANALYZER
L (µH)	13.048	11.45	
Parallel resistance (Ω)	68	109	
Series resistance (mΩ)	39.5	18.9	
Q (quality factor)	41.5	76.2	
Number of turns	N=11	N=4, airgap =1.5mm	
CORE TYPE	Toroid (T300-26) Iron powder	Ferrite (gapped)	
Core loss by material type from data sheet (@250KHz) mw/cm^3	80	1	

As can be seen from table 5.3, the quality factor (Q) for the designed inductor is much better than the original one. In addition, the material core loss is significantly less than the original toroidal core. Fig.5.20 shows photographs of the construction of the new inductor [Full core specification in Appendix G].

Fig.5.20 Designed inductor steps

[6] The choke was wound on a Micro-metals T300-26 core by Trans-Tronic Ltd.

Fig.5.21 shows the efficiency test for the VFC using two different inductors: the original one (orange curve) and the designed new one (blue curve). The results verify that with the new inductor the converter has a better efficiency. Furthermore, the new inductor core remains cool, even at high currents.

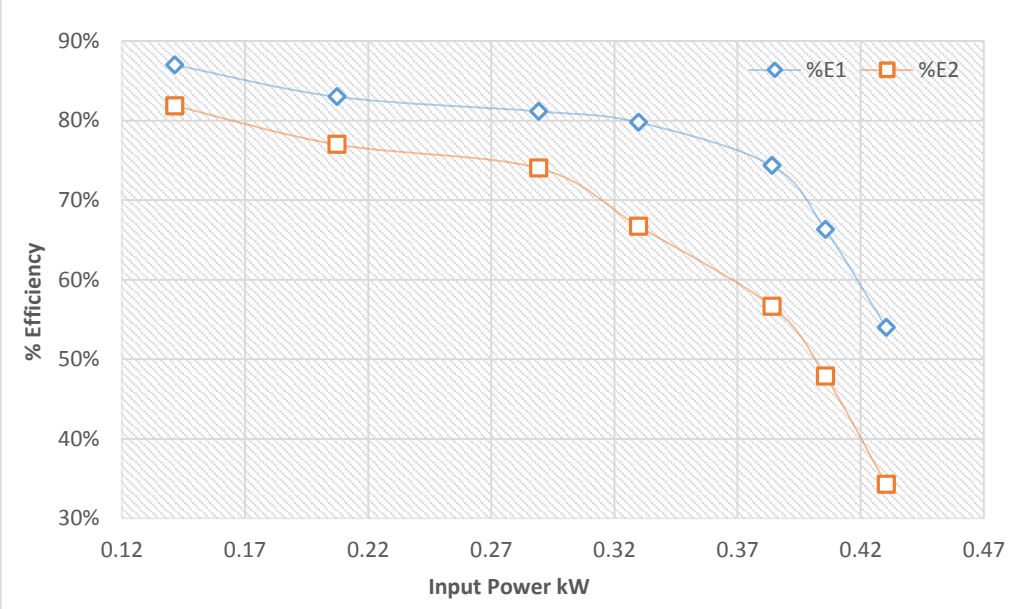


Fig.5.21 Converter efficiency test with different L design (%E1= new inductor, %E2= existing inductor)

5.11 BDC Control

In order to design a controller for the BDC, the system has been modelled and simulated using Matlab/SLPS system and the controller will be implemented using dSPACE.

5.11.1 Timing Pulses Using Matlab

Fig.5.22 shows the full timing circuit for the BDC. The circuit is designed to generate six pulses (four for the MOSFETs, and two for the IGBTs) with a dead-band between the pulses of the same leg devices and a controlled phase shift as shown in Fig.5.23.

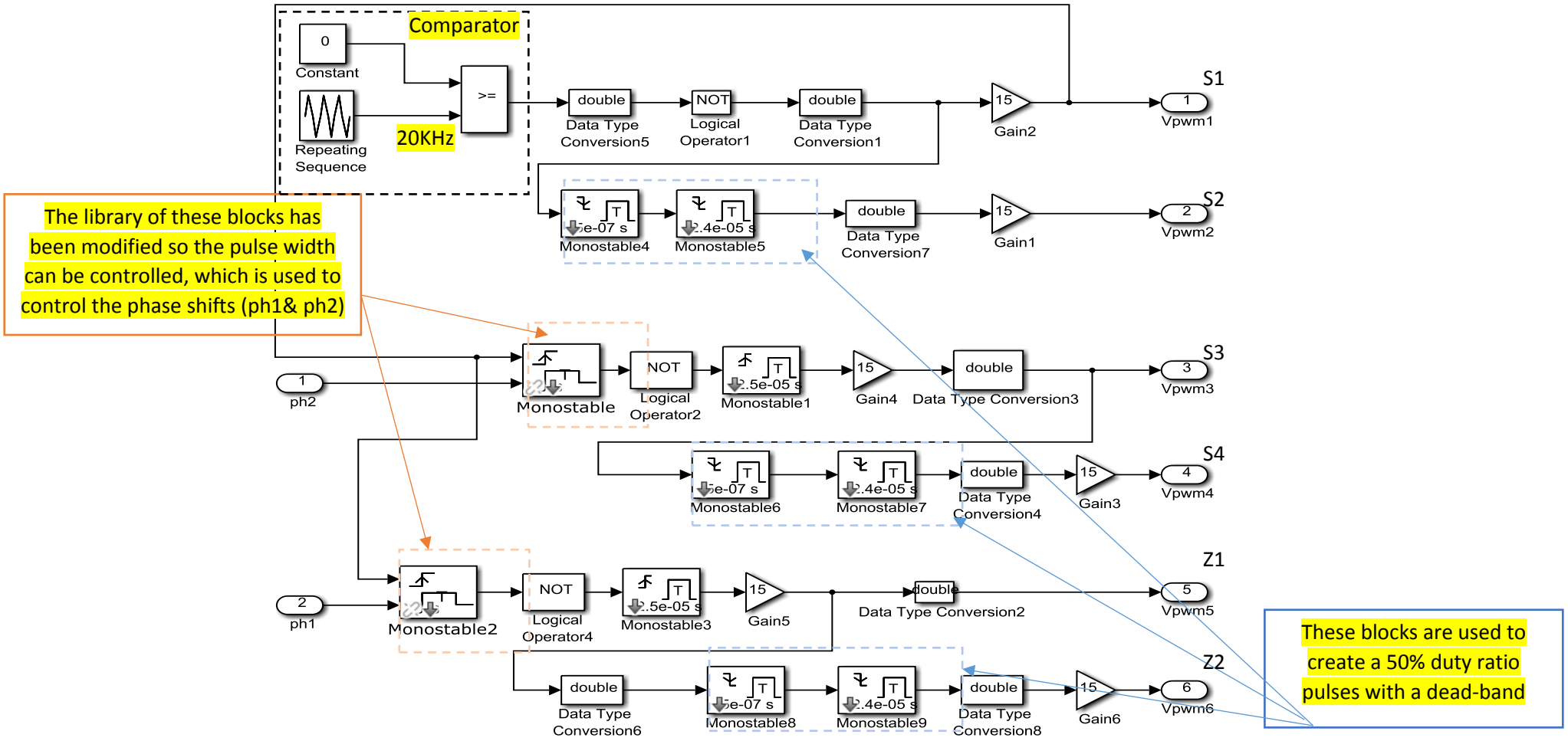


Fig.5.22 VFC timing signals using Matlab Simulink

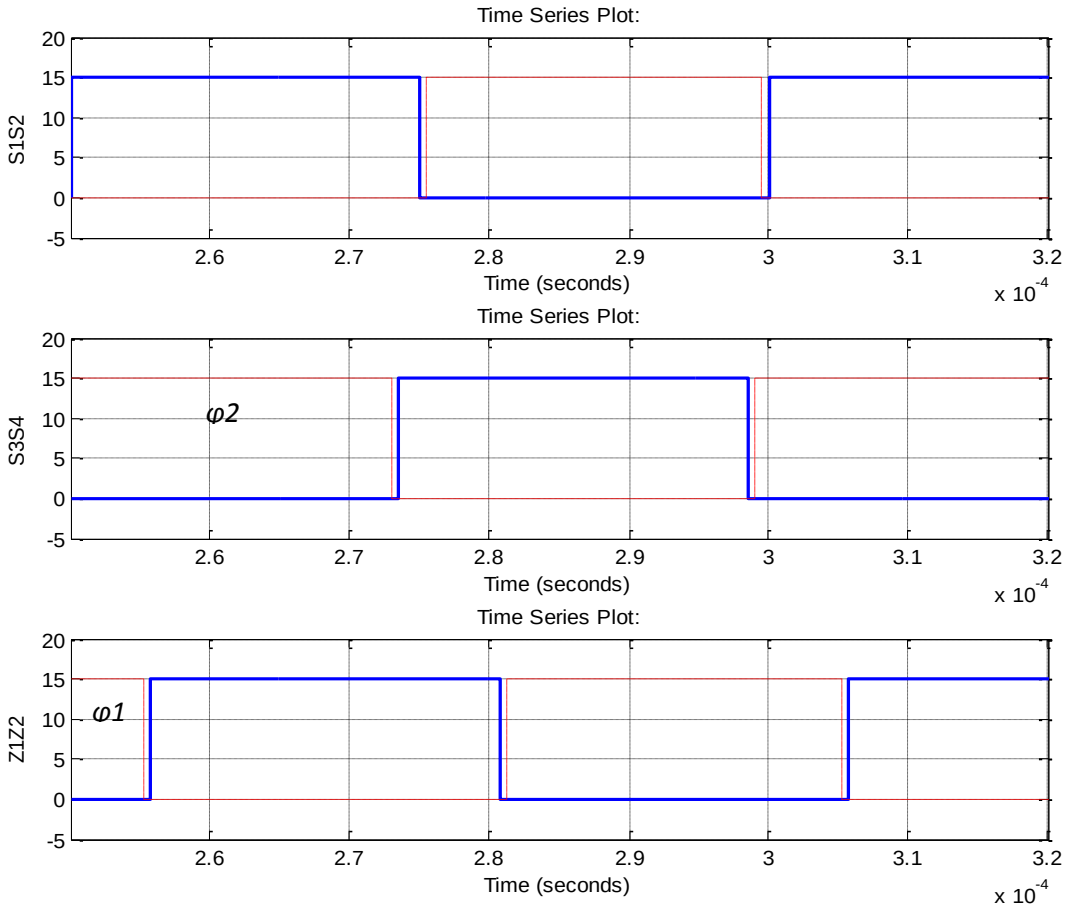


Fig.5.23 Timing signals of the circuit in Fig.5.22

5.11.2 Matlab/PSpice Co-Simulation

In order to simulate a realistic, the BDC, the Matlab/PSpice co-simulation was used as shown in Fig.5.24. The PSpice software is very suitable for simulating power electronic circuits that contain switching devices and non-linear elements. But it is less suited for control system simulation because of potential convergence difficulties. Also, simulating the control system in PSpice may require a large amount of time for analysis. On the other hand, Matlab/Simulink is a very powerful program for control engineering, but it is less suitable for accurate modelling of power electronic circuit characteristics. The SLPS interface has been developed to overcome these problems.

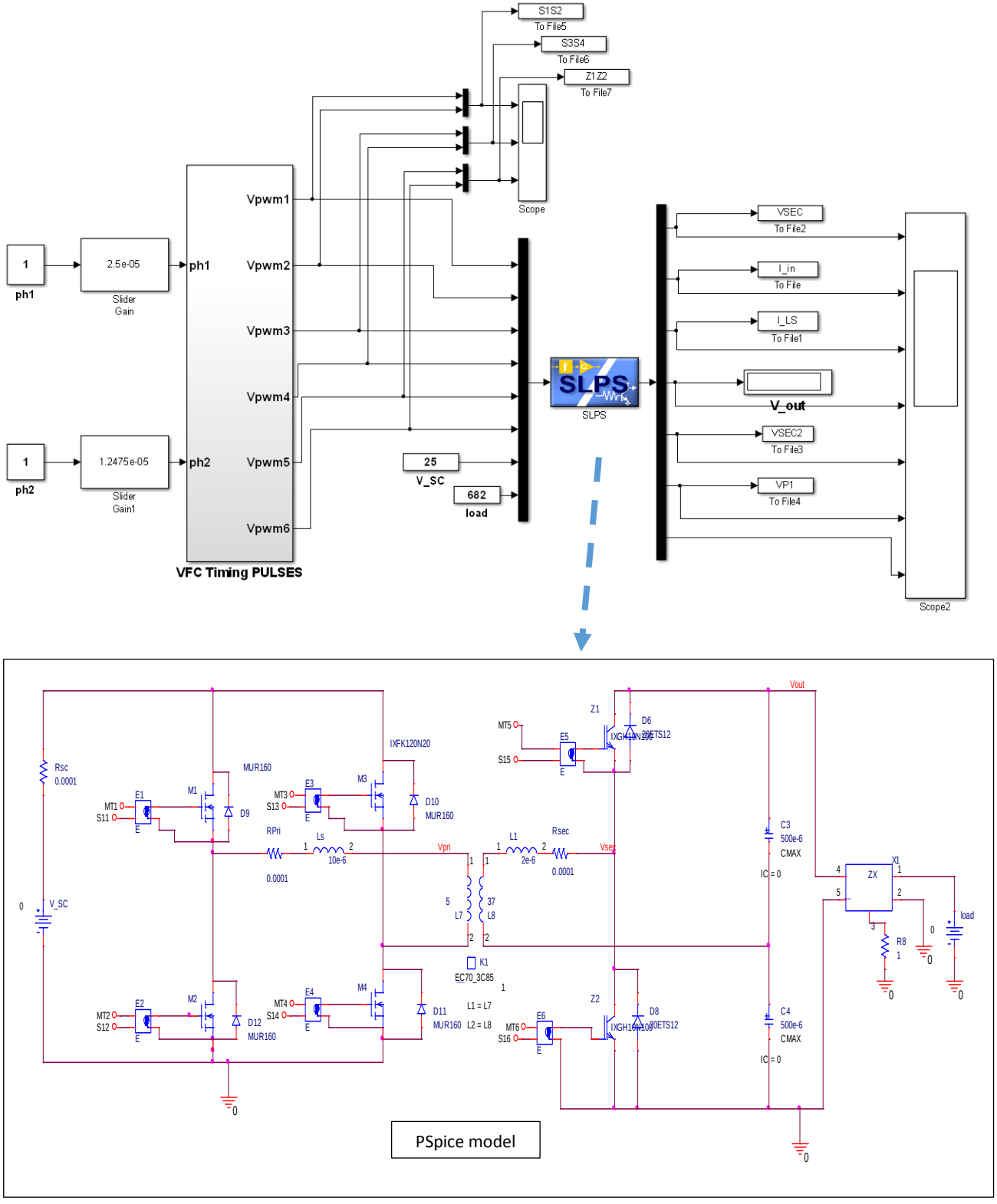


Fig.5.24 VFC simulation using Matlab/SLPS

The gain slider blocks in the circuit of Fig.5.24 have the ability to change their settings while Simulink is running, and they are used to control the phase shifts (ph1, ph2) between the timing signals on both sides of the BDC converter.

To specify a load in Simulink, a variable impedance ZX is used instead of a load resistor, thus making it possible to determine the resistance value using the voltage source V_{load} and to be able to control it from Simulink. Fig.5.25 illustrate the load model in PSpice.

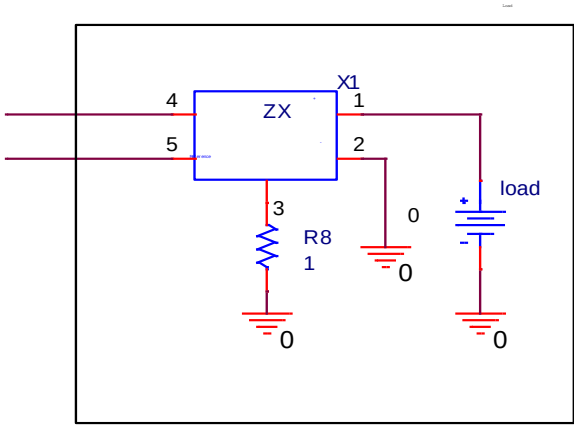
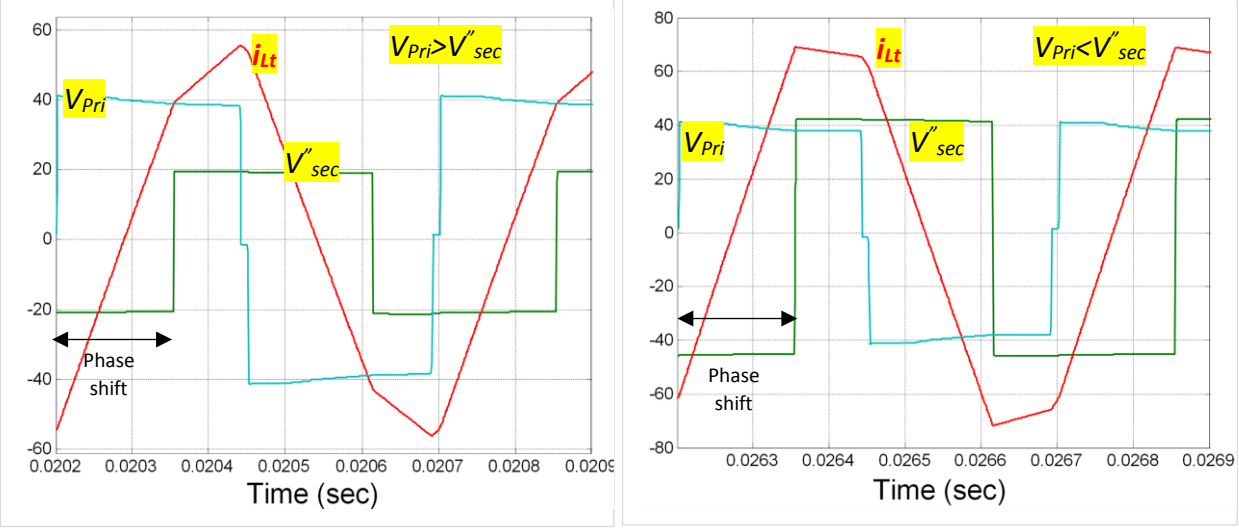


Fig.5.25 Load model in PSpice to be controlled in Matlab/SLPS

The shape of the inductor current depends on the magnitudes of the voltages across its terminals. Two cases, Buck for $V_{Pri}>V''_{sec}$ and Boost for $V_{Pri}<V''_{sec}$, are illustrated in Fig. 5.26.



(a) (b)

Fig.5.26 Simulation waveforms of the VFC using Matlab/SLPS for two operation conditions

As the structure of the converter is semi symmetrical, the power flow direction is achieved through reversing the sign of the phase shift φ [147]. Fig.5.27 shows simulation results for main waveforms of the converter for both power flow directions.

The power flow direction of the bidirectional converter is achieved by changing the sign of the phase shift φ_1[7] resulting in a change in the direction of power between the converter input and output. This will result in controlling the charging and discharging modes of the ultra-capacitor. Fig.5.27 shows the main BDC simulated waveforms for both power flow directions.

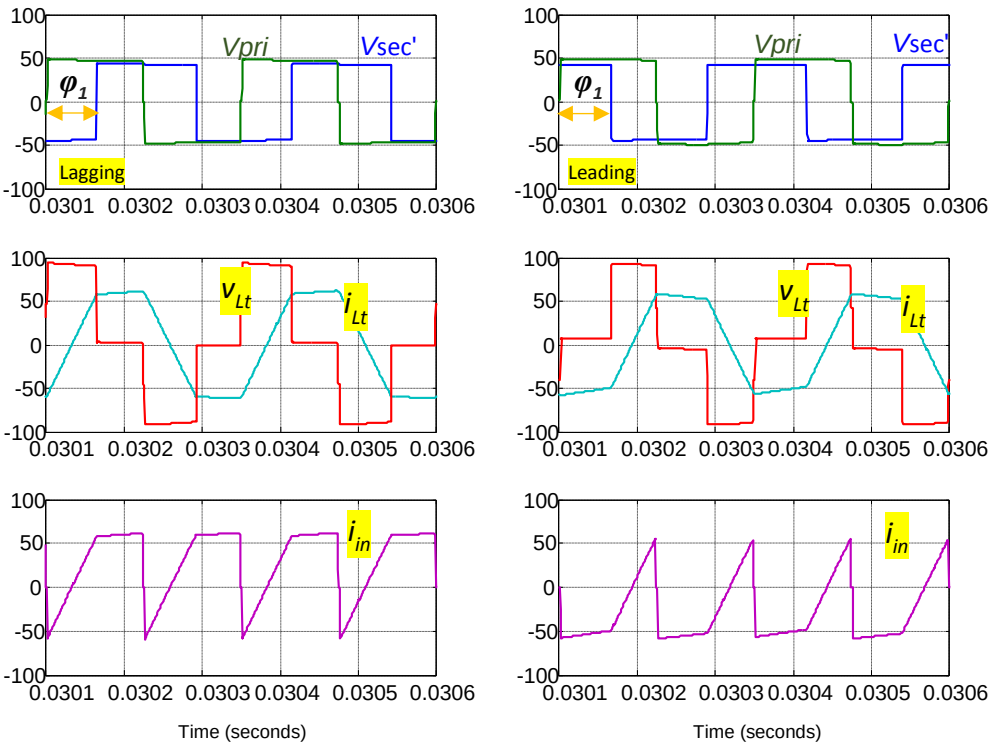


Fig.5.27 BDC with two operation modes: a) UCDM for $\varphi_1=90^o$, $\varphi_2=180^o$, b) UCCM $\varphi_1=-90^o$, $\varphi_2=180^o$

It can be seen from Fig.5.27a that the secondary voltage Vsec' is lagging the primary voltage *Vpri* by around 90°, while, in Fig.5.27b Vsec' is leading *Vpri* by around -90°.Therefore, the direction of the BDC currents i_{Lt}, and i_{in} are reversed in both cases.

[7] φ_1 is The phase shift between HV side and LV side of the BDC

During this investigation the phase shift values φ_1, *and* φ_2 were chosen to ensure a maximum power operation. Fig.5.28 shows the input power measurements for the power in both directions.

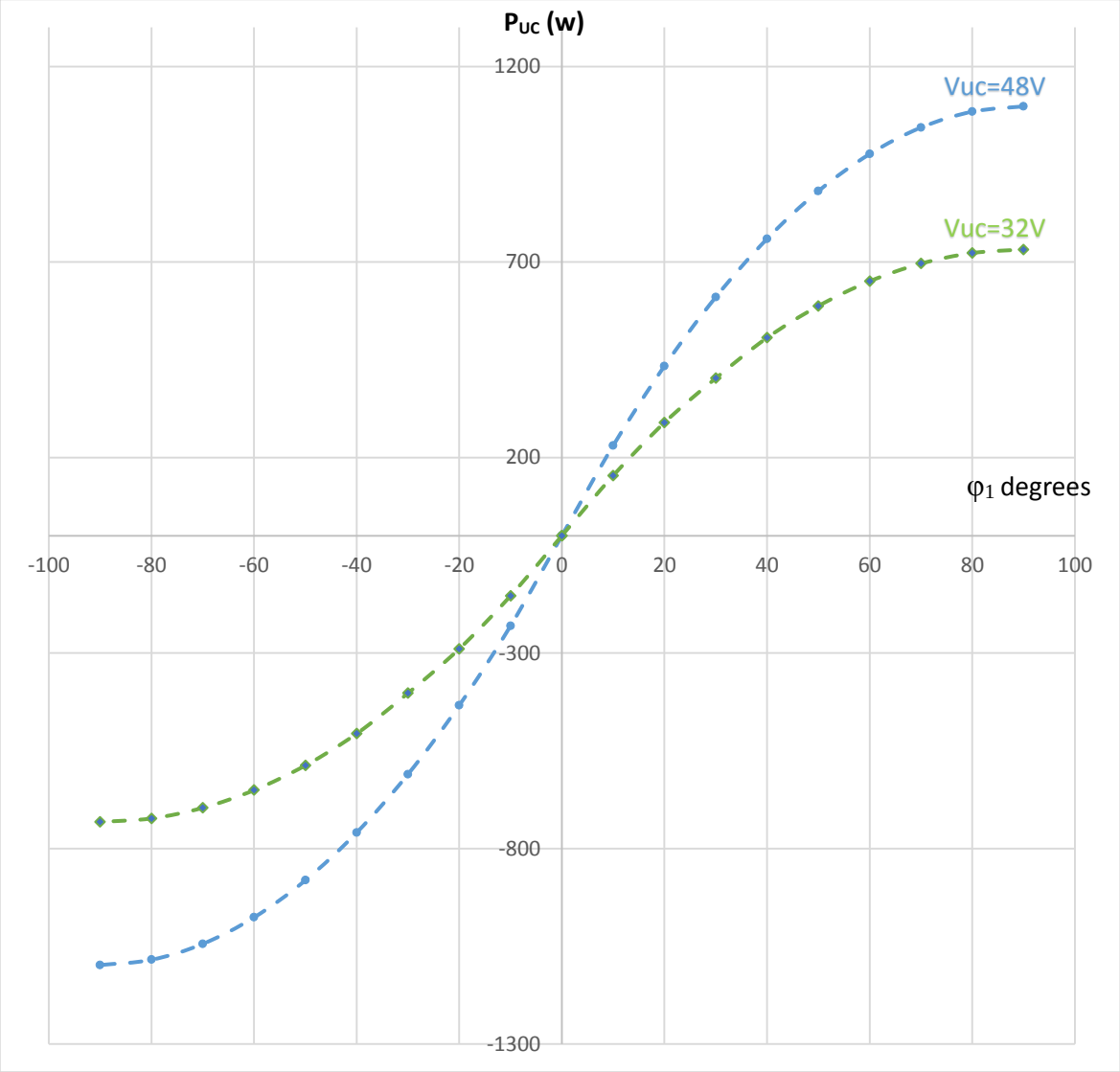


Fig.5.28 Input power for both power flow direction, (L_t=10µH, n=7.4, V_O =650v, and fs=20 kHz)

As can be seen From Fig.5.28, the BDC power flow under CPC can be achieved by controlling the phase shift φ_1 from 0 to 90°, φ_2=180° in one direction and from 0 to -90° for the opposite direction. It can be noted that approximately the same amount of power can be delivered in both directions by only changing the sign of the phase shift angle φ_1. The results in Fig.5.27 and Fig.5.28 prove that the phase shift φ_1 is the main variable that

controls the amount and the direction of the power of the BDC. Additionally, It can be seen that the power increasing reaching to the maximum value where $\varphi_1 = \frac{1}{2}\varphi_2$ (according to equation 5.16).

5.12 Charging and Discharging the Batteries Using the BDC

In this section a test has been carried out for testing the BDC ability to transfer power in both directions. Fig.5.29 shows a practical result for the output current from the high voltage side of the BDC. In this test, three batteries with 12.5V each were used as the converter input as a first step before using the UC.

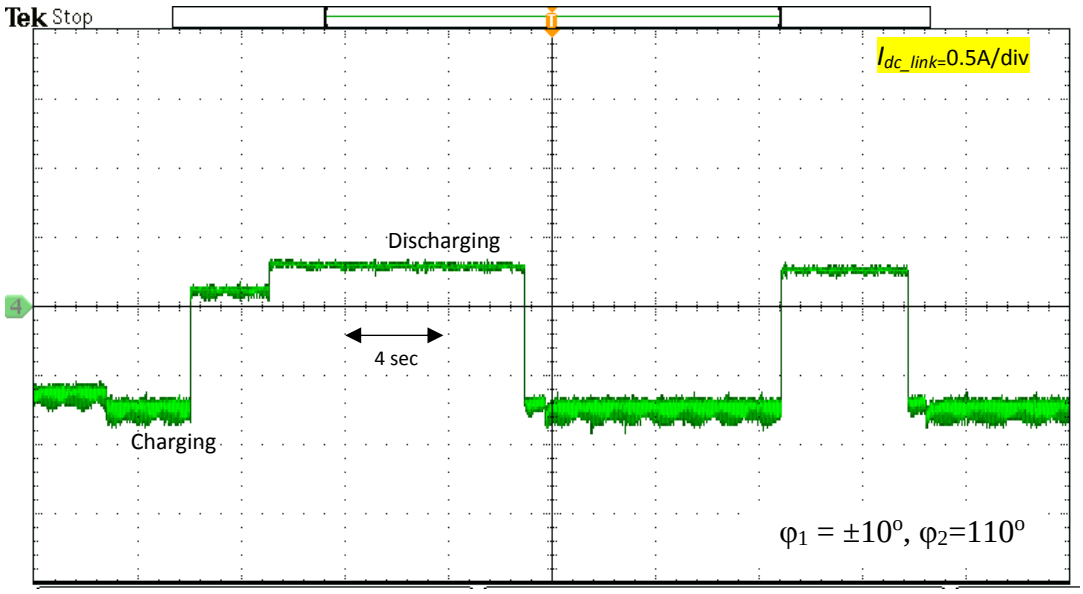
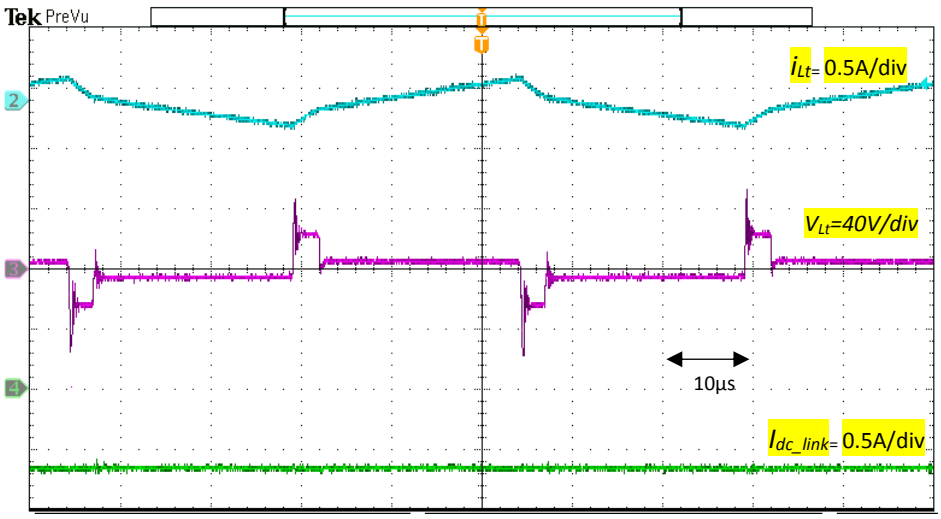


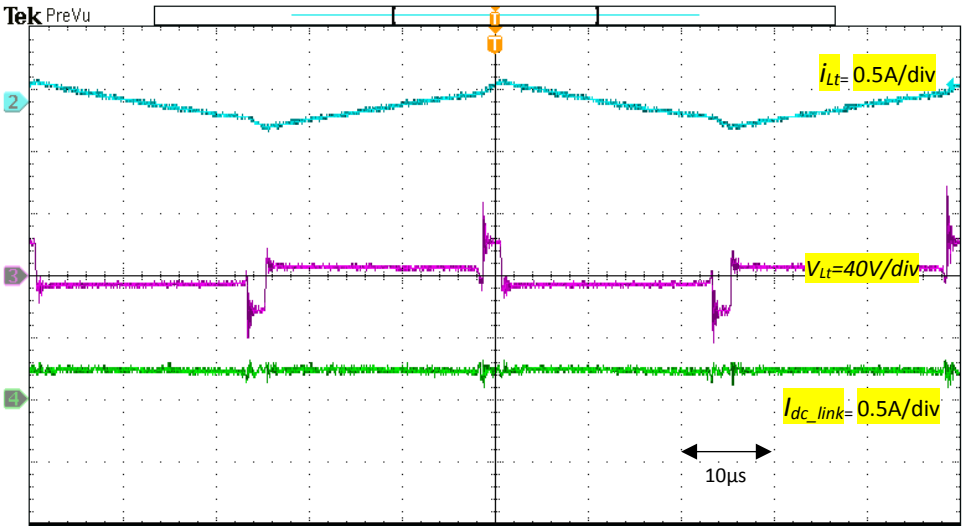
Fig.5.29 Current direction during charging and discharging of the batteries

This result shows the ability of the BDC to transfer power in both direction by only controlling the phase shift of the converter. The results of Fig.5.29 show that the converter has the ability to convert the power direction instantaneously according to the system needs of charging and discharging the batteries/Ultra-capacitor.

Fig.5.30 shows the converter waveforms during this process. By comparing Fig.5.30a with 5.30b, it can be seen that the inductor (L_t) voltage and DC link current direction were reversed due to the change in direction of the power flow.



(a)



(b)

Fig.5.30 Experimental waveforms of the BDC during a) charging, and b) discharging batteries, from the top; the inductor current Lt, the inductor voltage Lt, and the dc link current

5.13 Charging and Discharging the Ultra-capacitor using the BDC

For this test, a DC link voltage source was created. It was composed of 16 batteries with around 12.5 volt each. These batteries were connected in a series to generate around 205 volt. The idea of using batteries was to create a dc link that was capable of delivering and absorbing power to charge and discharge the super capacitor. The ultra-capacitor that is used in this test was 50F, 32volt. The charging and discharging processes was controlled by controlling the phase shift of the bridge side which is called ph_inner (S3) with respect

to the reference pulses of S1. Fig.5.31 shows the gate signals for each process (charging and discharging the capacitor).

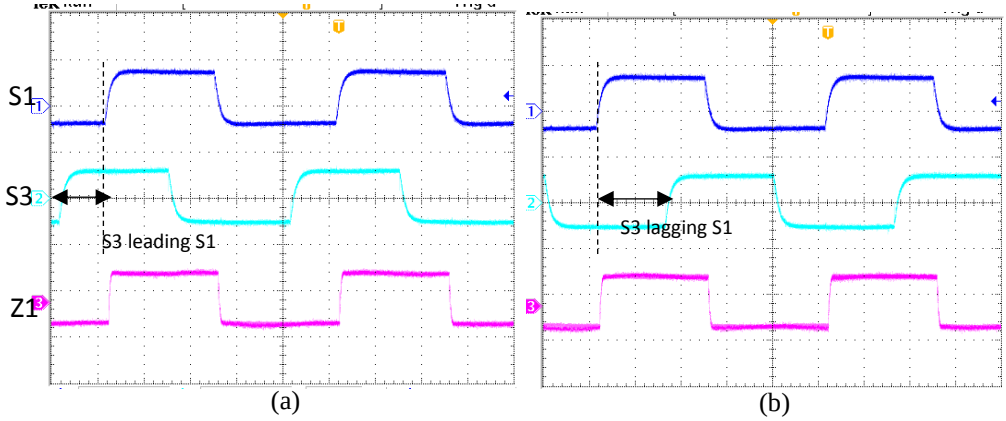


Fig.5.31 shows the firing pulses of the devices with: a) charging process, b) discharging

From Fig.5.31, if the gate pulse S3 is leading the reference pulse S1, this means that the power flow will be from the batteries to the capacitor (charging mode) as shown in Fig.5.31a. However, if S3 is lagging S1 (Fig.5.31b) the power flow will be reversed from the capacitor to the batteries (discharging mode). Fig.5.32 shows the capacitor voltage and current during the charging and discharging processes.

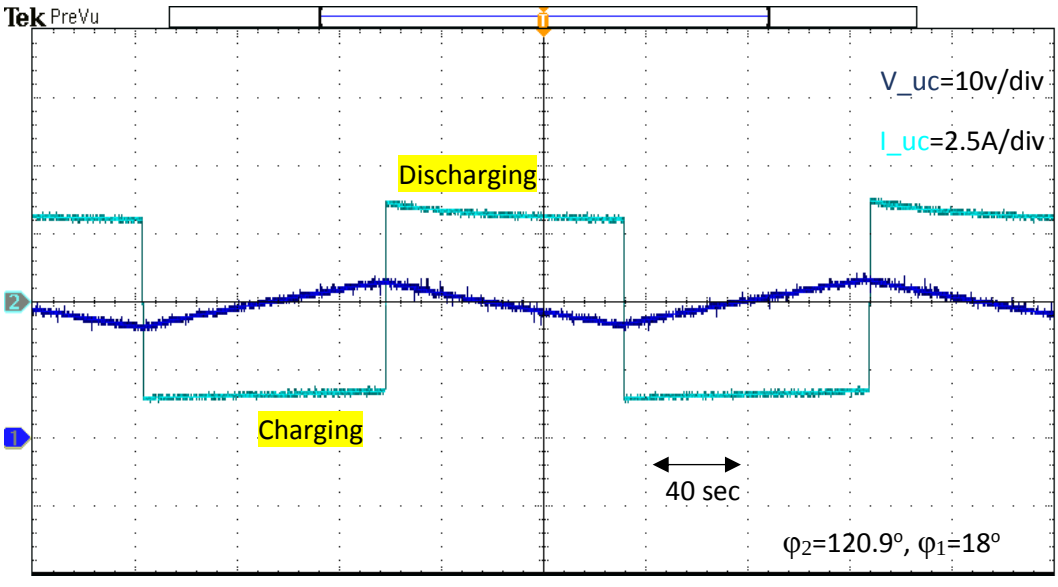


Fig.5.32 Ultra-capacitor voltage and current

Fig.5.32 shows the charging and discharging processes of the UC using the bidirectional converter. This process was controlled by controlling the phase shifts of the bridge side using dSPACE with the help of the ControlDesk layout of the dSPACE. Fig.5.33 shows

the dSPACE Matlab configuration for BDC control. Table 5.4 illustrates all the measurement values of the converter during the test.

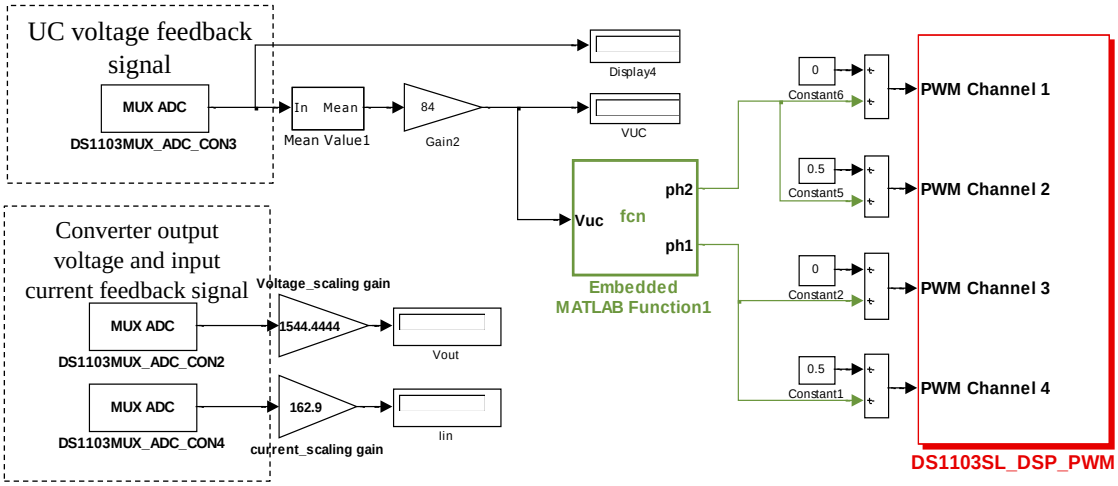


Fig.5.33 dSPACE Matlab configuration for BDC control

As shown in Fig.5.33, the UC feedback signal is measured from the SPB of the converter and fed to the dSPACE using the MUXADC block. This signal is rescaled to its actual value using Gain2 block. Hence, it is fed to the fcn block where a code is written to control the phase shift values according to the UC level. This process controls the charging and discharging process of the converter by controlling φ_1 and φ_2.

Table 5.4 Measurements of the converter during the test

φ_2=120.9°, φ_1=18°	Charging	Discharging
Capacitor current	3.445	3.4
Capacitor voltage	18	21
Batteries current	0.4104	0.295
Batteries voltage	201.8	204
$P_{capacitor}$ (kW)	0.0669	0.0603
$P_{battries}$ (kW)	0.0798	0.0517
%Efficiency	83.8%	85.7%

Fig.5.34 below shows the instant of change of the phase shift and the corresponding reversal of the current that gives an idea about how fast the converter is during the reversal of the power flow when changing the phase shift. It can be seen that the UC response is

in the order of msec. This makes it the premium choice to be used for backup of the FC within the DC micro-grid system.

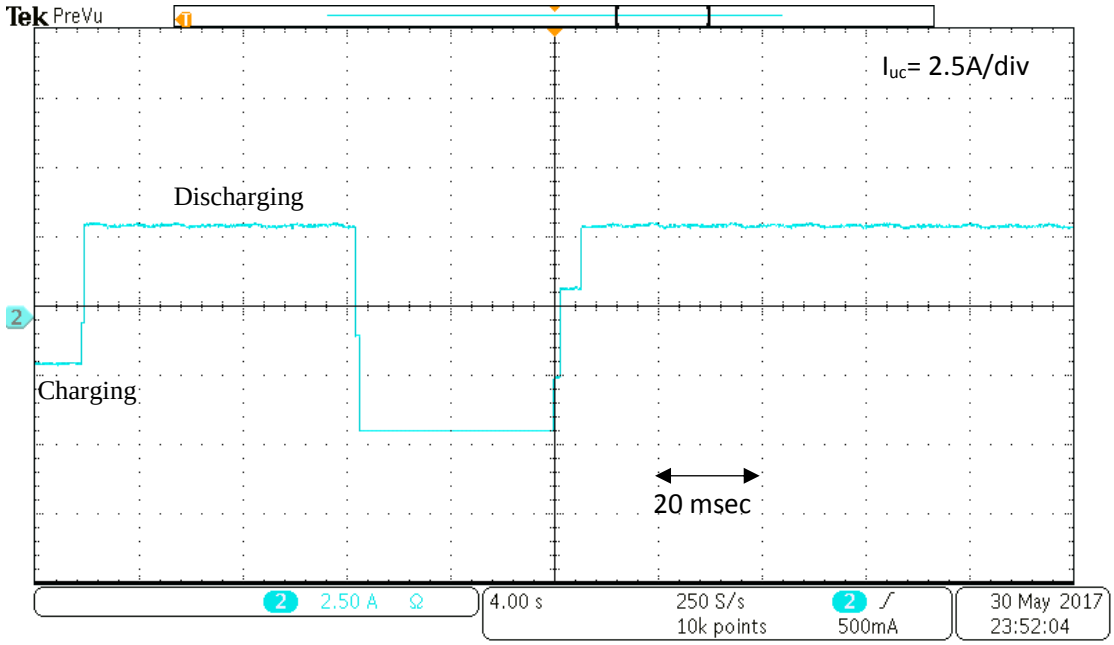


Fig.5.34 UC current during the charging and discharging

Fig.5.35 shows test results for measuring the BDC input power with two different levels of power under CPC by changing the phase shift φ_1 from 0 to 180^o and keeping φ_2 constant at 180^o.

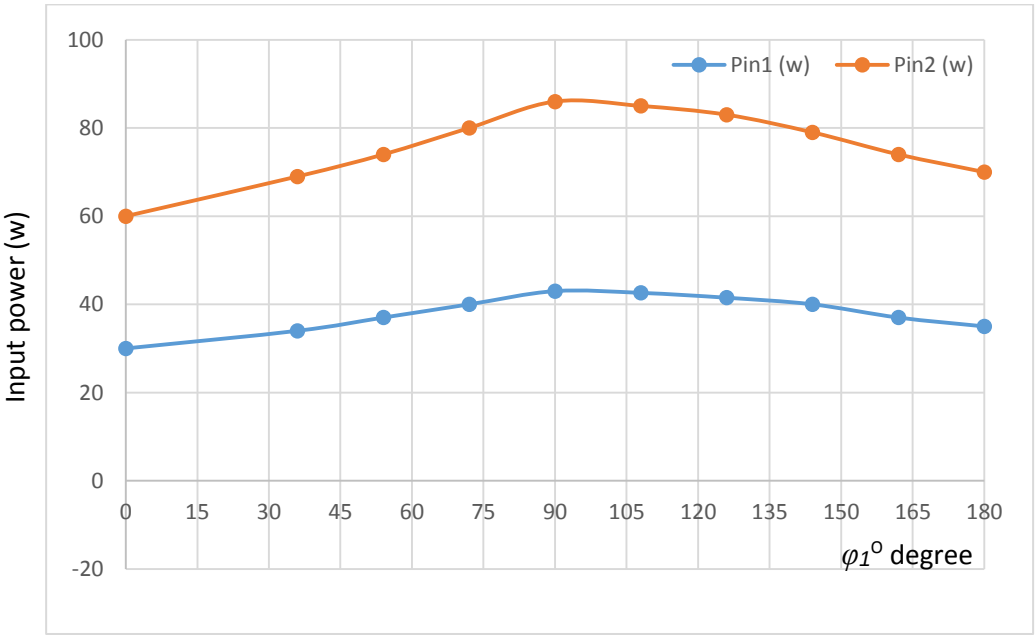


Fig.5.35 Test results for measuring the BDC input power

According to equation 5.16, the test results in Fig.5.35 proves that the BDC maximum power transfer can be obtained by setting $\varphi_1=90^o$, and $\varphi_2=180^o$ ($\varphi_1=\varphi_2/2$). This result validate the simulation results in both Fig.5.11, and Fig.5.28.

5.14 Investigation of the Proposed Algorithm

An investigation into the different operating modes proposed in [97] was carried out to find an optimum operating range for the inner and the outer phase-shifts φ_1 and φ_2 that result in the lowest RMS current and switching losses, and secondly to test the proposed algorithm using Matlab/slps model. The algorithm worked satisfactorily in Matlab/slps model and the results shows a good performance regarding the primary RMS current and the efficiency.

The maximum power achieved by the BDC operating in Modes I, II, IV, and V under UCDM is shown in Table below, where the following parameters have been used Lt=10μH, Vo= 650V; n=7.4, fs=20kHz, Vuc= 48V [97].

Table 5.5 Power Capabilities of the BDC with Different Operating Modes

Modes	Phase shift Conditions	P_{UC}	Puc Theoretical (W)
I	$0^0 \le \varphi_1 \le 90^0$, $0^0 \le \varphi_2 \le 90^0$ with $\varphi_1 = \varphi_2$	$Puc = \frac{V_O V_{UC}}{32 n f_s L_t}$	659
II	$0^0 \le \varphi_1 \le 90^0$, $0^0 \le \varphi_2 \le 90^0$ with $\varphi_1 \le \varphi_2/2$	$Puc = \frac{3V_O V_{UC}}{64 n f_s L_t}$	988
III	$90^0 \le \varphi_1 \le 180^0$, $90^0 \le \varphi_2 \le 180^0$	$Puc = \frac{V_O V_{UC}}{16 n f_s L_t}$	1318
IV	$90^0 \le \varphi_1 \le 180^0$, $0^0 \le \varphi_2 \le 90^0$	$Puc = \frac{V_O V_{UC}}{32 n f_s L_t}$	659
V	$0^0 \le \varphi_1 \le 90^0$, $90^0 \le \varphi_2 \le 180^0$ with $\varphi_1 \le \varphi_2/2$	$Puc = \frac{V_O V_{UC}}{16 n f_s L_t}$	1318

It can be seen from Table 5.5 that the converter can operate at the full power rating only in Modes III and V. Hence, modes I and II and IV are undesirable since they are not able to deliver the required maximum power. The calculated primary RMS currents for different operating Modes and for two different UC voltage levels are plotted in Fig.5.36. By looking for the RMS values of the different modes, it can be seen that mode III has

the largest RMS current even though this mode could have delivered the maximum power as shown in Table 5.3. Hence, operation in Mode III is unwanted. However, Fig.3.36 shows that mode V has the lowest RMS value comparing it with the other modes, and can deliver the maximum power as indicated in table I. Therefore, mode V is the most efficient operating mode.

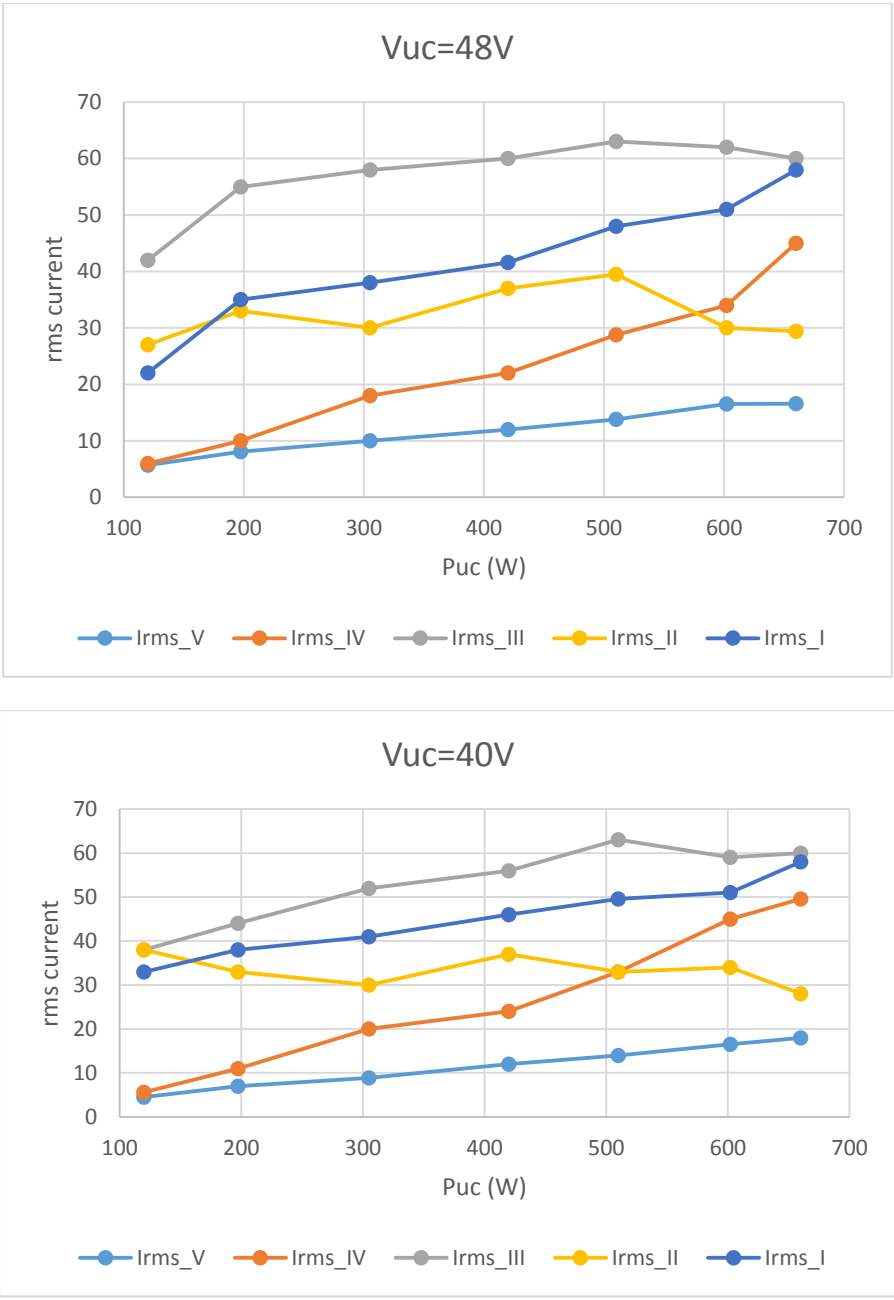


Fig.5.36 The resulting primary RMS current of the BDC operating with different modes under UCDM (L_t=10µH, V_o= 650; n=7.4; f_s=20kHz) for (a) V_{uc} = 48V, (b) V_{uc} = 40V

It would, of course, be preferable to find the optimum combination of φ_1 and φ_2 that leads to the lowest RMS current and thus increase the converter efficiency. But this would require a very complex algorithm to find the minimum RMS current. Hence, an optimal modulation method is proposed in [97] which is designed to achieve low RMS currents to reduce the conduction losses [See Appendix H for the Control Algorithm of the Proposed Optimal Modulation Scheme in [97]]. This code is set to ensure that the BDC converter is working with optimum circulating power flow at different power ranges. Fig.5.37 shows a simplified flow chart for the optimum phase shift control algorithm that is proposed in [97]. This flow chart describes the converter boost operation to ensures the optimum phase control for minimum circulating power flow. Depending on the measured UC power P_{uc}, the converter phase shifts can be set to push the converter to work with three operations modes [97];

1. Inner single-phase shift mode (ISP): by setting φ_1 to zero and adjusting φ_2. This mode only for the small power operation to get lower circulating power flow.
2. Zero circulating power flow mode (ZCPF): in this mode, both phase shifts φ_1 and φ_2 are adjusted to guarantee zero circulating power flow.
3. Minimum circulating power flow mode (MCPF): this mode is set by adjusting φ_1 and φ_2 for a power range beyond the ZCPF mode to ensure minimum circulating power flow.

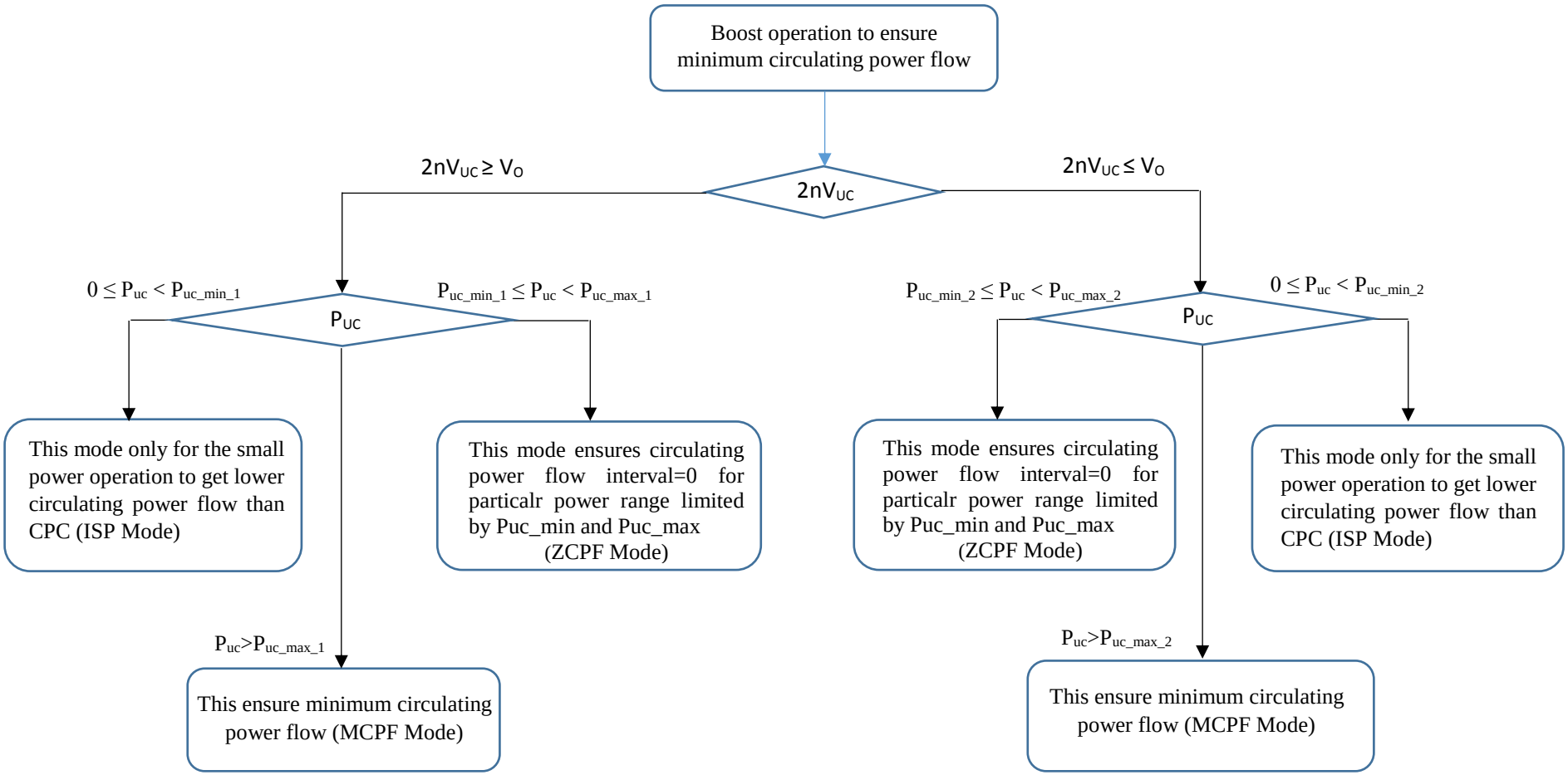


Fig.5.37 A flow chart of the optimum phase shift control algorithm (boost operation)

An investigation has been carried out to validate the proposed algorithm in [97]. Using the Matlab/SLPS model, the written code has been modified and the phase shift output have been rescaled in Matlab using a designed circuit to convert the phase shift unit from degree to time scale. To use the algorithm code [Appendix H] in the Matlab model, a function block was used. The code was merged inside this block to be executed during the simulation run. This code depending on the measured UC voltage and the input power P_{uc}. Hence, generating the required optimum phase shifts (φ_1, φ_2) that leads a lower RMS current and a higher efficiency. Fig.5.38 shows the Matlab/SLPS model combined with the Matlab function block that was used to generate the required phase shifts of the proposed algorithm.

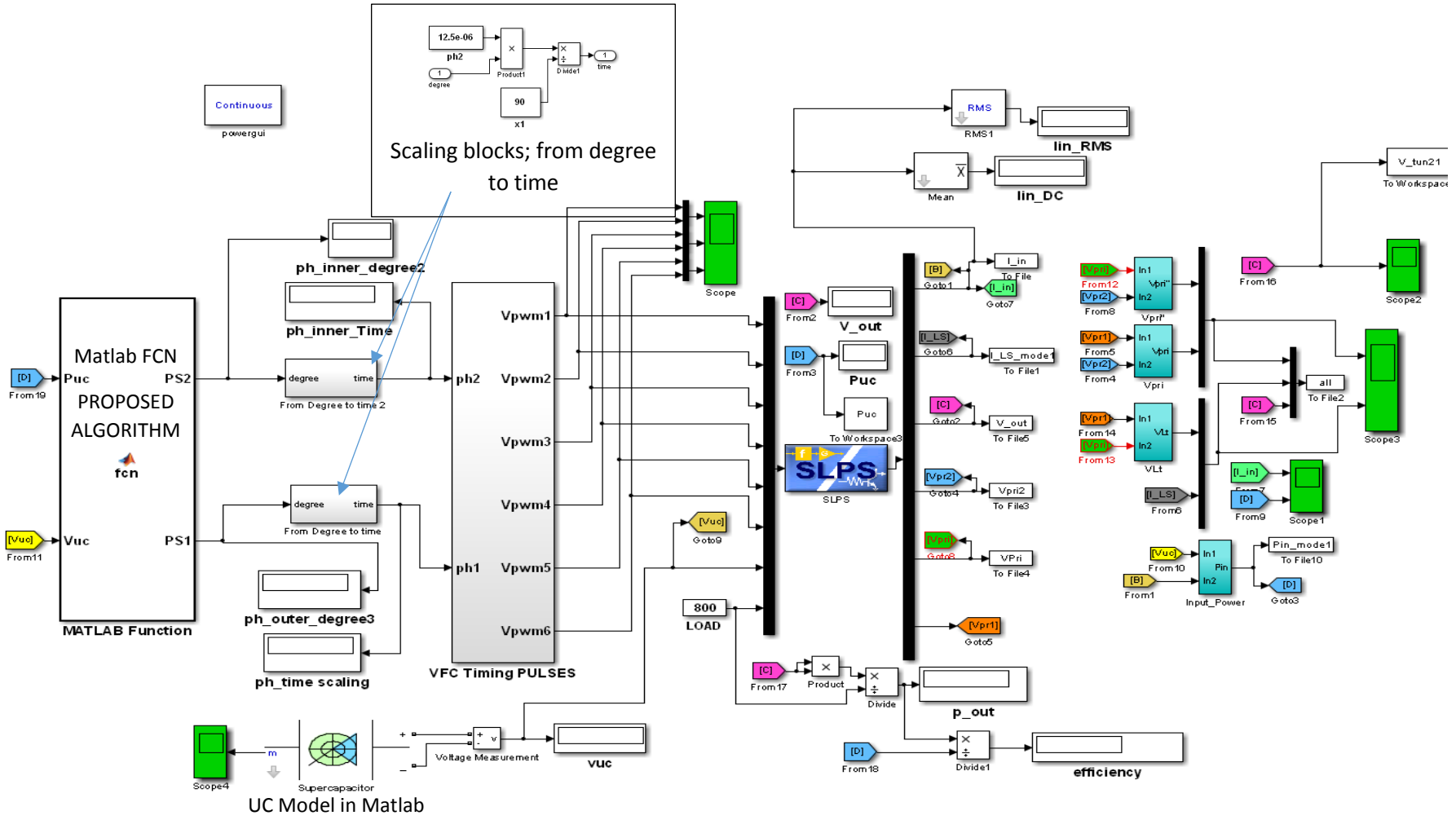
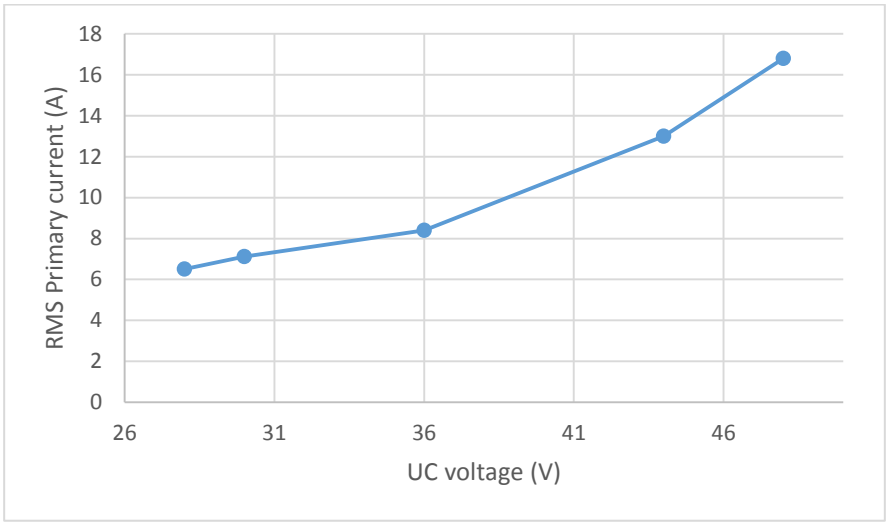
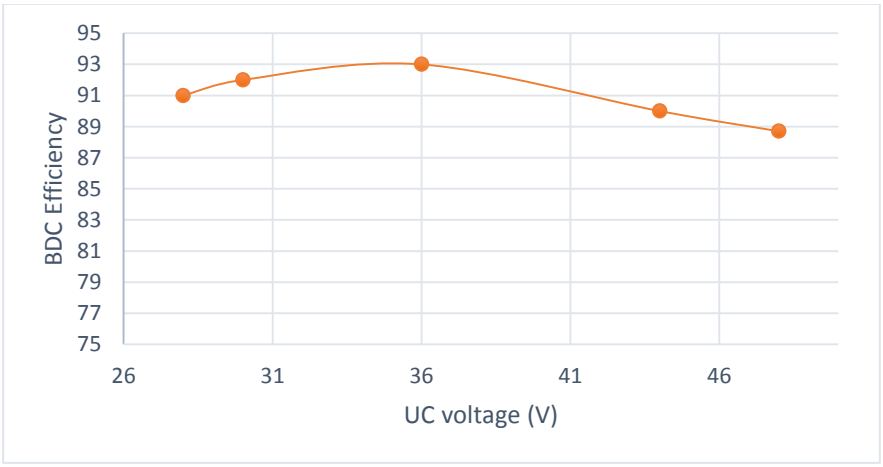


Fig.5.38. Matlab/SLPS model

After testing the algorithm in the model of Fig.5.38, the results show that the converter operated with lower RMS currents and a high efficiency. Fig.5.39 shows the simulation results of the transformer RMS current and the efficiency of the converter for different UC voltage levels. However, running the simulation using the Matlab function block slows the simulation because of the number of equations used in the written Matlab code.



(a)



(b)

Fig.5.39 a) RMS current vs UC voltage levels, b) converter efficiency under different UC voltage levels

Another test was conducted to calculate the efficiency and the primary RMS current under different load step. Additionally, the Matlab code was applied using dSPACE. The first test shows that the algorithm ran without any problem when it was executed in dSPACE in real time.

5.15 Conclusion

The isolated bidirectional converter (BDC) seems very attractive for interfacing the ultra-capacitor with the DC grid. It is capable of achieving bi-directional power flow as well as a high voltage boost capability and isolation between the energy storage and the load side. Both the modelling and the prototype show the ability of this converter to transfer power in both directions. This converter was modelled and tested using Matlab/PSpice and was implemented. The required pulses to drive all UC converter devices was generated using dSPACE. However, dSPACE does not have dedicated blocks to create the required phase shifted pulses. A novel method was implemented to overcome the dSPACE limitations. This method creates the set of phase shifted pulses that are required to control both the amount and the power flow direction. The test results have shown the ability of the UC converter for fast response and to transfer power in both directions. A dual phase shift control test to control the power flow was implemented. This test was fully controlled in dSPACE to control both the amount and the direction of the power between the UC and the dc link (charging and discharging the UC). By using the Matlab function block, a simple Matlab code was written to control the values of the bridge phase angles, φ1 and φ2 according to the feedback voltage of the UC. The results prove the capability of the converter to transfer power in both directions to charge and discharge the UC with a fast response in the order of 5msec.

Chapter Six

Chapter Six

Conclusions, and Suggestions for Future Work

This chapter summarises the conclusions that are drawn from this research work and describes the main contributions of this study along with suggestions for future work.

6.1 General Conclusions

The aim of this research study is to investigate and develop high-efficiency power electronic converters for the interconnection of various elements within a DC micro-grid. The main focus is on the power electronic converter topologies for connecting fuel cells and ultra-capacitors to a DC micro-grid for stationary power distribution systems. As this thesis seeks to prove, it has attempted to address the following issues and suggested the following corresponding findings:

- As for the investigation of existing unidirectional DC–DC converter topologies that are suited for the fuel cell energy buffer, presented in the thesis is a relevant literature review written in this respect and proposed that a full-bridge current fed converter is the most applicable technique to be applied to the fuel cell energy buffer. In the thesis, for instance, it is shown that a full-bridge current fed converter has the potential to overcome the fuel cell requirements such as low ripple current and unidirectional power flow.
- In terms of investigating and improving the Current fed DC-DC converter efficiency, in the thesis it is proposed to introduce a new clamp circuit topology. A modified ACC (MACC) has been developed to retain the desired rectangular shape of the transformer current and thus improve the efficiency of the converter. It has been shown that when using the MACC, the transformer and bridge currents become rectangular shaped to a large extent with a considerably lower rms value than the peaky currents resulting from the conventional ACC (CACC). While the

transformer primary voltages are close to square waves in both cases, a lower ringing voltage can be observed with the MACC.

Using the results obtained from the simulations over the full power range of the fuel cell, the efficiency of the converter fed from a constant voltage source was determined for both clamp circuits. The results shows that the simulation predicts an overall improvement with the use of the MACC by up to 2% points. It is obvious that the MACC has a better performance than the CACC, and the result shows that a significant reduction in the ringing can be obtained by using the MACC. These improvements obtained from the practical results presented in chapter three have been implemented on an existing 1.2 kW FBCFC. The transistor gate pulses were generated using dSPACE hardware, employing the DS1103SL_DSP_PWM3 block in Matlab, which has the ability to generate pulses with a frequency up to 5MHz.

- In order to compare the overall performance of the FBCFC with the two clamp circuits, the efficiency was measured with various loads up to 1.2 kW. The results demonstrate an efficiency improvement with the new clamp configuration of up to 2%, with a maximum value of 98%, in close agreement with the results from the simulations.
- Because the converter is designed for FC applications, efficiency test was also carried out using an actual FC, a Nexa 1.2kW. The results shows that the efficiency at higher converter outputs reduces steadily. This is due to the drop in FC output voltage with increasing load, forcing the converter to work with an increasing overlap period. However, the converter efficiency remains above 90% over most of the power range, which is considerably better than for a VFC, and the MACC still provides a better performance compared with the CACC.

- Pertaining to the control of output voltage, in case of using a single-loop controller, the RHPZ would limit the available bandwidth (BW) for stable operation of the proposed converter. Different techniques have been proposed to eliminate the RHPZ or to increase the RHPZ frequency in order to speed up the response of the system [18, 19]. However, these techniques make the input current discontinuous, which is not acceptable for a FC source. For that reason, a two-loop controller has been applied to eliminate the RHPZ from the closed-loop characteristic. The controller was implemented using dSPACE.
- In dealing with the bidirectional DC–DC converter topologies that are suited for the ultra-capacitor energy buffer, various literature reviews have been consulted and reported in chapter two. An interesting topology is described that provides a lower number of active devices at the lowest voltage rating and the highest efficiency can be achieved.
- Also reported in chapter two, are experimental tests that have been carried out to analyse the dynamic performance of the fuel cell/ ultra-capacitor. The time response to the fuel cell and the ultra-capacitor has been measured at the rate of seconds, it has been found the time response of the latter is significantly fast (in 5 msec), whereas the time response of the fuel cell was comparatively slow (in 0.24 sec).
- The ultra-capacitor converter topology proposed in chapter two has been constructed and implemented in chapter five. The required pulses of the converter devices were generated. The required pulses to drive all UC converter devices was generated using dSPACE. However, dSPACE does not have dedicated blocks to create the required phase shifted pulses. A novel method was implemented to overcome the dSPACE limitations. This method creates the set of phase shifted

pulses that are required to control both the amount and the power flow direction. The test results have shown the ability of the UC converter for fast response and to transfer power in both directions.

- Using an existing inductor, the UC converter was tested in the laboratory. It was, however, found that this inductor resulted in excessive heating and poor performance of the UC converter. Therefore, a new inductor was designed and implemented for the voltage-fed converter. Efficiency tests were carried out for the converter using two inductors with the same values but with different cores. The results of the efficiency comparison prove the importance of selecting the right core dimensions and material. The efficiency test results in chapter five verify that with the new inductor, the converter shows better efficiency than the converter combined with the old inductor.
- A dual phase shift control test was implemented in chapter five. This test was fully controlled in dSPACE to control both the amount and the direction of the power between the UC and the dc link (charging and discharging the UC). By using the Matlab function block, a simple Matlab code was written to control the values of the bridges phase angles, $\varphi 1$ and $\varphi 2$ according to the feedback voltage of the UC. The results prove the capability of the converter in transferring the power in both directions to charge and discharge the UC with a fast response in the order of 5msec. The dc link was created for this test by using 16 batteries (around 12.5 V each) to create approximately 205 V DC link.
- Finally, the ongoing investigation which aims at achieving an optimum dual phase-shift technique for controlling the ultra-capacitor converter system has paused at this point due to time limitations.

6.2 Contributions

- Improving the performance and the efficiency of the fuel cell converter by the means of introducing a modified active clamp circuit. Furthermore, the performance of the new circuit was improved by adding an additional diode to eliminate the circulating current through the clamp switch, consequently reducing the losses. This improvement was validated using both modelling and experiments setup.
- The BDC was modelled, fully constructed and successfully implemented in the lab. The required phase shifted pulses to drive the converter and controlling the power flow between the UC and the DC link was generated with a novel approach using dSPACE.
- The development of simulation models and the control system in this research was experimentally implemented in dSPACE to prepare the converters to be used with the FC-UC system.

6.3 Suggestions for Future Work

Based on the results of this work, the following recommendations for further research are suggested:

- A control strategy for selecting the phase-shift regime will need to be developed and an investigation needs to be conducted to optimize the power flow between the FC and the UC connected to the DC micro-grid. The control strategy will be implemented using dSPACE.
- Design and implementation of a controller that suits the optimum usage of the available energy to minimise the fuel consumption of the fuel cell when supplying a variable load.

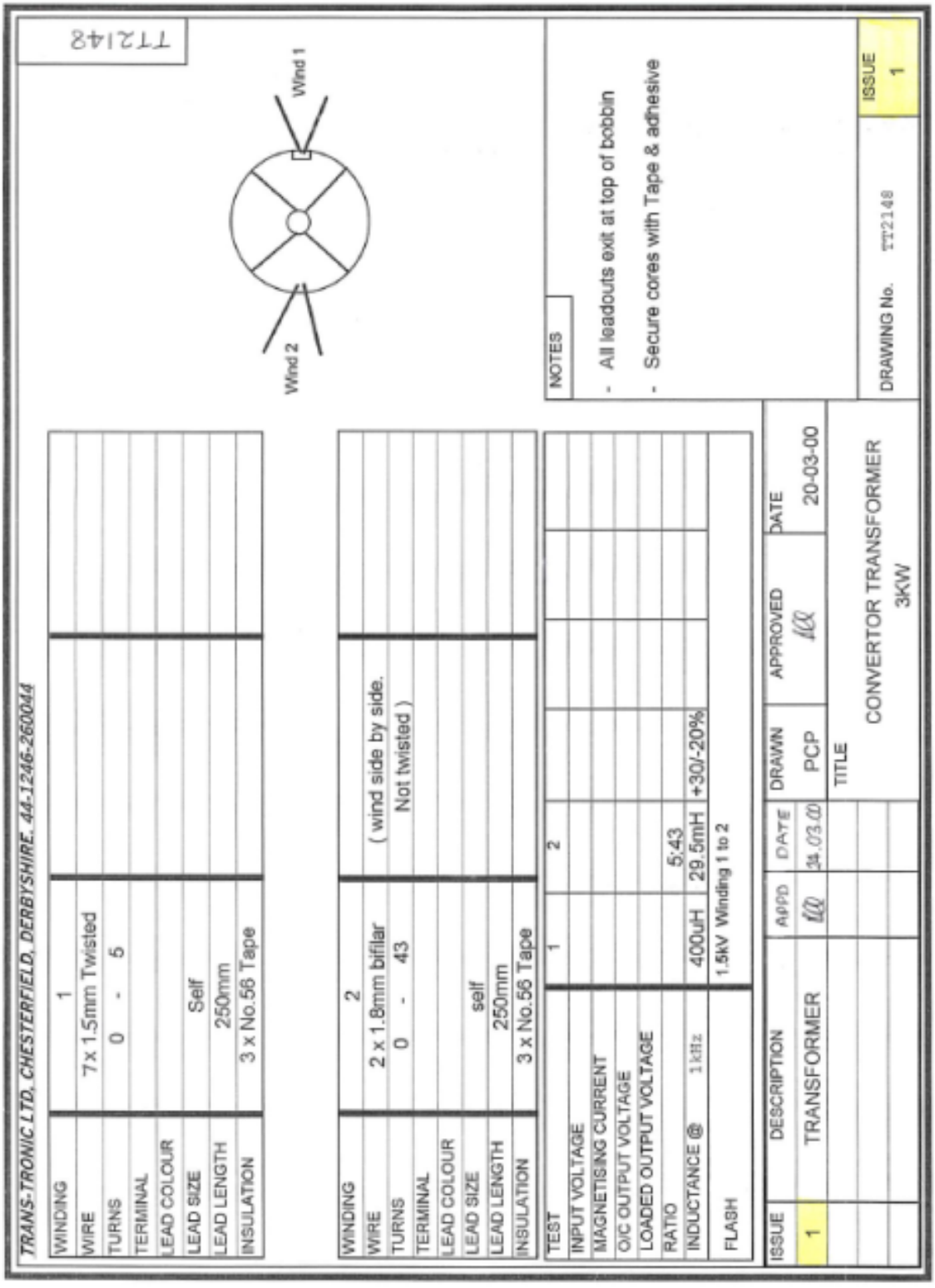
- Further research in the modelling and control of the power management for the FC–UC DC micro-grid is needed. The control strategy described in chapter two needs to be adjusted to optimise the bidirectional converter operation.
- Investigating the stability of the system made up of the incorporation of intermittent generators, e.g. PV, wind etc., and the operation of the micro-grid when it is linked to an AC distribution network via a bi-directional DC-AC converter.

Appendixes

Appendix A

HF Transformer Datasheet

The manufacture datasheet of the HF transformer that used in both the FBCFC and the BDC.



Appendix B

The Overlap Pulses Circuit Design in PSpice for the FBCFC

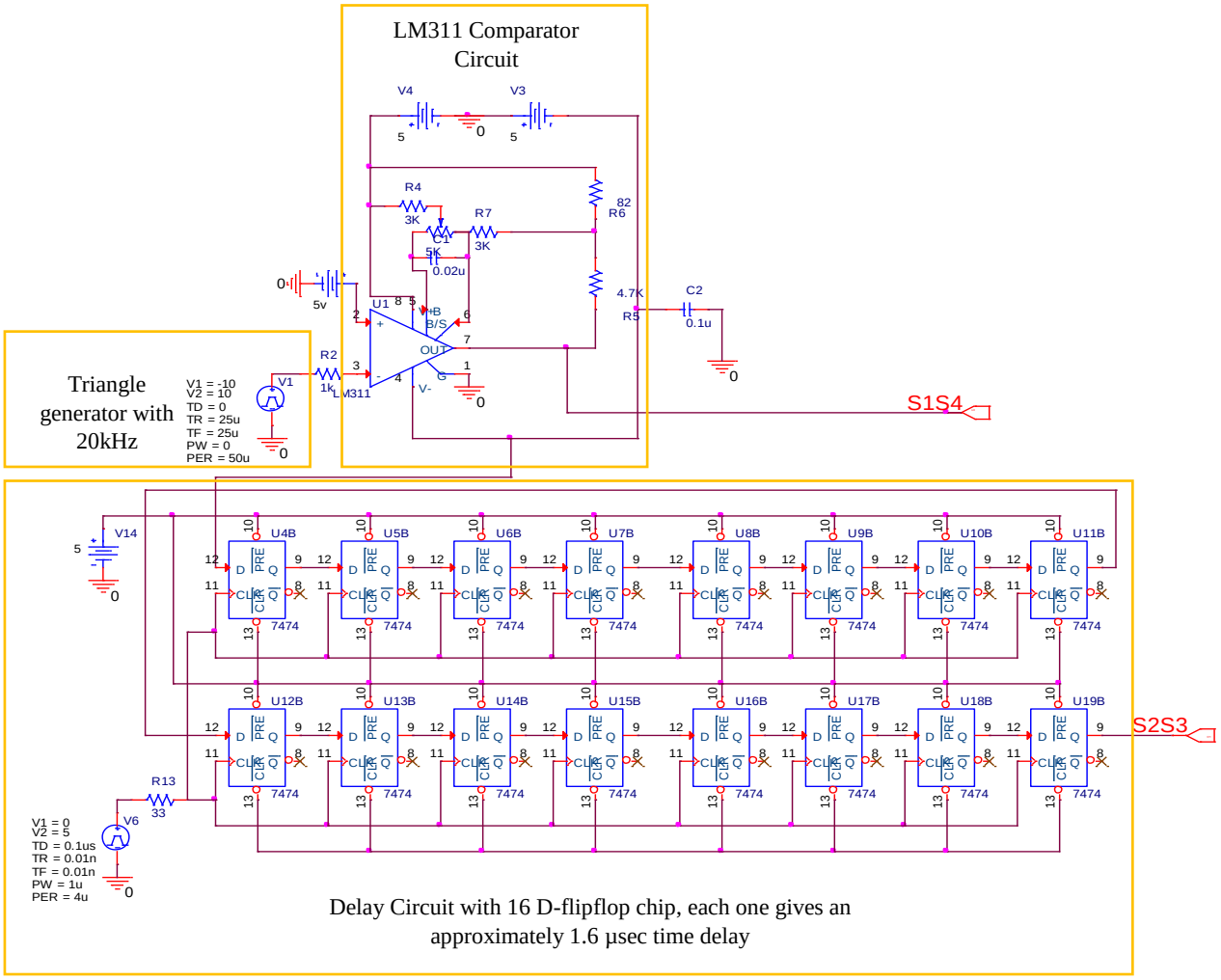


Fig. B. A circuit diagram for creating overlapping pulses for the FBCFC

Appendix C

Full Parameters Description of the Two loop Controller of the FBCFC [97]

Table C1: Parameters descried in equation 4.3 and 4.4

Parameters
$G_{io} = (g_3 V_{Ca} - D' g_1)/(D')^{\wedge 2}$
$a_o = V_{Ca} \cdot C_a / (g_3 V_{Ca} - D' g_1)$
$b_1 = L_b C_a / (D')^{\wedge 2}$
$b_2 = L_b g_3 / (D')^{\wedge 2}$
$G_{vo} = JR_o$
$k = CR_o/2$
$g_3 = (D')^{\wedge 2}/2 \cdot L_{lea} \cdot f_s$
$g_1 = ((T_s.D'/L_{lea})(V_{ca} - V_o/2n) - I_{Lb})$
$J = (D' + \Delta)/n$

Where, D' is the complementary of duty cycle D, V_{Ca} is the clamp capacitor voltage, L_b is the boost inductor, R_o is the load resistance, f_s is the switching frequency, L_{lea} the leakage inductance of the high frequency transformer, Δ is the steady-state duty cycle ,and n is the HF transformer turns ratio. The design parameters of the proposed converter are given in Table 4.5.

Table C2: FBCFC Parameters used in equations 4.3 and 4.4

Parameter	Value	Parameter	Value
Fuel Cell Voltage (v_{fc})	43-26 V	Boost Inductance (L_b)	475µH
Output Voltage (V_o)	650 V	Clamp Capacitance (C_a)	10 µF
Transformer Turns Ratio (n)	7.4	Leakage Inductance	2µH
Switching Frequency (f_s)	20 kHz	Duty Cycle (D)	0.01-0.8
Output Capacitor ($C=C_1=C_2$)	500µF	Output Power (P_o)	0.1-1.2kW

By using the coefficients given in table above with converter parameter values in table below and substituting these values in equations (4.3), and (4.4), the following expressions for $G_{vi}(s)$ and $G_{id}(s)$ was obtained:

$$G_{vi}(s) = 28.166 \frac{1}{0.176s + 1} \tag{C.1}$$

$$G_{id}(s) = 599.758 \frac{2.468e^{-6}s + 1}{1.515e^{-8}s^2 + 0.005938s + 1} \tag{C.2}$$

Appendix D

dSPACE Controller Blocks

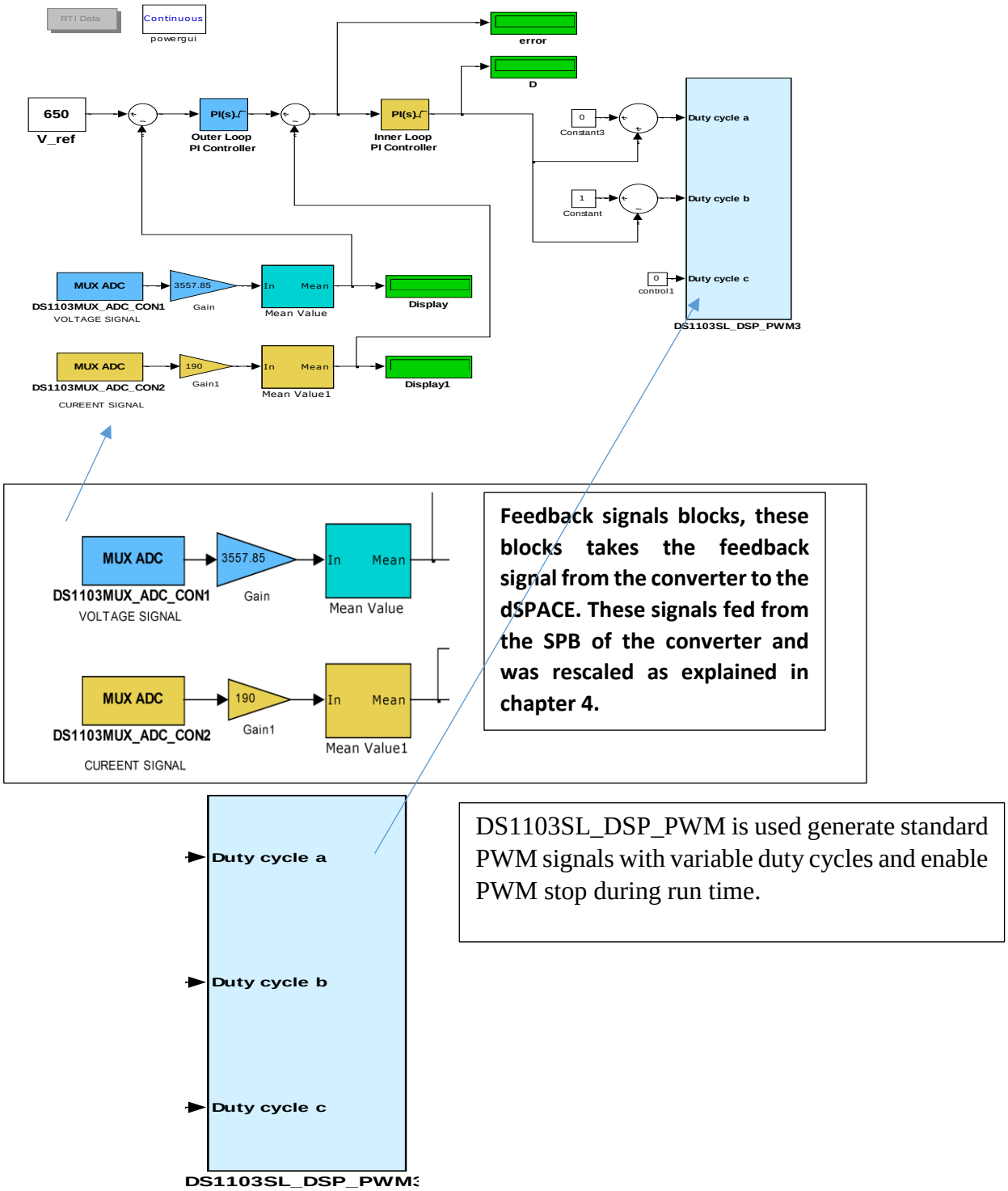


Fig.B FBCF Controller Blocks using dSPACE

Appendix E

CFC code generated by Matlab during the controller execution using dSPACE to control the FBCFC

```
                    Starting build procedure with RTI 6.7 (RTI1103,
23-May-2011)
Model: "closedloop_circuit" (C:\Documents and
Settings\Administrator\My
Documents\MATLAB\osamawork\closedloop_circuit.mdl)
-------------------------------------------------------------------------
  *** Using configuration set : "Configuration"
*** Working directory       : "C:\Documents and
Settings\Administrator\My Documents\MATLAB\osamawork"
*** Initializing code generation
## # Starting Real-Time Workshop build procedure for model:
closedloop_circuit
## # Generating code into build directory: C:\Documents and
Settings\Administrator\My
Documents\MATLAB\osamawork\closedloop_circuit_rti1103
Warning: Use fixed buffer size in 'closedloop_circuit/Mean
Value/Transport Delay'
is not selected. When generating GRT/ERT code, Simulink will
automatically use
fixed buffer of the initial buffer size set by user. Code generation
results and
simulation results may differ
Warning: Use fixed buffer size in 'closedloop_circuit/Mean
Value1/Transport
Delay' is not selected. When generating GRT/ERT code, Simulink will
automatically
use fixed buffer of the initial buffer size set by user. Code
generation results
and simulation results may differ
*** Optional User System Description File closedloop_circuit _usr.sdf
not available
## # Invoking Target Language Compiler on closedloop_circuit.rtw
## # Using System Target File: D:\dSPACE\matlab\r ti1103\tlc\r
ti1103.tlc
.
  ### Loading TLC function libraries
.....
## # Initial pass through model to cache user defined code
...
  *** Postprocessing RTI blocks
*** Starting I/O block checking
.
  *** Passed I/O block checking
## # Caching model source code
..................................................
  ### Writing header file closedloop_circuit.h
## # Writing header file closedloop_circuit _types.h
## # Writing source file closedloop_circuit.c
.
  ### Writing header file rtwtypes.h
## # Writing header file rt_SATURATE.h
## # Writing header file closedloop_circuit _private.h
.
```

```
  ### Writing header file rtmodel.h
## # Writing source file closedloop_circuit _data.c
## # Writing header file rt_nonfinite.h
## # Writing source file rt_nonfinite.c
.
  ### Writing header file rtGetInf.h
## # Writing source file rtGetInf.c
## # Writing header file rtGetNaN.h
.
  ### Writing source file rtGetNaN.c
## # TLC code generation complete.
          ### Generating TLC interface API.
        ......................
*** Generating file closedloop_circuit _rti.c
*** Generating file closedloop_circuit _rti.mk
*** Generating Variable Description File closedloop_circuit.trc

-------------------------------------------------------------------------
---------
                    NOTE: The following option in the Configuration
Parameters dialog has been
      used:

       Optimization:
       "Conditional input branch execution" On

      This leads to code optimization in which blocks are not computed
if their
      outputs are not required in the simulation step, for example, if
their
      output values are used as input for a Switch block and the
Switch
      currently routes another signal. When the corresponding output
signals
      are displayed in ControlDesk, their values are static.

        To ensure that the blocks are computed, turn off the
      "Conditional input branch execution" option and rebuild the
model.
       ---------------------------------------------------------------
---------------
     ....
    *** Found User-Code File closedloop_circuit _usr.c from 30-Nov-
2015 09:45:30
*** Found User Makefile closedloop_circuit _usr.mk from 30-Nov-2015
09:45:30
*** Optional User Variable Description File closedloop_circuit
_usr.trc not available
.
  ### Processing Template Makefile: D:\dSPACE\matlab\r ti1103\m\r
ti1103.tmf
## # closedloop_circuit.mk which is generated from D:\dSPACE\matlab\r
ti1103\m\r ti1103.tmf is up to date
## # Successful completion of Real-Time Workshop build procedure for
model: closedloop_circuit
*** Finished RTI build procedure for model closedloop_circuit (code
generation only)
```

Appendix F

Parameters and Components of the BDC

TABLE F: Parameters and Components of the BDC

Parameters & Components	Part/Value Practical
Rated Power	1.2kW
Input voltage	24-48V DC
Output voltage	650V DC
Output capacitors C_1, C_2	2x 470µF 400V Electrolytic + 1uF 1000V polyester in parallel
Main bridge MOSFETs	4x IRFP4110PBF (100V/120A) RDS(on)= 3.7mΩ
DC link side IGBTs	2x IRG4PSH71UDPBF 99A, 1.2kV
Gates Driver	SKHI21A Driver
Transformer leakage inductance L_{lea}	2µH
Transformer turns ratio n	5:37
series inductor $L_{SERIOUS}$	10 µH
Switching Frequency f_s	20kHz

Appendix G

Series Inductor Lt new core specifications

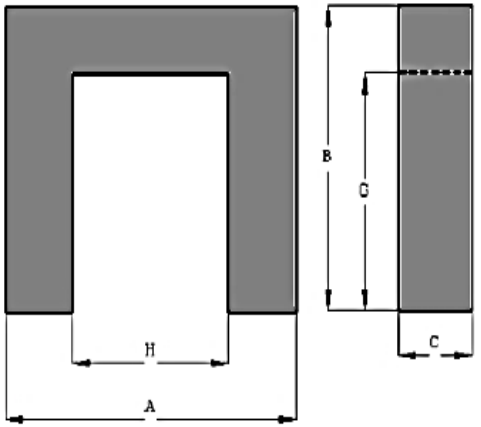
Magnetic Data (for a Pair of U100 115 Cores)

Parameter	Symbol	Value
Effective magnetic path length	L_e	300mm
Effective area of magnetic path	A_e	620mm²
Effective magnetic volume	V_e	186000mm³
$\sum L/A$	CL	0.48mm⁻¹

Magnetic Data (for a Pair of U93 Cores)

Parameter	Symbol	Value
Effective magnetic path length	L_e	185.8mm
Effective area of magnetic path	A_e	228.8mm²
Effective magnetic volume	V_e	42450mm³
$\sum L/A$	CL	0.81mm⁻¹

U100 & U93



Standard Characteristics of Material

Material /Core	μiac	Tanσ/μiau (x10⁻⁵) 10KHz	TC (°C)	f (MHz)	ρ (Ω. cm)	Bms mT (25°C)	Hcms Am	Pc (100KHz) @100mT (Kw/m3)		Pc (100KHz) @200mT (Kw/m3)	
								25°C	100°C	25°C	100°C
CF138 U100	4700+30% -20%	<2.5	220	<0.3	100	480	15	<155	<80	<800	<500
CF138 U93	5000+30% -20%	<2.5	220	<0.3	100	480	15	<155	<80	<800	<500

Appendix H

BDC Control Algorithm for Optimum Operation [97]

```
function [PSI,PS1,PS2,Puc_min_1,Puc_max_1,Puc_min_2,Puc_max_2] =
fcn(Puc,Vuc)

%% controller algorithm of the proposed optimal modulation scheme to
ensure min CPF interval with three modes of operation for the both
power flow directions (UCCM) and (UCDM:

%%MODE ISPM:   P_uc<P_min1 &P_min2
%%MODE ZCPFM:  P_min1&2<Puc<P_max1&2
%%MODE MCPFM: Puc>P_max1&2

n=7.4;
L=10e-6;%%L=Lt
w=2*pi*20e3;
% Puc=Vuc*Iuc;

              %%%%%%%%%%%% BOOST Operation %%%%%%%%%%%%%
             %%%%%%%%%%%% 2nVuc>== Vo %%%%%%%%%%%%%%%%%%%

Puc_min_1=(1/8)*L^(-1)*n^(-2)*pi*Vo^2*Vuc^(-1)*((-1/2)*n^(-
1)*Vo+Vuc)*w^(-1); %% Pmin for boost 2nVuc>Vo %%
Puc_max_1=(1/8)*L^(-1)*n^(-
1)*pi*Vo^2*Vuc*(Vo+2*n*Vuc)*(Vo^2+2*n*Vo*Vuc+2*n^2*Vuc^2)^(-1)*w^(-
1);%% Pmax for boost 2nVuc>Vo %%
Puc_min_2=(1/8)*L^(-1)*n^(-1)*pi*Vo^(-1)*Vuc*(Vo^2+(-
4)*n^2*Vuc^2)*w^(-1);%% Pmin for boost 2nVuc<Vo %%
Puc_max_2=(1/8)*L^(-1)*n^(-
1)*pi*Vo^2*Vuc*(Vo+2*n*Vuc)*(Vo^2+2*n*Vo*Vuc+2*n^2*Vuc^2)^(-1)*w^(-
1);%% Pmax for boost 2nVuc<Vo %%

 if (2*n*Vuc>=Vo)
    if(Puc>=0 && Puc < Puc_min_1)%this mode only for the small power
operation in order to get lower PSI than CPC
    PS1=0;
    PS2=((1/2).*Vo.^(-1).*Vuc.^(-
1).*(pi.*Vo.*Vuc+pi.^(1/2).*(pi.*Vo.^2.*Vuc.^2+(-
16).*L.*n.*Puc.*Vo.*Vuc.*w).^(1/2)))*(180/pi); %% inner phase-shift
angle

    elseif (Puc>=Puc_min_1 && Puc<=Puc_max_1)% this ensure PSI=0 for
particalr power range limited by Puc_min and Puc_max

    Phi1= (1/2).*Vo.^(-1).*(Vo.^2+2.*n.*Vo.*Vuc+2.*n.^2.*Vuc.^2).^(-
1).*(pi.*Vo.^3+(-
1).*(2.*pi).^(1/2).*(n.^2.*Vo.*Vuc.*(pi.*Vo.^2.*Vuc.*(Vo+2.*n.*Vuc)+(-
8).*(Puc/Vuc).*L.*n.*Vuc.*(Vo.^2+2.*n.*Vo.*Vuc+2.*n.^2.*Vuc.^2).*w)).^
(1/2));
    PS2=(180/pi)*((1/2).*n.^(-1).*(pi+(-2).*Phi1).*Vo.*Vuc.^(-1));%
for +ve
    PS1=(180/pi)*Phi1;

    elseif (Puc>Puc_max_1)  %this ensure lower Ip and PSI
```

```
    PS2=real((((1/2)*Vo^(-1)*Vuc^(-1))*(2*pi*Vo*Vuc-
sqrt(complex(2*pi^2*Vo^2*Vuc^2+(-
16)*L*n*pi*Puc*Vo*Vuc*w))))*(180/pi));
    PS1=PS2-(90);

              %%%%%%%%%%%% Buck Operation %%%%%%%%%%%%
            %%%%%%%%%%%% 2nVuc>== Vo %%%%%%%%%%%%%%%%%%%

    elseif (Puc<0 && Puc > -Puc_min_1)
    PS1=0;
    PS2=((1/2).*Vo.^(-1).*Vuc.^(-1).*((-1).*pi.*Vo.*Vuc+(-
1).*pi.^(1/2).*(
pi.*Vo.^2.*Vuc.^2+16.*(Puc/Vuc).*L.*n.*Vo.*Vuc.^2.*w).^(1/2)))*(180/pi
);

    elseif (Puc<= -Puc_min_1 && Puc>= -Puc_max_1)    % this ensure
PSI=0
    Phi1=(1/8).*Vo.^(-1).*(Vo.^2+2.*n.*Vo.*Vuc+2.*n.^2.*Vuc.^2).^(-
1).*(( -
4).*pi.*Vo.^3+4.*(2.*pi).^(1/2).*(n.^2.*Vo.*Vuc.*(pi.*Vo.^2.*Vuc.*(Vo+
2.*n.*Vuc)+8.*L.*n.*Puc.*(Vo.^2+2.*n.*Vo.*Vuc+2.*n.^2.*
Vuc.^2).*w)).^(1/2));
    PS2=(180/pi)*((-1/2).*n.^(-1).*(pi+2.*(Phi1)).*Vo.*Vuc.^(-1));
    PS1=(180/pi)*Phi1;


    else %this ensure lower Ip and PSI
     PS2=real((((1/2).*Vo.^(-1).*Vuc.^(-1))*((-
2).*pi.*Vo.*Vuc+sqrt(complex(2.*pi.*(pi.*Vo.^2.*Vuc.^2+8.*L.*n.*Puc.*V
o.*Vuc.*w)))))*(180/pi));
     PS1=PS2+(90);
    end
    %%the following equations are to determine PSI value for different
mode
    %%for the boost and buck operation under 2nVuc>Vo condition
        if(PS1>=0 && PS2>=0)
        PSI=(180/pi)*((1/2).*((1/2).*Vo+n.*Vuc).^(-1).*((-
1/2).*pi.*Vo+(PS1*(pi/180)).*Vo+n.*(PS2*(pi/180)).*Vuc)); %% for boost
        else
        PSI=(180/pi)*((1/2).*((1/2).*Vo+n.*Vuc).^(-
1).*((1/2).*pi.*Vo+(PS1*(pi/180)).*Vo+n.*(PS2*(pi/180)).*Vuc)); %% for
Buck
        end
                %%%%%%%%%%%% BOOST Operation %%%%%%%%%%%%
              %%%%%%%%%%%% 2nVuc<= Vo %%%%%%%%%%%%%%%%%%%
else

    if(Puc>=0 && Puc < Puc_min_2)
    PS1=0;
    PS2=((1/2).*Vo.^(-1).*Vuc.^(-
1).*(pi.*Vo.*Vuc+pi.^(1/2).*(pi.*Vo.^2.*Vuc.^2+(-
16).*L.*n.*Puc.*Vo.*Vuc.*w).^(1/2)))*(180/pi);

    elseif (Puc>=Puc_min_2 && Puc<=Puc_max_2)

    Phi1= (1/2).*Vo.^(-1).*(Vo.^2+2.*n.*Vo.*Vuc+2.*n.^2.*Vuc.^2).^(-
1).*(pi.*Vo.^3+(-
1).*(2.*pi).^(1/2).*(n.^2.*Vo.*Vuc.*(pi.*Vo.^2.*Vuc.*(Vo+2.*n.*Vuc)+(-
8).*(Puc/Vuc).*L.*n.*Vuc.*(Vo.^2+2.*n.*Vo.*Vuc+2.*n.^2.*Vuc.^2).*w)).^
(1/2));
```

```
    PS2=(180/pi)*((1/2).*n.^(-1).*(pi+(-2).*Phi1).*Vo.*Vuc.^(-1));%
for +ve
    PS1=(180/pi)*Phi1;

    elseif (Puc>Puc_max_2)
    PS2=real((((1/2)*Vo^(-1)*Vuc^(-1))*(2*pi*Vo*Vuc-
sqrt(complex(2*pi*(pi*Vo^2*Vuc^2+(-8)*L*n*Puc*Vo*Vuc*w)))))*(180/pi));
    PS1=PS2-(90);

                %%%%%%%%%%% Buck Operation %%%%%%%%%%%%
                   %%%%%%%%%%% 2nVuc<= Vo %%%%%%%%%%%%

    elseif(Puc<0 && Puc > -Puc_min_2)
    PS1=0;
    PS2=((1/2).*Vo.^(-1).*Vuc.^(-1).*((-1).*pi.*Vo.*Vuc+(-
1).*pi.^(1/2).*(pi.*Vo.^2.*Vuc.^2+16.*L.*n.*Puc.*Vo.*Vuc.*w).^(1/2)))*
(180/pi);

    elseif (Puc<= -Puc_min_2 && Puc>= -Puc_max_2)
    Phi1=(1/8).*Vo.^(-1).*(Vo.^2+2.*n.*Vo.*Vuc+2.*n.^2.*Vuc.^2).^(-
1).*(( -
4).*pi.*Vo.^3+4.*(2.*pi).^(1/2).*(n.^2.*Vo.*Vuc.*(pi.*Vo.^2.*Vuc.*(Vo+
2.*n.*Vuc)+8.*L.*n.*Puc.*(Vo.^2+2.*n.*Vo.*Vuc+2.*n.^2.*
Vuc.^2).*w)).^(1/2));
    PS2=(180/pi)*((-1/2).*n.^(-1).*(pi+2.*(Phi1)).*Vo.*Vuc.^(-1));
    PS1=(180/pi)*Phi1;

    else
     PS2=real((((1/2).*Vo.^(-1).*Vuc.^(-1))*((-
2).*pi.*Vo.*Vuc+sqrt(complex(2.*pi.*(pi.*Vo.^2.*Vuc.^2+8.*L.*n.*Puc.*V
o.*Vuc.*w)))))*(180/pi));
     PS1=PS2+(90);

    end
     %%the following equations are to determine PSI value for
different mode
    %%for the boost and buck operation under 2nVuc<Vo condition
       if(PS1>=0 && PS2>=0)
        PSI=(180/pi)*((1/2).*((1/2).*Vo+n.*Vuc).^(-1).*((-
1/2).*pi.*Vo+(PS1*(pi/180)).*Vo+n.*(PS2*(pi/180)).*Vuc)); %% for boost
        else
        PSI=(180/pi)*((1/2).*((1/2).*Vo+n.*Vuc).^(-
1).*((1/2).*pi.*Vo+(PS1*(pi/180)).*Vo+n.*(PS2*(pi/180)).*Vuc)); %% for
Buck
        end

end
```

Abbreviations

Name	Description
ACC	Active Clamp Circuit
BDC	Bidirectional DC–DC converter
CACC	Conventional Active Clamp Circuit
CFC	Current-fed converter
CHP	Combined heat and power
CPC	Conventional phase-shift control
DAB	Dual active bridge
DER	Distributed Energy Resources
DG	Distributed Generation
DSP	Digital signal processing
dSPACE	Digital Signal Processing and Control Engineering
FBCFC	Full bridge current-fed converter
FC	Fuel cell
LED	Light Emitting Diode
LTCFC	L-type current fed converter
MACC	Modified Active Clamp Circuit
MACC	Modified Active Clamp Circuit
MTRM	Modified triangular current modulation
OEM	Original Equipment Manufacturer
PED	Power Electronic Devices
PEMFC	Proton exchange membrane fuel cell
PV	Photovoltaic
PWM	Pulse Width Modulation
RHPZ	Right–half–plane–zero
SLPS	Simulink-PSpice
SOC	State-of-charge
SSW	Soft-switching
TRM	Triangular current modulation
TZM	Trapezoidal current modulation
UC	Ultra-capacitor
VFC	Voltage-fed converter
WECS	Wind Energy Conversion System
ZCS	Zero-current switching
ZVS	Zero-voltage switching

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