Methods for Investigating Interactions between Multiple Maximum Power Point Trackers in Photovoltaic Systems

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Abstract

Power loss due to photovoltaic (PV) module mismatch is a well-known problem for PV systems. The ability to recuperate the power lost has increased the popularity of distributed maximum power point tracking (DMPPT) systems using per-module 'power optimisers'; DC-DC converters that track the maximum power point (MPP) of each module.

There are concerns over systems with multiple maximum power point trackers (MPPTs) incurring unwanted interactions between MPPT controllers. A method for electrical engineers to analyse such systems is required. A lack of in-depth evaluation in literature has been addressed in this work through practical testing and development of a computer model for simulating various DMPPT systems.

To achieve acceptably accurate models of DMPPT power conditioning devices (PCDs) practical testing systems were employed: a solar emulator with real PV module, a real outdoor DMPPT test system and a PV emulator (PVE) developed during this work.

A fast and dynamically stable PV module emulator (PVME) was developed for testing a power optimiser. The PVME consists of a linear regulator and an analogue computation circuit for speed and flexibility. The steady-state operation of the power optimiser was tested with the PVME whereas the solar emulator obtained the true dynamic response. The extension of the PVME into a PV array emulator (PVAE) through the addition of a switched-mode controllable DC voltage source and a digital lookup table was considered.

PSpice 'block models' of PCDs were created for ease of reconfiguration using averaged equations of the switching power electronics and an equation for inverter ripple derived in this work. An MPPT model was developed in Simulink for co-simulation with the PSpice electrical models using SLPS. The overall DMPPT model showed similar behaviour to the outdoor test system. A number of proposed scenarios for investigating DMPPT system interactions have been suggested for further work.

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Table of Abbreviations

ACC	Analogue Computation Circuit
A/D	Analogue to Digital converter
CDCPS	Controllable DC Power Supply
CMPPT	Centralised Maximum Power Point Tracking
D/A	Digital to Analogue converter
DCPO	DC Power Optimiser
DLCS	Digital Lookup Computation System
DMPPT	Distributed Maximum Power Point Tracking
FFT	Fast Fourier Transform
FIT	Feed-In Tariff
GUI	Graphical User Interface
HUI	Hardware User Interface
LSB	Least Significant Bit
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracker
P&O	Perturb and Observe
PCD	Power Conditioning Device
PPPE	Photovoltaic Power Profile Emulation
PV	Photovoltaic
PVAE	Photovoltaic Array Emulator
PVE	Photovoltaic Emulator
PVI	Photovoltaic Inverter
PVME	Photovoltaic Module Emulator
PWM	Pulse Width Modulation
SCPVM	Separately Controlled Photovoltaic Module
SM	SolarMagic power optimiser
SMDCVS	Switched-Mode DC Voltage Source
STC	Standard Test Conditions

Chapter 1 Introduction

The photovoltaic (PV) demonstration facility at the University of Leicester is subjected to severe partial shading and so employs a number of power conditioning devices. The presence of such a system has sparked the inspiration for completing this study.

In this introductory chapter the current environmental, political and technical reasons for carrying out research into PV systems are discussed. Thereafter an indication of the theoretical background to the research presented in this thesis and the main aims are given. The chapter concludes with the structure for the remainder of the thesis.

1.1 Importance of Photovoltaic Power Generation

This section provides a brief overview of why PV is increasingly important as a means of electrical power generation.

1.1.1 Increase in Demand for Electrical Power

UN statistics given in [1] show that the global population is increasing by around a thousand million people every ten years as can be seen in Figure 1.1.

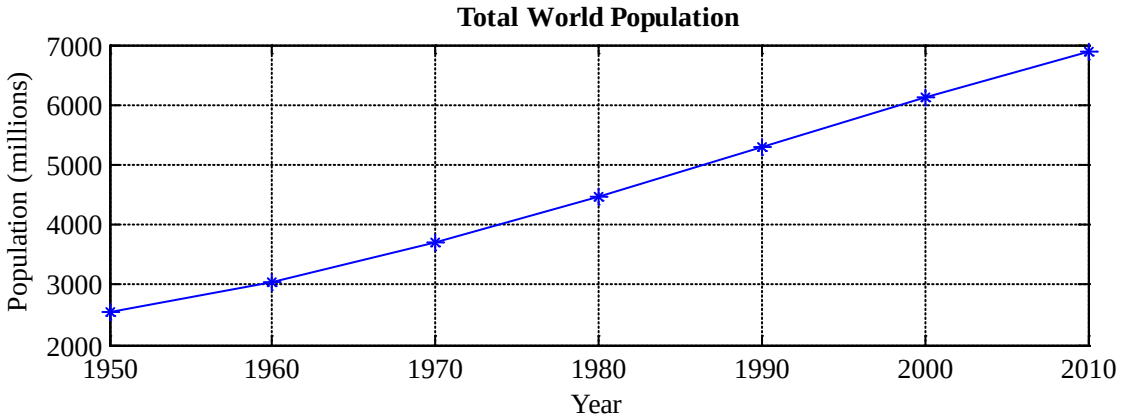


Figure 1.1: Estimated mid-year world population taken from UN statistics [1]

The graph in Figure 1.2, taken from [2], shows that the total global electrical energy generation has risen from around 5000 TWh in 1971 to around 20,000 TWh in 2009, a factor of around 4, whereas the global population has approximately doubled. This

shows that the energy demand per person is increasing at the same time as the number of people increases, further driving the increase in demand for electrical power.

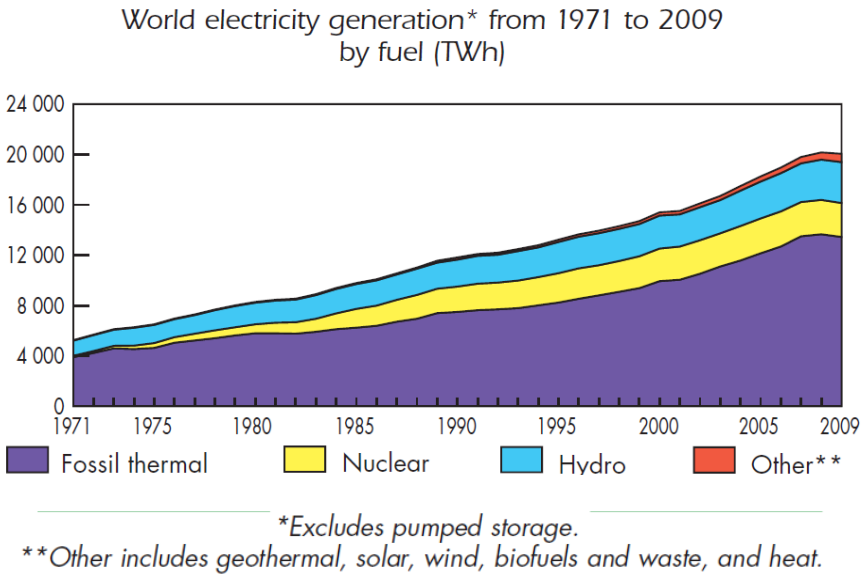


Figure 1.2: World Electricity Generation Statistics from the International Energy Association [2]

1.1.2 Concerns Over Fossil Fuels

In [2] it is shown that the percentage of electrical energy production from fossil fuels has fallen from 75.1% in 1973 to 67.1% in 2009. However this means there has been a rise in the absolute electrical energy production from fossil fuel of around 10,000 TWh. This reliance on the burning of fossil fuels for the production of energy has negative implications for the world.

Firstly, there is a limited supply of fossil fuels available since they were created naturally from the effect of millions of years of geological heat and pressure on organic matter. This means that if there is no practical alternative in place when the fossil fuel supply runs out there will be a global problem of energy shortage.

Secondly, there is the environmental cost involved with the use of fossil fuels. Fossil fuels are carbon based and to release their energy with current technology they have to

be burned. There are several by-products of this process that are harmful to the environment, including the greenhouse gas carbon dioxide.

A detailed history of the debate on climate change is provided by [3]. The cited study discusses how in the scientific community the greenhouse action of carbon dioxide is widely accepted as a contributing factor to global warming. The following explanation of the greenhouse effect was taken from the source:

‘To stay at a constant temperature, the Earth must radiate as much energy as it receives from the Sun... the Earth radiates most of its energy as infrared rays… Infrared radiation beaming up from the surface is intercepted by "greenhouse" gas molecules in the lower atmosphere, and that keeps the lower atmosphere and the surface warm…. The most important greenhouse gases are water vapour and carbon dioxide (CO_2).’

Thirdly, there are the problems of extracting and distributing fossil fuels. Over the last few years there have been environmental disasters that show the risk of drilling for and transporting oil, such as the Deepwater Horizon oil spill in the Gulf of Mexico and the Rena tanker that ran aground off New Zealand, both spilling oil into the sea. There have also been human disasters such as the Gleision Colliery in Wales, where four miners lost their lives after being trapped in a flooded coal mine.

1.1.3 Alternatives to Fossil Fuels

One of the main problems facing the world today is where to find the sources to sustain our ever more energy intensive lifestyles. Figure 1.2 and [2] show that the non-fossil fuel based energy sources used in the 2009 generation mix include nuclear fission (13.4%), hydro (16.2%), and other renewable sources (3.3% including geothermal, solar, wind, and biofuel).

Due to technical, environmental, and political reasons none of these ‘clean’ methods for electrical energy production in current use will be able to meet the global demand on

their own. It is likely that a combination of all of these sources will be needed if the global electricity demand is to be met.

There is the future possibility of nuclear fusion which may be able to provide a supply of clean electrical energy to meet the global demand. Researchers have demonstrated working fusion reactors; the problem lies in developing a reactor that is viable for commercial operation. How long this will take, and whether it will ever be achieved depends on who is asked.

1.1.4 Initiatives for Increased Use of PV Generation

Governments around the world have recognised the need to change to clean and sustainable sources of electrical energy production. This has led to greater funding of research, raising public awareness and incentive schemes for generating electricity from such sources.

One such scheme implemented by governments around the world is state funded payments to producers of electrical energy from clean renewable sources, commonly known as a feed-in tariff (FIT). In the UK the FIT and relaxed installation regulations for non-commercial systems make PV an attractive option for domestic power generation. This makes it possible to install a system on the roof of a house without the need for planning permission, and with a straightforward connection to the grid.

The electricity produced from such a system can also be used in the house, thus reducing the amount of electricity required from the supplier and reducing bills at the same time as receiving FIT payments for generation. This reduces the payback time for the owner to recover the costs of installing the system making it a more viable economic investment. This study will concentrate on domestic PV generation systems since industrial PV systems generally do not pose the same technical challenge in terms of

control and stability due to not requiring multiple maximum power point trackers (MPPTs).

1.2 Outline of the Research Topics and Goals

The previous section has briefly described the social and political incentives for research in the area of generation of renewable energy and particularly PV systems. This section provides an indication of the current technical challenges in PV systems that this study addresses.

1.2.1 Interactions in Multiple MPPT Systems

The electrical characteristics of a typical PV cell are given in Figure 1.3. The I-V curve shows a type of characteristic that could be associated with a current source that is voltage limited. The voltage limiting is not ideal since there is a gradual curving of the characteristic before the gradient steepens. This creates a smooth 'knee' as opposed to the square knee that you would expect for an ideal current source with voltage limiting.

It can be seen from the associated P-V curve that there is a distinct maximum in the power P that occurs around the middle of the knee of the I-V curve at the maximum power point (MPP). The MPP where the voltage $V = V_{mpp}$ and the current $I = I_{mpp}$, along with the open circuit voltage V_{oc}, where $I = 0$, and the short circuit current I_{sc}, where $V = 0$, are the 3 main points of interest on the I-V characteristic.

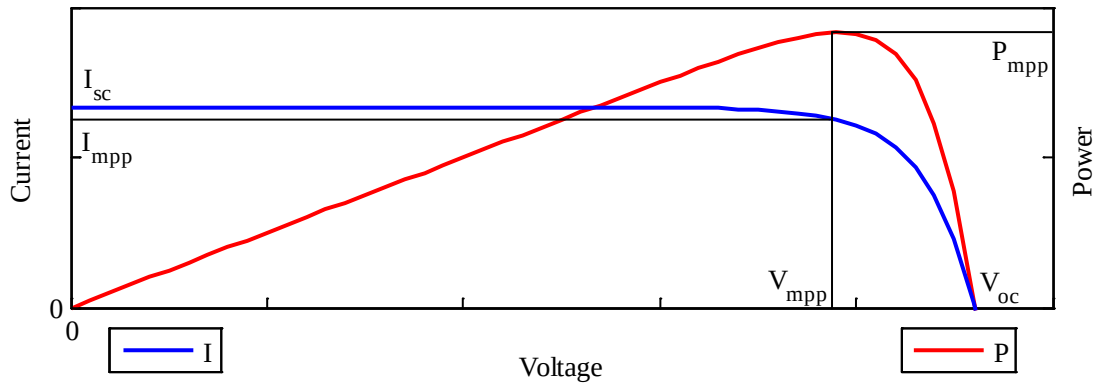


Figure 1.3: Electrical characteristics of a PV cell

The PV cell needs to be operated as close to the MPP for as much time as possible to obtain the best return on the investment of a PV system. Therefore power electronics systems are used to match the load characteristic to the PV characteristic. These power electronics are known as power conditioning devices (PCDs) and they are controlled using an MPP tracker (MPPT) algorithm to maintain proximity to the MPP. An example of a domestic PV system configuration is demonstrated in Figure 1.4. The system has 4 series connected PV modules and a central PCD, in this case embodied in an inverter.

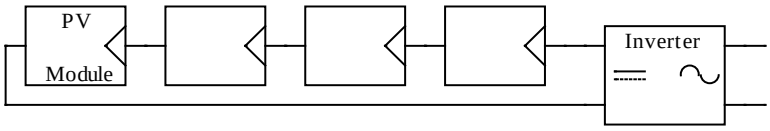


Figure 1.4: Typical domestic PV system

The PV characteristics in Figure 1.5 demonstrate a common problem in PV systems known as mismatch. Mismatch occurs when there is a shift in the I-V characteristic of a PV cell with respect to other PV cells in the system. This shift may have a number of causes including partial shading of a PV array where a shadow is cast onto a fraction of the PV cells. This problem is particularly prevalent in domestic PV systems where there is often a chimney, tree or other nearby object that causes a shadow to fall on the PV array.

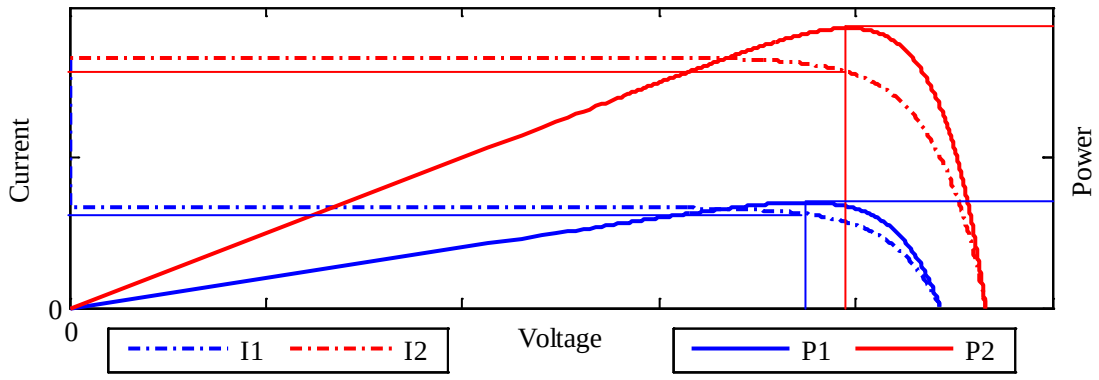


Figure 1.5: Mismatched PV cells

The example given in Figure 1.5 is for two PV cells with one of the cells, cell 1, receiving only 40% of the level of irradiance of the other PV cell, cell 2. The shifting of the I-V curves causes a number of problems when the PV cells are series connected. Since a PV cell will typically have a V_{mpp} of less than 0.6V they are usually connected in series to obtain a practical voltage level.

Figure 1.5 shows that the I_{mpp} of cell 1 is around 40% of cell 2. When the two PV cells are directly connected in series they are forced to share the same current. It is therefore impossible to operate both PV cells at their MPP. Also if the current through a number of series connected PV cells is allowed to rise above the I_{sc} of the underperforming PV cell, the other cells will start to feed power into this cell.

The extra power dissipation in cell 1 will create a 'hot-spot' where the cell starts to overheat. The excessive heating of the cell can cause accelerated degradation or even failure of the PV cell. To protect against the hot-spot problem the majority of PV modules come fitted with bypass diodes. These diodes are connected across a number of series connected PV cells as illustrated by Figure 1.6. If mismatch occurs in the PV module and the current rises above I_{sc} for the underperforming cells the diode will limit the reverse voltage across them by providing an alternative path for the current to flow.

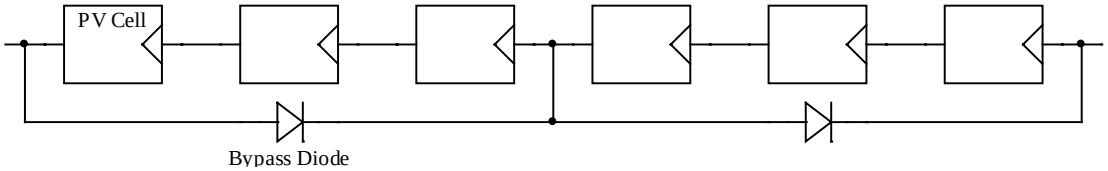


Figure 1.6: Bypass diode configuration

The characteristics of the mismatched PV cells of Figure 1.5 are shown again here in Figure 1.7 with the additional characteristics created from the series connection of cell 1 and cell 2 that results in the current I_s and power P_s. It is assumed here that there is an

ideal bypass diode across cell 1 that limits V1 to 0V for any current above the I_{sc} of cell 1.

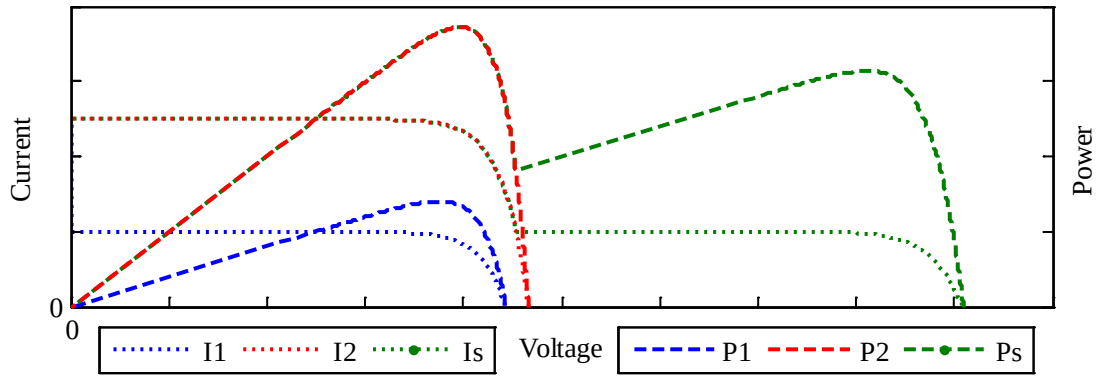


Figure 1.7: Mismatched PV cells connected in series

The coincidence of the series characteristics and the cell 2 characteristics for currents above the I_{sc} of cell 1 shows that as well as preventing hot-spots in the underperforming cells the bypass diodes also allow the normal cells to operate at their MPP.

However, it can also be seen in Figure 1.7 that the bypass diode creates a 'stepped' I-V curve which can lead to multiple local maxima in the power. This may confuse the MPPT algorithm of the connected PCD and cause it to stick at a local maximum that is at a lower power than the true MPP of the PV array.

For example, most MPPT algorithms will start at V_{oc} and reduce the voltage until the MPP is reached. In the case of Figure 1.7 this would mean that the MPPT would find the local maximum of lower power at the higher voltage. If this is allowed to go on for a considerable time the energy lost from not operating at the true MPP would become significant.

In chapter 2 a short discussion is included on studies that have been carried out on MPPT algorithms that are able to find the true MPP of series connected PV cells or modules. However, even when operating at the true MPP the power that could be obtained from bypassed PV cells is being lost. An alternative solution, distributed

maximum power point tracking (DMPPT) is able to recuperate most of the power of the underperforming PV cells whilst maintaining the MPP of the unaffected cells.

The principle of DMPPT is to break down the PV array into sections and provide each section with a PCD to perform MPP tracking. The PCD maintains the MPP of an underperforming section by converting the output to match the I_{mpp} of the other sections. The example of Figure 1.8 utilises per-module power optimisers where the PCD takes the form of a DC-DC converter.

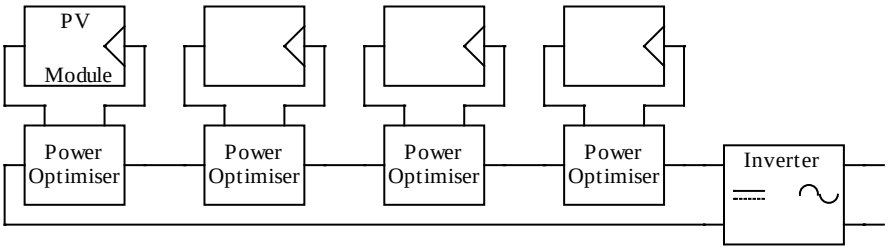


Figure 1.8: Per-module power optimisers

There are concerns over whether having multiple MPPT controllers may cause problems due to unwanted interactions. In the example of Figure 1.8 it is not obvious what would happen if each of the PV modules had a different I_{mpp}. Normally the power optimiser MPPT would try to match the PV characteristic to the load characteristic. However, the load current would depend on the other 3 power optimisers and so it is possible that the MPPTs could interact. This is further complicated in situations where the inverter is also equipped with an MPPT.

The possible interactions between the MPPT controllers may lead to problems such as the system becoming unstable or the power optimisers not tracking the MPP of the PV module correctly. This could result in less power being delivered than without the power optimisers.

To investigate possible interactions in DMPPT systems and their effect on overall performance, computer simulation is developed in this study. The system configuration

is easily changed due to the ‘black-box’ nature of the model. The electrical models of the PV system components are constructed in OrCAD Capture in such a way that the user need only place the representative parts and connect them as an electrical circuit.

All of the MPPT control is performed by a MATLAB Simulink model and linked to the PSpice model derived from the Capture circuit using the SLPS interface tool, provided in OrCAD thus combining the detailed electrical simulation abilities of PSpice with the ability to easily generate control algorithms in Simulink.

The main aim of the reported study is therefore the development of a computer model of DMPPT systems. The developed model can be executed for analysis of DMPPT systems to determine whether any undesired interactions could occur and under what conditions. Suggestions of required investigations for various system configurations and scenarios that may lead to such interactions are provided.

1.2.2 Emulator for Investigating Power Conditioning Devices

The previous subsection defines the main objective of this investigation as the development of a model for analysing DMPPT systems. This involves combining a model for each component of a DMPPT system. To obtain an accurate simulation experimental data is required for verification of the PCD models.

The ever-changing environmental conditions on outside PV arrays make repeatable controlled testing of PCDs extremely difficult. The irradiance and temperature would need measuring and the data used to convert all of the test results to a standard level for both. This is time consuming and may lead to inaccuracies.

An alternative method is to run an indoor test setup for analysing the PCDs. The construction of a test rig for testing a PV inverter utilising real PV modules and solar emulators (controllable uniform light sources) is costly and requires a large space. It also restricts the testing to the type of module used in the rig.

A preferable method is to use a PV emulator which is a controllable DC power supply (CDCPS) whose output will follow the electrical characteristic of a PV module or array. As discussed in Chapter 3 there are various commercial CDCPSs available that are either purpose-built for use as a PV emulator or can be combined with a pc and specific software to create a PV emulator. However, these CDCPSs are expensive and most do not have the specification required for this investigation.

It is therefore beneficial to design and construct a purpose-built PV emulator for indoor testing of the PCDs as this is cheaper. Moreover its specification can be designed to match the requirements of this research. The secondary goal of this work is the development of such a device.

1.3 Structure of Thesis

The objectives of the work presented in this thesis have been described in the previous section. This section outlines how this work is presented in the remainder of the thesis.

In Chapter 2 a more detailed analysis of the problems addressed is given with reference to literature. This starts with the operating principles of PV cells, modules and systems before providing further details on the causes and effects of mismatch and the methods for reducing these effects. The various techniques of modelling of PV cells and modules are discussed and the choice of models used throughout the thesis is justified. Finally evidence of the relevance and novelty of the main objective of the study is provided.

Chapter 3 provides a discussion on the PV emulator. The various methods for controlling the electrical output characteristic are defined and a comparison is given. A review of PV emulators with details of commercially available emulators and an overview of the literature are presented.

Chapter 4 goes on to describe the methods used for controlling the PV emulators developed in this study. The first section details the analogue computation method that

is used for a PV module level emulator and the second section reports the more flexible digital lookup computation method developed for a PV array emulator.

The development of a controllable DC power supply (CDCPS) for use in a PV emulator is demonstrated in Chapter 5. A standard commercial power supply is tested to show why it is not suitable for use in a PV emulator. A linear regulator output stage that overcomes the limitations of the commercial power supply is devised and tested. The design of a switching power electronics circuit for limiting the voltage drop across the linear output stage in a high voltage PV array emulator is discussed.

The testing of power conditioning devices (PCDs) is described in Chapter 6. The setup for each test is defined and the main results of the tests are analysed. The investigations include the indoor testing of a SolarMagic (SM) per-module PCD using a solar emulator, and also using a PV emulator, the testing of an SMA SB700 inverter on an outdoor PV array, and the outdoor testing of a distributed maximum power point tracker (DMPPT) system.

The computer model of the DMPPT system is developed in Chapter 7 with the technique of using non-switching blocks to represent the various system components. The generation of a PSpice model for a PV module with the ability to set the environmental conditions is described. The SM model is created in PSpice and a Simulink model of an MPPT is designed for use with the SM model. The SM model is verified using the Chapter 6 test results. A model of the SB700 inverter is developed and the MPPT model modified to represent the SB700 MPPT which is verified with the experimental results in Chapter 6. With each system component model completed the various models are combined to form the model of a DMPPT system which is compared with the results of the outdoor system in Chapter 6.

Chapter 8 goes on to describe scenarios that may lead to possible unwanted interactions in a DMPPT system for which the model developed in Chapter 7 can be used to analyse if and when any adverse interaction occurs.

Chapter 9 provides the conclusions drawn from this study and a proposal of future investigations for continuing the study. The conclusions are broken down into sections: the construction of a PV emulator and the creation of a ‘black-box’ model for a PV.

Chapter 2 Operation of PV Cells, Modules and Systems

In Chapter 1 the objectives of this study were introduced with a brief description of the background. This chapter elaborates on the theoretical principles behind the work carried out during the research. It also enables the reader to gain a proper understanding of why the development of methods for investigating interactions between multiple maximum power point trackers (MPPTs) was deemed necessary, based on the reviewed literature.

2.1 Principles of PV Power Generation

Knowledge of the fundamentals of photovoltaics (PV) is essential for understanding the operation of PV power generation as part of an electrical power generation system. This knowledge also allows development of a model to predict the electrical behaviour. A brief description of the PV principles and the derived electrical models are presented in this section.

The type of PV cell used in a generation plant is a trade-off between cost and efficiency. The more expensive but higher efficiency crystalline silicon based PV technologies are used for systems where space is limited, including domestic systems. The cheaper but less efficient thin film technologies are used in large solar farms where there is more space. Since this study is concerned with domestic PV systems only crystalline silicon based PV cells will be considered here.

2.1.1 PV Cell Operation

A silicon PV cell is constructed as a semiconductor junction between doped n-type and p-type layers - it is essentially a diode that is exposed to light radiation. The Shockley diode equation (2.1) holds for a PV cell in the absence of light where the net current through the diode I varies exponentially with the forward bias voltage V_d. The dark

saturation current I_o is a property of the semiconductor device itself and the physical constants q and k are the electron electrical charge and Boltzmann's constant respectively. The absolute temperature T also has an effect.

$$I = I_o \left[e^{\left(\frac{qV_d}{kT}\right)} - 1 \right] \qquad \textbf{(2.1)}$$

With zero external bias voltage the diffusion current across the transition region due to the high concentration of carriers either side will balance the drift current due to the voltage caused by the separated charges and the net current through the device is therefore zero.

When a diode junction is exposed to light radiation a proportion of the photons that are travelling through the material will be absorbed by a valence electron as shown in Figure 2.1. The energy of the absorbed photon is transferred to the electron elevating it from the valence band to the conduction band where it is free to move through the semiconductor material. The process also leaves a hole in the valence band that is free to move and thus an electron-hole pair has been created by the photon.

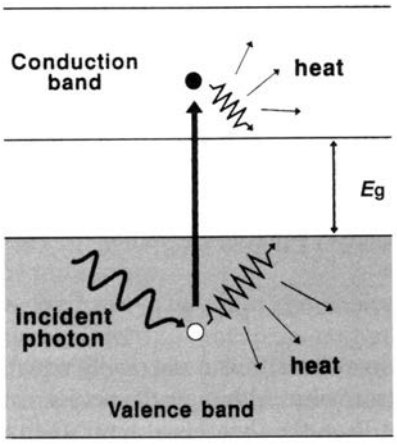


Figure 2.1: The generation of electron-hole pairs by light [4]

For the incident photon to be absorbed by an electron it must be of a higher energy than the band-gap energy E_g of the material. This limits the spectrum of light that can be absorbed by the semiconductor.

In a junction device the high concentration of electrons and holes either side of the transition region will cause the created electron and hole to travel in opposite directions by diffusion. If the terminals of the device are left open, the increase in charge either side of the transition region will give rise to a forward bias voltage across the junction creating a current to balance the additional diffusion. Therefore a voltage is created from the absorption of a photon, and this is called the photovoltaic effect.

The PV cell can be represented by the ideal equivalent circuit in Figure 2.2 where the current source I_{ph} represents the photo-generated diffusion current in the cell and the diode D represents the junction.

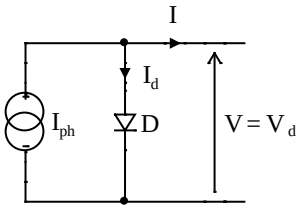


Figure 2.2: Ideal equivalent circuit of a PV cell

From the ideal equivalent circuit of Figure 2.2 and the Shockley equation (2.1), equation (2.2) can be derived to describe the behaviour of a PV cell. The number of electron-hole pairs generated is proportional to the incident irradiation G and so I_{ph}, which is due to the creation of the charge carriers, will also be proportional to G. The electrical I-V characteristic of the ideal solar cell and the effect of G on it are shown in Figure 2.3.

$$I = I_{ph} - I_o \left[e^{\left(\frac{qV_d}{kT}\right)} - 1 \right] \qquad \textbf{(2.2)}$$

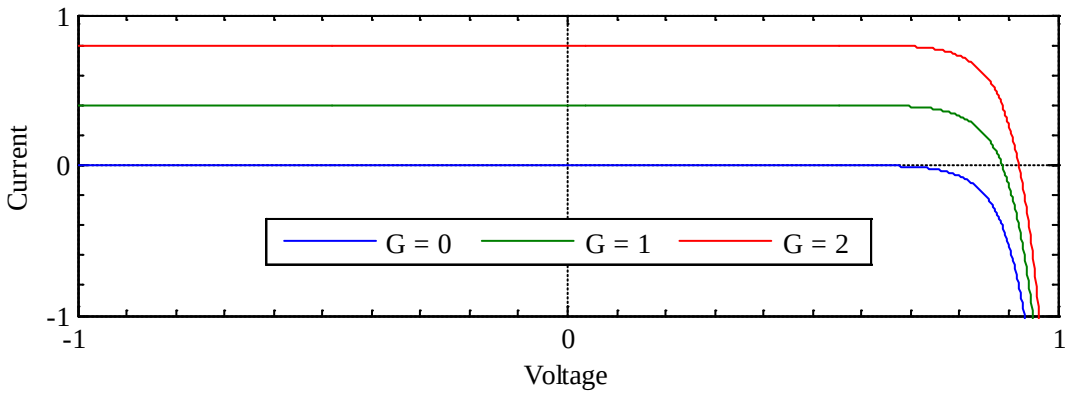


Figure 2.3: Effect of G on the I-V characteristic (arbitrary units)

The losses incurred by a PV cell are described in [4]. In brief these are the fundamental losses associated with the conversion of photons into charge carriers, recombination of charge carriers due to impurities, recombination at the surface and the metal contacts of the cell, and ohmic losses from the flow of current through the cell and the metal contacts. As this study is only concerned with the electrical behaviour of the PV cell the fundamental losses can be combined and accounted for using the linear factor K_{ph} in equation (2.3).

$$I_{ph} = K_{ph} G \qquad \textbf{(2.3)}$$

Since K_{ph} is a constant, equation (2.3) can be re-arranged and equated at two separate levels, G and G_{ref}, to give equation (2.4) for determining I_{ph} at G from the reference point $I_{ph}|_{ref}$.

$$I_{ph} = I_{ph}|_{ref} \frac{G}{G_{ref}} \qquad \textbf{(2.4)}$$

To incorporate both the ohmic and recombination losses the ideal equivalent circuit can be modified to give the equivalent circuit of Figure 2.4 which is described by equation (2.5). The ohmic losses are represented by the series resistance R_s to give a voltage drop that is proportional to the net current through the PV cell, whereas the recombination losses are represented by the parallel resistance R_p. In equation (2.5) the

γ term is the diode ideality factor, V_d is the diode junction voltage and V is the PV cell terminal voltage. The relation between V_d and V is given in equation (2.6).

$$I = I_{ph} - I_o\left[e^{\left(\frac{qV_d}{\gamma kT}\right)} - 1\right] - \frac{V_d}{R_p} \qquad \textbf{(2.5)}$$

$$V_d = V + IR_s \qquad \textbf{(2.6)}$$

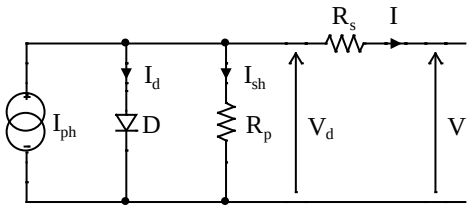


Figure 2.4: Equivalent circuit of a PV cell including losses

Substituting (2.6) into (2.5) results in equation (2.7) that shows the interdependence of the PV cell output variables I and V. The effects of R_s and R_p on the I-V characteristic of the PV cell are displayed in Figure 2.5. An increase in R_s from 0 will lessen the steepness of the curve between the open circuit voltage V_{oc} and the maximum power point (MPP). A reduction in R_p from infinity increases the slope of the curve between the short circuit current I_{sc} and the MPP.

$$I = I_{ph} - I_o\left[e^{\left(\frac{q(V+IR_s)}{\gamma kT}\right)} - 1\right] - \frac{V + IR_s}{R_{sh}} \qquad \textbf{(2.7)}$$

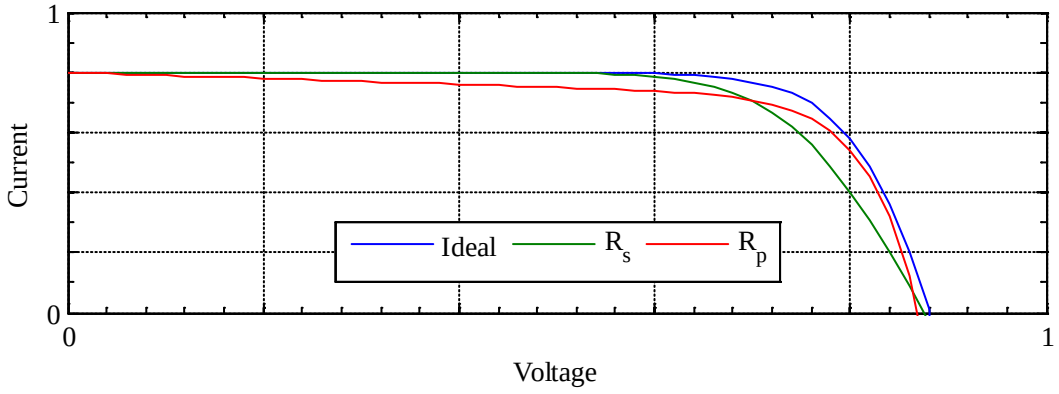


Figure 2.5: Effect of R_s and R_p on the I-V characteristic (arbitrary units)

2.1.2 PV Modules

According to [4] the theoretical maximum value for the V_{oc} of a single junction silicon PV cell is limited to around 0.7V. V_{mpp} would be even lower than this making it difficult to extract the power directly from the cell in an efficient manner. To obtain a practical level for V_{mpp} a number of cells are connected in series to form a PV module. Occasionally PV modules may also have parallel connected cells but generally consist of a single series connected 'string' of PV cells.

An example I-V characteristic of a PV module - the BP7175S - is displayed in Figure 2.6. The BP7175S consists of 72 series-connected mono-crystalline silicon PV cells that provide a V_{oc} of 44.2V, i.e. approx. 0.614V per PV cell. The MPP of the module is given as 36V and 4.9A.

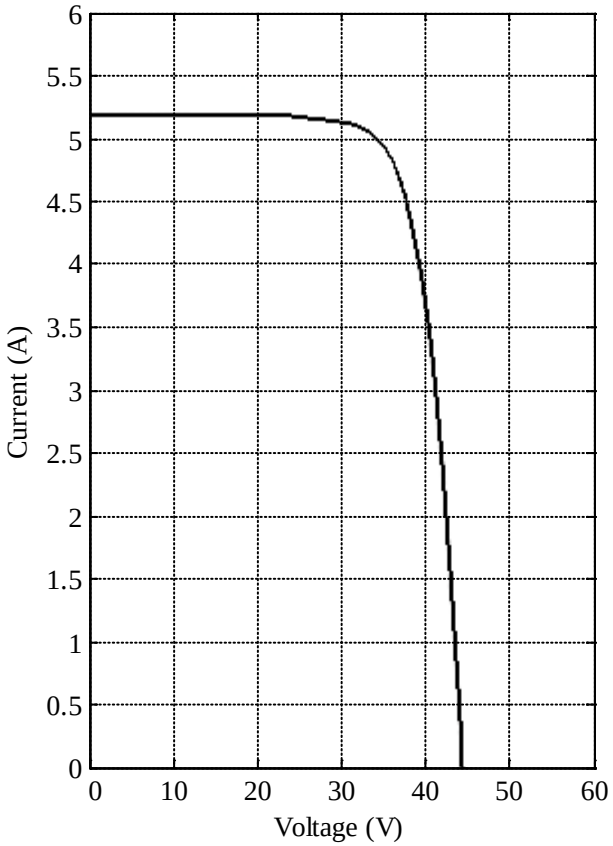


Figure 2.6: I-V characteristic for BP7175S taken from the datasheet

The characteristics and data provided by a manufacturer are for a particular set of environmental conditions, the so-called standard test conditions (STC), so that a comparison between different PV modules can be made. STC assumes a panel

temperature of 25°C, an irradiance level of 1000Wm^{-2} and a spectral distribution of the incident light of an air mass of 1.5 (AM1.5).

Figure 2.7 shows that an air mass of 1 represents the sunlight travelling directly through the earth's atmosphere along a path normal to the earth's surface. If the sunlight travels at a non-normal angle through the atmosphere then the air mass index is approximately the inverse of the cosine of the angle from the normal.

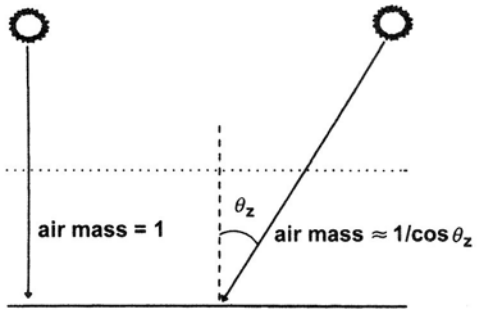


Figure 2.7: Definition of air mass [4]

2.2 PV Systems

The previous section has described the characteristics of a PV module including the environmental effects of temperature and irradiance. This subsection will introduce the other elements of a PV system, the power conditioning devices (PCDs), and indicate the various system topologies constructed from PV modules and PCDs.

2.2.1 MPP Tracking

Chapter 1 describes the use of PCDs in a PV system to maintain proximity to the MPP of the PV modules with a maximum power point tracker (MPPT) algorithm. An overview of MPPTs is provided in this subsection.

A comparison of MPPT techniques has been presented in [5] which states that 'at least 19 distinct methods have been introduced in the literature with many variations on implementation'. The authors produced Table 2.1 and have discussed the suitability of each method with regards to the application requirements. For domestic PV systems the MPPT technique should be easy to implement whilst providing constant tracking of the

MPP. Most PCDs will operate a 'hill-climbing' or 'perturb and observe' (P&O) algorithm since they can be easily implemented in a cheap microcontroller.

MPPT Technique	PV Array Dependent	True MPPT	Analogue or Digital	Periodic Tuning	Convergence Speed	Implementation Complexity	Sensed Parameters
Hill-climbing/P&O	No	Yes	Both	No	Varies	Low	Voltage, Current
Incremental Conductance	No	Yes	Digital	No	Varies	Medium	Voltage, Current
Fractional V_{OC}	Yes	No	Both	Yes	Medium	Low	Voltage
Fractional I_{SC}	Yes	No	Both	Yes	Medium	Medium	Current
Fuzzy Logic Control	Yes	Yes	Digital	Yes	Fast	High	Varies
Neural Network	Yes	Yes	Digital	Yes	Fast	High	Varies
RCC	No	Yes	Analogue	No	Fast	Low	Voltage, Current
Current Sweep	Yes	Yes	Digital	Yes	Slow	High	Voltage, Current
DC Link Capacitor Droop Control	No	No	Both	No	Medium	Low	Voltage
Load I or V Maximisation	No	No	Analogue	No	Fast	Low	Voltage, Current
dP/dV or *dP/dI* Feedback Control	No	Yes	Digital	No	Fast	Medium	Voltage, Current
Array Reconfiguration	Yes	No	Digital	Yes	Slow	High	Voltage, Current
Linear Current Control	Yes	No	Digital	Yes	Fast	Medium	Irradiance
I_{mpp} or V_{mpp} Computation	Yes	Yes	Digital	Yes	N/A	Medium	Irradiance, Temperature
State-based MPPT	Yes	Yes	Both	Yes	Fast	High	Voltage, Current
OCC MPPT	Yes	No	Both	Yes	Fast	Medium	Current
BFV	Yes	No	Both	Yes	N/A	Low	None
LRCM	Yes	No	Digital	No	N/A	High	Voltage, Current
Slide Control	No	Yes	Digital	No	Fast	Medium	Voltage, Current

Table 2.1: Major characteristics of MPPT techniques [5]

Both the hill-climbing and P&O techniques work on the principle of applying a perturbation to the system and determining the trajectory of the PV power. The preceding perturbation and power trajectories will determine the subsequent direction of the perturbation as illustrated in Table 2.2. In the case of the hill-climbing technique, the perturbation is applied directly to the duty cycle of the PCD power electronics whereas the P&O method will apply a perturbation to the PV voltage.

Perturbation	Change in Power	Next Perturbation
Positive	Positive	Positive
Positive	Negative	Negative
Negative	Positive	Negative
Negative	Negative	Positive

Table 2.2: Summary of hill-climbing and P&O algorithm [5]

2.2.2 Overview of PCDs

The previous subsection indicated that the MPP tracking in a PV system is implemented through PCDs. To allow tracking of the MPP the resistance of the connected load must be matched to the output resistance of the PV generator at MPP. The tracking is required since both the MPP and the resistance of the load will vary. The PCD is

required as an intermediate converter stage to provide the resistance matching between the generator and load. The converter will invariably be of the switched variety to maintain a high efficiency.

In a grid-connected PV system there is a requirement for inversion of the DC power generated by the PV into AC power that can be fed into the grid. The PCD used in this case would be an inverter. A PV system may also utilise DC-DC converters as PCDs, for instance as an input stage to the inverter to increase the operating voltage range of the PV generator.

2.2.3 PV System Topologies

The system topology depends on the combination of PV modules and PCDs used. The topologies considered in this study are all grid-connected as the majority of domestic PV plants are connected to the AC grid. The following terminology is used in this work.

String	A series connection of PV modules.
Array	A collection of PV modules that form a PV generator. An array can consist of a single string or a number of strings connected in parallel.

Central Inverter: This topology consists of a PV array that is connected to a single inverter. The inverter performs both the MPPT function and the DC-AC inversion. A variant on this topology is the use of a DC-DC converter input stage for the inverter. The DC-DC converter takes over as the MPPT. This topology is common in commercial PV plants.

String Inverter: This topology involves the use of more than one inverter. Each inverter has its own string and MPPT. The inverters are then connected in parallel on the AC side.

Per-module Inverters: Each PV module in the array is connected directly to an inverter. The inverters are then connected in parallel on the AC side. These are known as ‘micro-inverters’ or ‘AC modules’.

Per-module Converters: Each PV module in the array is connected to a DC-DC converter. The DC-DC converter outputs are connected, usually in series and fed in to a central inverter.

2.3 Mismatch of PV Cells and Modules

The concept of mismatch in PV systems introduced in Chapter 1 is described in more detail in this section. To recap, mismatch occurs when a variation in the MPP of interconnected PV cells and modules leads to differences in their respective I_{mpp} and V_{mpp}. Particular attention is paid to the various causes and attempts at reducing the effects.

2.3.1 Causes of Mismatch

There are various factors that can produce a difference in the electrical characteristics of PV cells. Firstly, all PV cells are manufactured to a tolerance; in [6, 7] the authors offer methods for classification of manufacturing tolerances of PV cells. However, the mismatch effect due to manufacturing tolerance is minimal and is not to be considered in this study.

Investigations into the degradation of PV modules carried out on outdoor PV systems have been reported in [8, 9]. It has been shown that the performance of PV modules within the same array will degrade at varying rates due to localised problems such as the oxidation of cell contacts. The problem of degradation takes effect over a number of years and can therefore be monitored. Most manufacturers of PV modules will offer a guarantee so any prematurely degraded PV modules should be replaced.

As reported in [10-21] the main concern for causing mismatch in a PV system is partial shading. This is where a shadow falls across part of the PV array creating a non-uniform changing irradiance pattern, illustrated by Figure 2.8 (a).

Figure 2.8: Effects of nearby tree on University of Leicester PV array

The speed at which the shading moves across the array will depend on what the cause of the shadow is. For instance if a bird flies over the array this will cause a shadow for less than a second, whereas the shadow created by a nearby static object will take minutes or even hours to move across the array.

The mismatch can also be caused by soiling of the PV array where the dust, dirt or debris that has accumulated on the PV module will partially prevent the light from reaching the PV cells as shown in Figure 2.8 (b). Partial shading is of interest to this study since domestic PV systems are more susceptible to partial shading due to a likelihood of nearby objects such as chimneys and trees.

2.3.2 Bypass Diodes

To demonstrate the creation of 'hot-spots' the reverse characteristic of a PV cell is shown in Figure 2.9 with plots at various irradiance levels. A hot-spot occurs when a series-connected string of PV cells containing an underperforming cell is operated at a current that is higher than the short-circuit current I_{sc} of that cell. The graph indicates that a small rise in current above I_{sc} causes a large increase in reverse voltage, and

therefore power dissipation, producing an excessive temperature in the cell. The generation of hot-spots is explained in greater detail in [22].

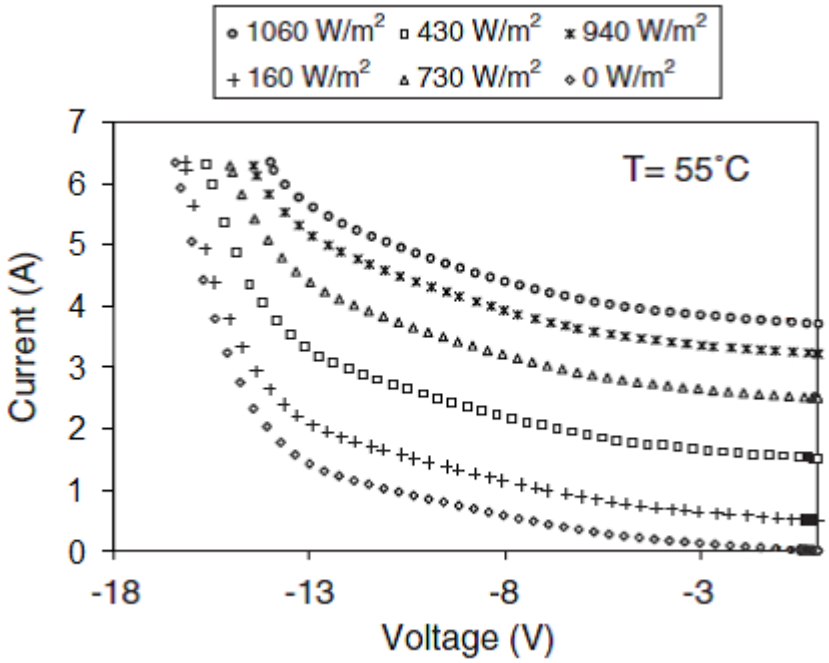


Figure 2.9: Measured reverse characteristic of a sample PV cell [23]

To prevent hot-spots occurring in underperforming PV cells the reverse voltage is usually limited through the use of bypass diodes. Passive bypass diodes are easy to implement since they can be encapsulated in the PV module during manufacturing.

However, passive diodes incur power losses with a current flowing through them due to the voltage drop across the junction. A study presented in [24] discusses how this power loss will get higher as the PV cells become larger and more efficient and the available current increases. The increase in power dissipation in the diode will cause a temperature that exceeds the IEC61215 standard.

The active bypass circuit developed in [24] uses a MOSFET to bypass the underperforming PV cells to produce a lower voltage drop than a conventional bypass diode. The lower voltage drop reduces the power losses associated with the bypass technique and prevents an excessive temperature.

It is also suggested in [24] that the ‘use of an active bypass element offers the opportunity to short circuit the PV module, e. g. during installation or in case of fire. The module will be activated by a remote signal, provided e. g. by the PV inverter’ but no further details are provided, such as experimental testing of this communication.

2.3.3 Improved MPPT Algorithms

A comparison of MPPT techniques taken from [5] was listed in Section 2.2. Ref. [5] includes a discussion on overcoming the problem of multiple local power maxima and at the time [5] was written, only the state-based method and current-sweep method were able to track the true MPP of a PV array.

The state-based method proposed in [25] combines a state-space model of the array and a dynamic non-linear feedback controller. However, the technique was only verified using a computer simulation of an array with 2 parallel connected strings, one shaded and the other not, to create the multiple local maxima in power. The PV array characteristic of series connected PV modules subjected to mismatch tends to be more complex due to the scope for greater variation in the current. Therefore the technique requires experimental testing on a partially shaded series string. Also the requirement of a state-space model specific to the PV array makes it impractical for use in commercial PCDs.

In the current-sweep method of [26] a periodic scan is carried out by varying the current from 0 to I_{sc} to find the I-V curve of the PV array. The V_{mpp} of the PV array is then computed from the I-V characteristic. Power is lost during the scanning period when the PV array will not be operating at the MPP. Also, a change in the PV array characteristic during the period between scans won’t be noticed until the next scan. The length of time between scans is therefore a trade-off between the ability to respond quickly to changes in the PV characteristic and the power lost from scanning.

According to [5] both the state-based method and the current-sweep method are of high complexity and depend on knowledge of the PV array to which they are applied. It is observed that hybrid methods have been developed such as in [27-30] where a standard MPPT algorithm, for instance incremental conductance, is employed with a secondary technique for scanning the PV array characteristic to ensure operation at the true MPP.

The investigation in [30] defines the conditions for initiating a scan of the PV characteristic due to suspected multiple local maxima. The losses incurred by scanning are therefore reduced since it is no longer necessary to carry out a periodical scan.

2.3.4 Distributed Maximum Power Point Tracking

Various PV system topologies are displayed in Figure 2.10. A traditional centralised maximum power point tracker (CMPPT) system consisting of a PV array of directly interconnected modules supplying a single inverter is shown in diagram (a). The CMPPT topology is susceptible to mismatch losses and the methods for minimising the mismatch losses described in the previous subsections are advised.

However, as Chapter 1 describes, distributed maximum power point tracking (DMPPT) systems are able to recover the majority of power lost through mismatch and are therefore preferable to CMPPT systems with intelligent MPPT algorithms for use in arrays that frequently encounter mismatched conditions.

To recover most of the power lost a DMPPT system uses per-module PCDs to convert the I_{mpp} of an underperforming section of a PV array so that it matches the current of the rest of the series-connected sections in the array. This subsection provides more detail on DMPPT systems with example topologies and types of PCD used.

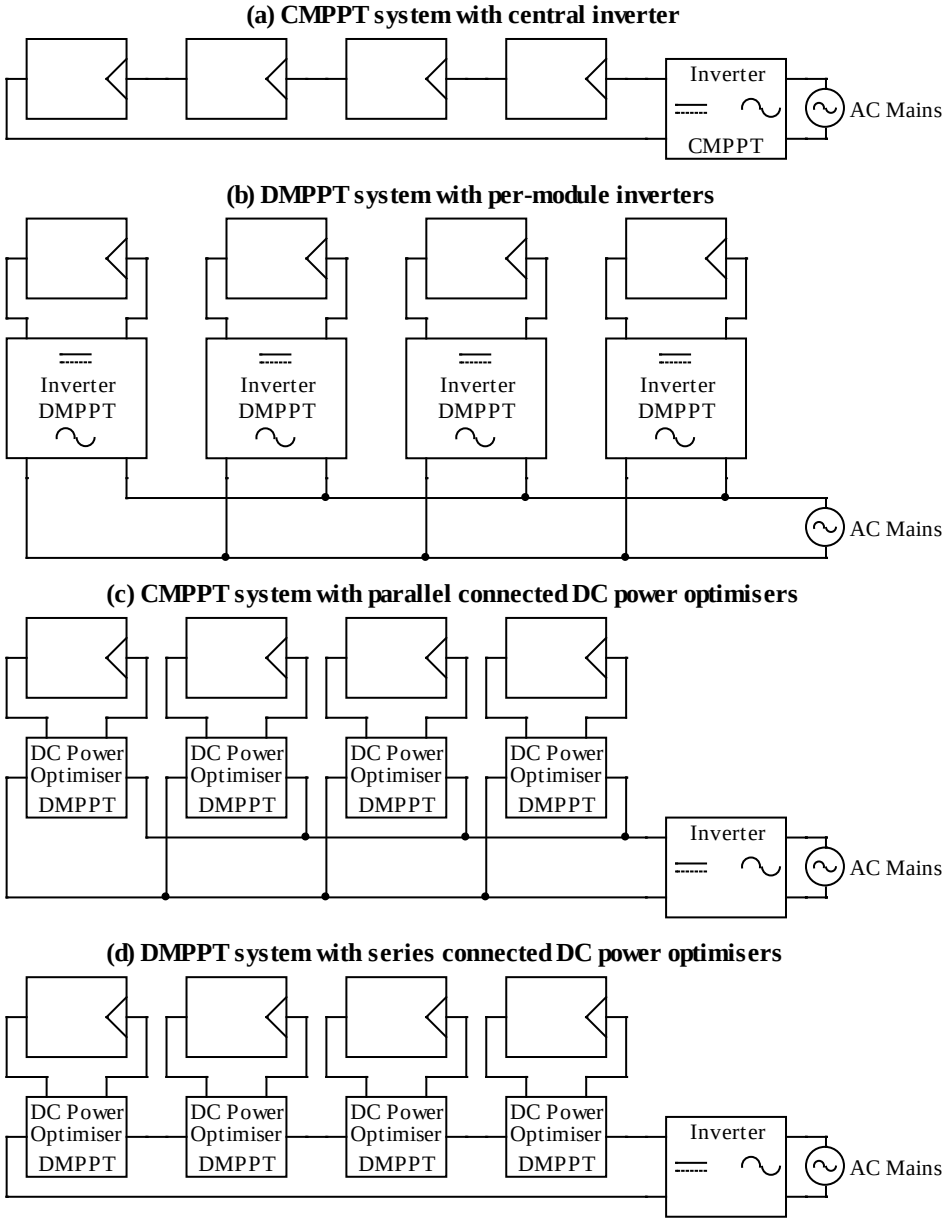


Figure 2.10: PV system topologies

The effect of a DC-DC converter PCD with MPPT on the PV module I-V curve is illustrated in Figure 2.11 [31]. This shows an area of constant power, bounded by limits to the current and voltage that arise from the effective conversion range of the PCDs power electronics. In [31] these limits are described by the minimum voltage conversion ratio K_{min} and the maximum voltage conversion ratio K_{max} multiplied by the V_{mpp} of the PV cells or modules on which the PCD is operating. Changing the PCD topology will

shift these limits but the overall shape of the characteristic will remain the same with the PCD able to maintain the MPP when the output remains within these limits.

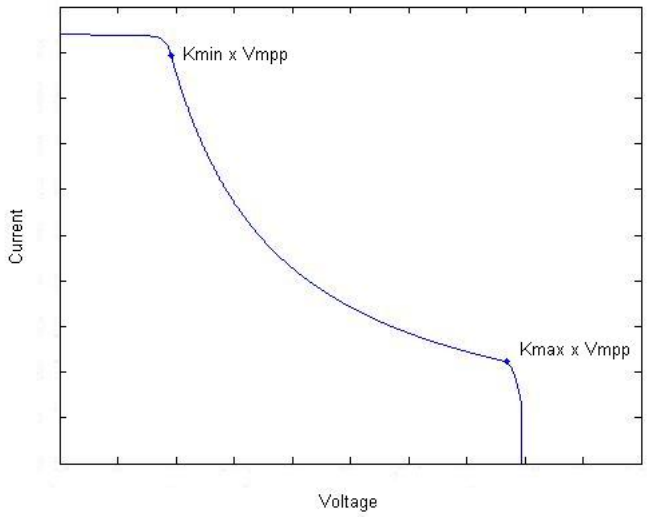


Figure 2.11: I-V curve taken after PCD with MPPT [31]

Ideally, DMPPT should be implemented on every cell in the PV array to ensure that each is operating at its individual MPP.

This approach has been applied to a solar powered vehicle in [32]. However, solar powered vehicles use high performance multi-junction PV cells since the space and weight is limited and therefore the cell voltage is high enough to allow for voltage losses in a converter. Also, the requirement of obtaining the maximum power possible with fast moving irregular shading caused by roadside objects, especially trees, justifies the extra complexity and cost of per-cell PCDs. At present the gain that would be achieved does not justify the extra cost and complexity of embedding per-cell PCDs in a commercial PV module for a domestic system.

The progression from using per-cell converters is to replace bypass diodes with MPPT controlled PCDs, a more appropriate solution than the active bypass diodes of [24]. MPP tracking would then be applied to each of these sub-strings in a PV module.

However, at the present time the additional cost and complexity of integrating such devices into PV modules outweighs the potential benefits.

It is possible for per-module converters to be housed in their own casing and wired externally to the PV module. Per-module DMPPT is therefore a practical solution in domestic PV systems, both technically and economically since they do not incur the expense of being embedded and connected internally within a PV module. There are various per-module DMPPT topologies as indicated in Figure 2.10.

In [33] an evaluation of PV module level DMPPT systems is given. DMPPT system disadvantages are increased installation costs and reduced efficiency under non-mismatch conditions since the PV module power now has to pass through the PCD circuit components as well as supply the DMPPT control circuits. The paper concludes that these systems only become viable for PV arrays where repeated partial shading from nearby objects mean mismatch losses will be a significant problem and the extra yield of a DMPPT system outweighs the disadvantages. They are most cost-effective for domestic PV systems where a fixture such as a chimney, flag-pole or nearby tree would frequently cast a shadow over the PV array, especially if the distributed PCDs can be applied to the affected PV modules only.

In [34-40] the concept of connecting an inverter directly to a PV module to create an ‘AC-module’, illustrated in Figure 2.10 (b), is proposed and investigated. The inverters are connected in parallel on the AC side and connected directly to the mains grid. This allows each PV module in an array to operate at its MPP, removing the effect of mismatch between modules.

However, as mentioned in [31], there are disadvantages to performing the DC-AC inversion at PV module level. These include the inefficiency of having to increase the voltage from a PV module to the level of the AC mains and significantly higher costs to

offer the same quality and safety as a central PV inverter. There are also the extra installation costs for wiring as each AC module is connected in parallel.

References [41-46] describe the development of DMPPT systems using per-module DC-DC converters (also called DC power optimisers or DCPOs) to perform MPP tracking at the module level. The main advantage of DCPOs over AC-modules is the straightforward series connection of the PCDs, Figure 2.10 (d), reducing the wiring costs and improving the efficiency.

However, [31] indicates that a DMPPT system using DCPOs is not always able to avoid mismatch losses. There are certain conditions where, due to the voltage conversion range of the DCPO's converter and the input voltage of the central inverter, some DCPOs cannot maintain the MPP of their PV module.

This is illustrated using plots to demonstrate the percentage of available power that the DMPPT system delivers. An example plot is given in Figure 2.12 where the ratio of unshaded to total PV modules (a) is plotted against the ratio of shaded to unshaded irradiance (α); the percentage of power extracted from the total available power (50-100%) is indicated as variations in colour. These plots assume a constant inverter input voltage and two distinct levels of irradiance.

The example plot indicates that for cases where the lower irradiance level is more than half the higher level ($\alpha > 0.5$) the DMPPT system can provide 100% of the available power since the required conversion ratio will always be within the DCPO limits. As expected, in the case of all modules being unshaded ($a = 1$) the system will again be able to provide 100% of the available power since there is no mismatch. There is also no mismatch if all of the modules are shaded. However, there is a level of irradiance below which the minimum inverter input can no longer be maintained which can be

seen in the plot for a = 0. There is a pattern to the variation of power output from the DMPPT system in the area between those already analysed.

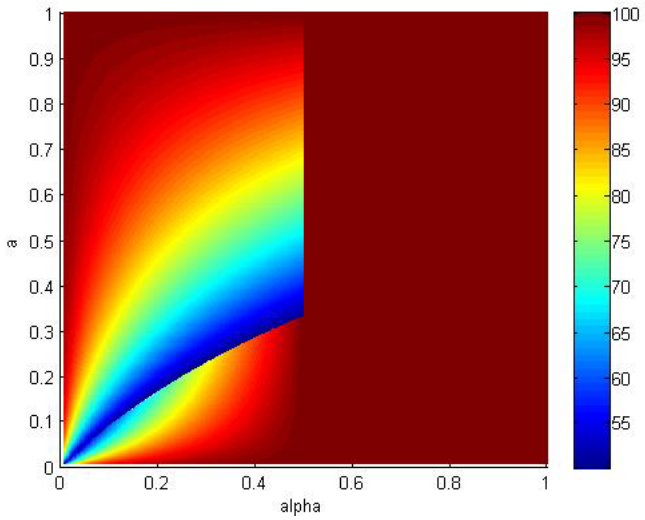


Figure 2.12: Indication of conversion limitation losses in DMPPT system with constant inverter voltage [31]

The plot of losses due to limitations in PCD conversion ratios in DMPPT systems are useful for visualising the amount of available power that can be delivered by such a system and demonstrate that it is not always possible to deliver 100%. However, they are restricted to two irradiance levels and a particular inverter voltage and so are not feasible for detailed analysis of DMPPT systems, especially where the inverter input is also MPPT controlled.

An overview of commercially available products for reducing mismatch losses, including DCPOs is given in [47]. Due to the higher cost, lower efficiency and poor reliability of the inverter contained within AC-modules, it is concluded that DCPOs are more viable for DMPPT systems. A list of available DCPOs given in [47] is provided below, and includes further details.

- **eIQ Energy vBoost 250/350** [48]
  - 250W and 350W units
  - Flyback topology with transformer allows paralleled output connections
  - Output voltage kept constant by the inverter
  - Communication via power line for data collection
- **National Semiconductor SolarMagic SM1230** (now Texas Instruments)* [49]
  - 230W unit
  - No communication
  - Buck/boost topology with series connected outputs
  - Inverter input can be constant voltage or MPPT controlled
  - Only required on PV modules suffering from poor performance [50]
- **National Semiconductor SolarMagic SM3320** (now Texas Instruments)* [51]
  - 320W unit
  - Chipset incorporated in PV module junction box
  - Tri-state topology: buck – panel mode – boost (based on buck/boost)
- **Tigo Energy Module Maximiser (MM)-ES/EP** [52]
  - ES: 300W series connected using buck topology
  - EP: 280W parallel connected using flyback topology with transformer
  - Wireless communication with central unit
  - Central unit controls DCPOs and collects data
- **SolarEdge PowerBox** [53]
  - 250W and 350W units
  - Series connected
  - Holistic approach requiring specialised inverter
  - PowerBox units keep string voltage constant
  - Power line communication
- **ST SPV1020** [54]
  - Monolithic boost converter IC with MPPT
  - Requires additional external components
  - Incorporated in PV module junction box
  - Can be used in place of bypass diodes located in junction box
  - Serial Peripheral Interface communication

** National Semiconductor has been taken over by Texas Instruments during this work. SM1230 unit is no longer manufactured –SM3320 chipset is still available.*

This list shows the various PCD topologies and DMPPT system configurations of the available DCPOs. The parallel connected DCPOs, the Tigo MM-EP and the eIQ vBoost, both encounter lower efficiency due to the internal transformer required to increase the PV module voltage, and increased wiring costs from the parallel connections. For the series connected DCPOs there is a mix of buck, boost, buck/boost and a tri-state method using a buck/boost circuit as reported in [55]

The tri-state method is explained using Figure 2.13. If the I_{mpp} of the PV module is lower than required the circuit behaves as a buck converter by keeping Q4 closed, Q3 open and using the buck leg (BK Leg) switches Q1-Q2 as a synchronous rectifier. If I_{mpp} is higher than required the circuit behaves as a boost converter by keeping Q1 closed, Q2 open and using the boost leg (BST Leg) switches Q3-Q4 as a synchronous rectifier. If I_{mpp} is at the correct level then 'panel mode' is engaged; switches Q5A/B close and all others remain open so that the PV module is directly connected to the output, removing the switching losses.

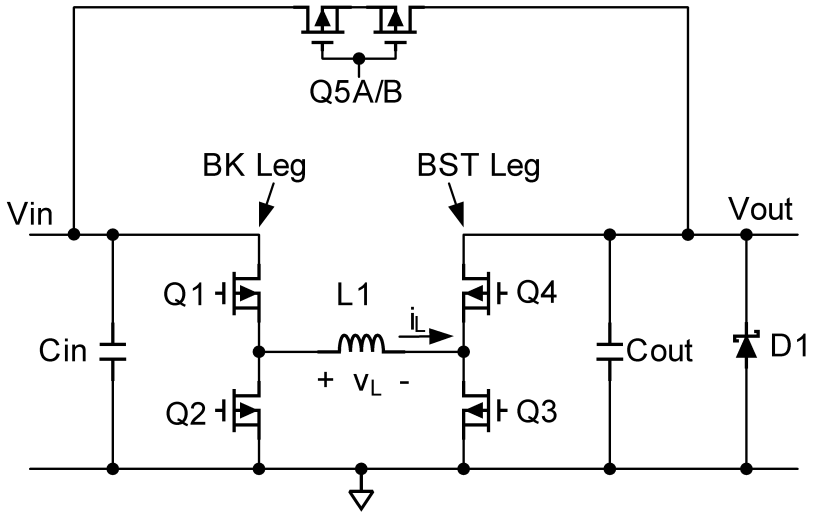


Figure 2.13: Tri-state buck/boost circuit of the SM3320 [55]

The PV system at the University of Leicester mentioned in Chapter 1 uses four SM1230 DCPOs to reduce the mismatch effects from partial shading of a nearby tree. The investigation into DMPPT systems presented in this work is therefore based on a system using SM1230 DCPOs.

2.4 Modelling of PV

A computer simulation model is required for prediction or analysis of a PV system. This section provides a summary of methods for modelling PV cells and modules, as well as a detailed description of the single-diode model with an explanation for the choice of the single-diode model for use in this study.

2.4.1 Overview of Modelling Techniques

There are numerous papers on the simulation of PV cells, modules and systems. The models have been developed for various reasons and are often tailored for their specific purpose. For example, in [56] a model is used to determine whether blocking diodes and bypass diodes are really needed, both [14] and [20] analyse the effects of shading on the PV array output characteristic whereas [57-59] describe a model that can be combined with the model of a PCD or for testing of an MPPT algorithm.

There are various methods for modelling PV cells and modules. The majority of the PV models presented in literature are based on versions of the single diode equivalent circuit of Section 2.1 which is widely accepted as an appropriate model for a PV cell. The equivalent circuit is displayed again in Figure 2.14 for reference.

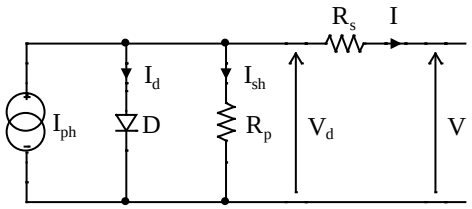


Figure 2.14: Equivalent circuit of a PV cell

The equivalent circuit is expanded in [57, 60] as illustrated in Figure 2.15 which includes a second diode junction to improve the model accuracy, especially at low irradiance levels. However, this increases the complexity of the model.

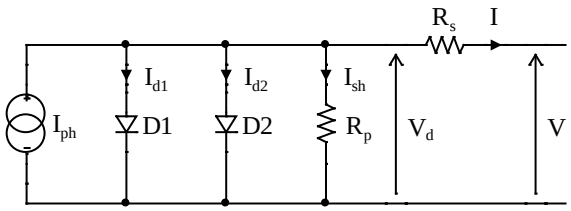


Figure 2.15: 2-diode model of a PV cell

It has been shown that there is a trade-off between accuracy and the complexity of a PV cell simulation model. The single-diode model including the resistances R_s and R_p is

used in this work because it provides sufficient accuracy whilst not requiring excessive processing power during simulation.

The single diode model has been adapted for various reasons. The performance of non-crystalline silicon PV cells modelled in [61-63] require modifications to the behaviour of certain circuit elements, such as the voltage dependency of I_{ph} in amorphous silicon described in [61]. In [64, 65] the complexity of the model is reduced by the removal of the parallel resistance R_p at the cost of accuracy.

2.4.2 Scaling of Model Parameters

The single-diode equivalent circuit presented in the previous subsection describes the behaviour of a PV cell. For simulating PV systems it is often desirable to simulate one or more PV modules. It would not be practical to set the parameters for each individual PV cell in this case as there would be hundreds or possibly thousands of cells. A technique for scaling the 5 PV cell parameters is required where the parameters are I_{ph}, I_o, γ, R_s and R_p.

The technique used in this study is based on the assumption that all of the PV cells within a module are identical and experience the same irradiance and temperature conditions. The procedure is used extensively in literature and is best described in [57]. The diagrams in Figures 2.16 and 2.17 show the case for two series connected cells and two parallel connected cells respectively.

The currents I_{ph}, I_d, I_p and I are the same for the individual cell circuits of (a) and scaled equivalent circuit of (b). Therefore, to maintain the output voltage V the voltages V_d and IR_s of the scaled circuit must be twice the value of the cell circuits as indicated in Figure 2.16. Since I and I_d are the same, the resistances R_s and R_p of the scaled circuit have to be twice the size.

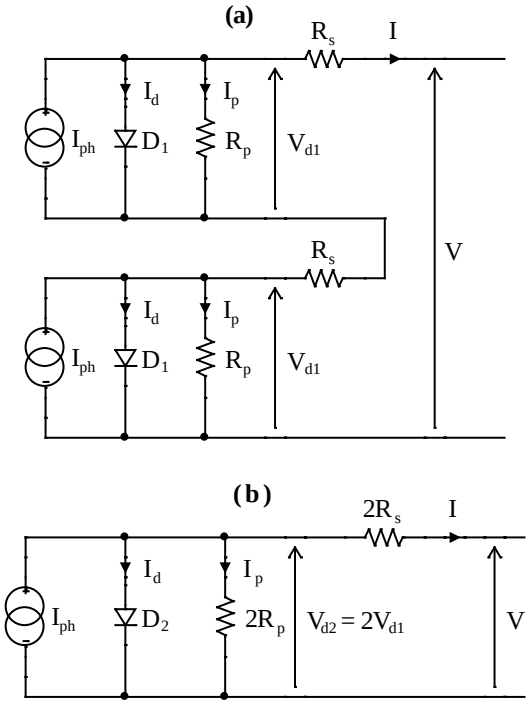


Figure 2.16: Single-diode representation of (a) 2 series connected cells and (b) the scaled equivalent circuit

Due to the non-linear nature of the diode, the manner of scaling the D_2 parameters to maintain I_d is not as clear. To show how the diode parameters are scaled the Shockley diode equation introduced in Section 2.1 is applied to both cases and equated to give equation (2.8).

$$I_o\left(e^{\left(\frac{qV_{d1}}{\gamma kT}\right)} - 1\right) = I_o\left(e^{\left(\frac{qV_{d2}}{2\gamma kT}\right)} - 1\right) \qquad \textbf{(2.8)}$$

To preserve I_d the exponential terms in (2.8) must be the same so a factor of 2 is brought into the denominator for the scaled equivalent circuit to reduce V_{d2} to V_{d1}. The scaling is therefore applied as a multiplication of the diode ideality factor γ.

In the parallel connection of Figure 2.17 voltages V and V_d are the same for the individual cell circuits of (a) and the scaled equivalent circuit of (b). Therefore, to maintain I in the scaled circuit the currents I_{ph}, I_d and I_p must be twice as large as the respective currents in the cell circuits.

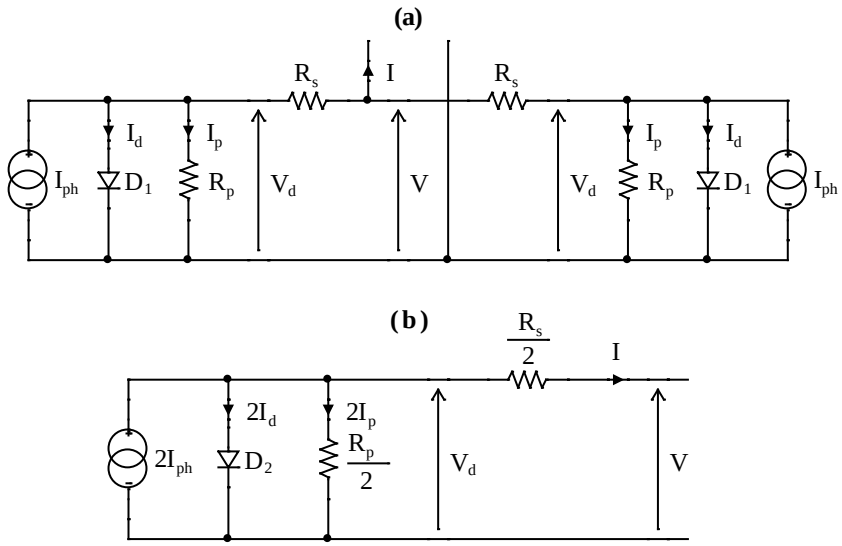


Figure 2.17: Single-diode representation of (a) 2 parallel connected cells and (b) the scaled equivalent circuit

Since V and V_d are the same size, resistances R_s and R_p are half the size in the scaled circuit. The scaling of the diode parameters is less complicated for the parallel case since the exponential term of the Shockley equation is the same for both cell and scaled circuits. To obtain $2I_d$ for the scaled circuit will therefore involve multiplying the I_o parameter by 2.

The series and parallel scaled equivalent circuits for 2 PV cells can be generalised for N_s series connections and N_p parallel connections by substituting the factor of 2 with N_s and N_p. These are superimposed to obtain the overall relationships for scaling the parameters as described by equations (2.9) to (2.13).

$$I_{ph}|_{module} = N_p I_{ph}|_{cell} \quad \textbf{(2.9)}$$

$$R_s|_{module} = \frac{N_s}{N_p} R_s|_{cell} \quad \textbf{(2.10)}$$

$$R_p|_{module} = \frac{N_s}{N_p} R_p|_{cell} \quad \textbf{(2.11)}$$

$$I_o|_{module} = N_p I_o|_{cell} \quad \textbf{(2.12)}$$

$$\gamma|_{module} = N_s \gamma|_{cell} \quad \textbf{(2.13)}$$

The scaling of the single-diode model parameters from PV cell level to PV module level was demonstrated for identical PV cells. This technique can also be applied to a PV array consisting of parallel-connected strings of series-connected PV modules to obtain a single equivalent circuit. This is useful when testing PV inverter MPPT algorithms.

2.4.3 Extraction of Model Parameters

The model described in this section requires 5 parameters to control the shape of the simulated I-V curve. In some cases, such as to allow the model to be fitted to experimental data, a means of extracting these parameters is required. The technique used in this study, derived from [66], is reported in Appendix A.

The developed approach involves the iterative 'generalised Newton's Method' described in [67] and uses the current and voltage values at the main operating points of the PV characteristic illustrated in Chapter 1. The values used in this process can be taken from the manufacturer's datasheet or from experimental data. The iterative algorithm has been found to consistently converge from the starting point outlined in Appendix A and is therefore suitable for use in this research.

2.4.4 Dependence of Model Parameters on Environmental Conditions

Variations in the environmental conditions of temperature T and irradiance G affect the 5 parameters of the single-diode PV model. For an accurate model that allows prediction of the PV module behaviour for changes in these conditions the environmental effects on the parameters must be accounted for.

The manufacturers' datasheets for PV modules usually provide data for a short circuit current temperature coefficient K_{Ti} and an open circuit voltage temperature coefficient

K_{Tv}. These can be used in equations (2.14) and (2.15) to obtain values for I_{sc} and V_{oc} at various temperatures where the subscript numbers denote the paired temperature and value.

$$I_{sc2} = I_{sc1}\left(1 + K_{Ti}(T_2 - T_1)\right) \quad \textbf{(2.14)}$$

$$V_{oc2} = V_{oc1} + K_{Tv}(T_2 - T_1) \quad \textbf{(2.15)}$$

It is common in literature to assume that I_{ph} and I_{sc} are equal since at short circuit conditions the currents I_d and I_p can be neglected due to the greatly reduced voltage across the diode junction and R_p. I_{ph} is also widely considered to vary linearly with the incident irradiance. This gives rise to the relation (2.16) for I_{ph} that takes into account the change in T and irradiance G:

$$I_{ph2} = I_{ph1}\frac{G_2}{G_1}\left(1 + K_{Ti}(T_2 - T_1)\right) \quad \textbf{(2.16)}$$

Equation (2.17), presented in [68-70], provides the temperature dependence of I_o, with γ assumed to be independent of G and T. The references also state that the effect of G on I_o is negligible. According to [68] the bandgap energy E_g of silicon has a temperature coefficient of approximately 0.027%/ °C. Over the operating temperature range of a PV module this would give rise to a negligible difference in E_g. Therefore E_g is assumed to be constant at 1.12eV, the value for silicon at 25°C.

$$I_{o2} = I_{o1}\left(\frac{T_1}{T_2}\right)^3 e^{\left(\frac{qE_g}{\gamma k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right)} \quad \textbf{(2.17)}$$

Reference [68] also indicates that since R_p is inversely proportional to I_{sc} it is also inversely proportional to G, giving rise to equation (2.18).

$$R_{p2} = R_{p1}\frac{G_1}{G_2} \quad \textbf{(2.18)}$$

To test the temperature dependence of the model parameters outlined in this section, the BP7175S PV module I-V curve was simulated using the temperature coefficients

provided by the manufacturer. The results were plotted in Figure 2.18 along with the curves given on the manufacturer's datasheet for temperatures ranging from 0°C to 75°C. The modelled I-V curve at 25°C is closely matched to the manufacturer's characteristic. The modelled variations in temperature show that the curves progress in the right direction but have a discrepancy at V_{oc}, and less so at I_{sc}.

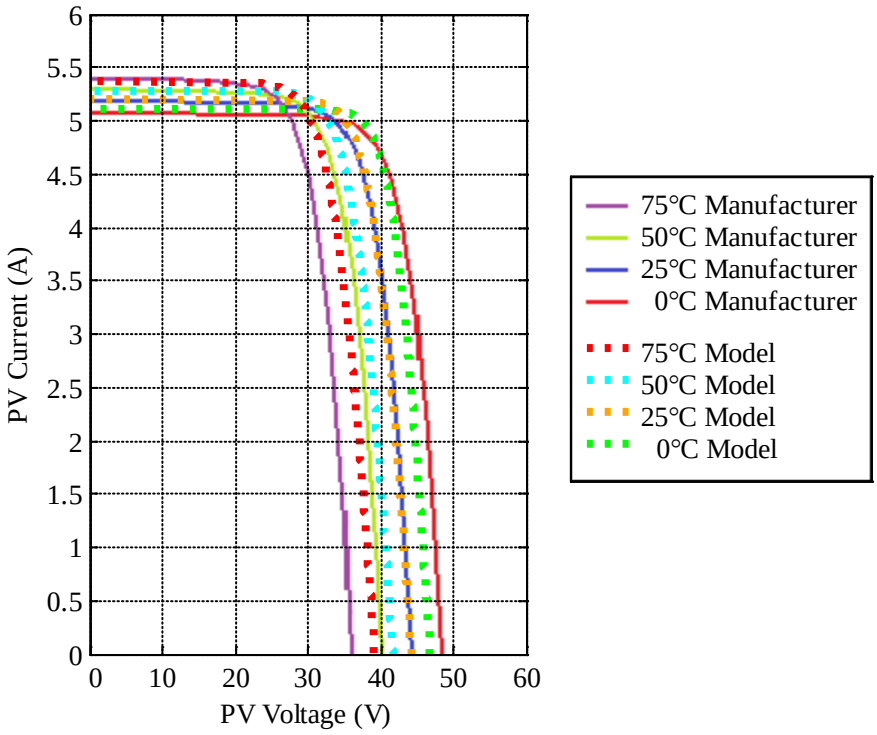


Figure 2.18: BP7175S datasheet and model I-V curves at various temperatures

2.5 Interactions in DMPPT Systems

This chapter has so far discussed in detail the operating principles and modelling techniques for PV cells, modules and systems. This section goes on to present the current state of research on the topic of interactions in DMPPT systems as described in the literature. A discussion is then presented on the methods of studying the possible interactions.

2.5.1 Overview of Reported Studies

In section 2.3.4 the performance of a DMPPT system based on DCPOs as described in [46] is discussed. The system is based on per-module DCPOs connected in a series string to an inverter with a constant input voltage. The paper suggests that there are no negative interactions between the MPPT controllers of the DCPOs and that any perturbation of the inverter current will not have an undesired effect on the stability of the system. However, no evidence has been given that this remains true for a range of possible scenarios.

In [71] a model of a PV system is presented which is expanded in [72] and adapted in [73] for analysis of DMPPT systems. [73] states that 'It is worth noting that an accurate DC and AC analysis capable of describing steady-state operation, dynamic behaviour and stability of a whole array of separately controlled PV modules (SCPVMs) has not been presented so far in literature'. The analysis presented in the paper is based on a single PV system configuration using mathematically based small-signal models of the components to determine the stability.

The system configuration consists of 13 PV modules with individual DCPOs that are connected in series, feeding a single phase inverter with a constant regulated input voltage. The inverter dynamics and control are assumed to have a negligible effect on the stability of the DMPPT system and so the inverter has been modelled as an ideal DC voltage source and a series resistance that provides slight voltage variations for changes in current. The 13 PV modules are split into two groups, H and L, with a particular irradiance level associated with each group.

Diagrams of the possible operating areas of DCPOs, similar to the plots of [31] displayed in Figure 2.12, are defined as 'feasibility maps'. The feasibility maps show the plane of group H module voltage against group L module voltage for a particular

irradiance pattern with the fraction of total possible output power obtainable shown as a variation in colour. A three dimensional feasibility map could be used to allow for variation in inverter input voltage or for a third level of irradiance.

In the review presented in [74] it is stated that DMPPT 'allows for reducing the impact of the mismatching effect, but its implementation requires further studies in terms of interactions among different systems, employing the MPPT function at the same time', while [75] concludes that any interaction of DMPPT converters during transient events, faults and start-up should be investigated.

The literature shows that there is a lack of investigation into the stability of DMPPT systems and the possibility for negative interactions. Only [71-73] have carried out research on the transient stability of such a system. However, the study was limited to a single system configuration and was performed using a small signal model in the frequency domain. It is challenging to expand a model such as this to use for a large range of DMPPT system configurations. It is the aim of the present research to provide a means for comprehensive analysis of DMPPT systems.

2.5.2 Techniques for Investigating DMPPT Interaction

There are various techniques for investigating distributed maximum power point tracking (DMPPT) systems. Three techniques considered in this study are: practical indoor testing, practical outdoor testing and computer based modelling.

For practical indoor testing of DMPPT systems a test setup involving solar emulators (controllable sources of light) and real PV modules is not feasible due to space and power requirements. An alternative method is to use module level PV emulators (controllable sources of electrical power) supplying per-module power optimisers that perform the DMPPT and feed a PV inverter. This method offers some flexibility in terms of varying the I-V characteristics of the PV emulators but is limited by the PCDs

that are available. This would become expensive if a range of power optimisers and inverters were to be tested.

Since all of the system components used for practical outdoor testing are genuine devices this method would offer the most realistic test conditions. However, the flexibility is limited by the available system components in the same manner as the practical indoor testing. Also, the variability of the outdoor environmental conditions makes it challenging to analyse the results and conduct controlled testing.

To provide exceptional flexibility and controllable testing a computer model can be used to simulate DMPPT systems since a variety of PCDs can be tested and the PV array conditions set by the user. However, a model needs to be verified using experimental data.

A combination of the three methods is used in this study: experimental data is obtained on the operation of the PCDs through the use of a PV emulator, and on the operation of an outdoor PV system. This data is used to validate the co-simulation of the PV system in OrCAD PSpice and Simulink which can then be modified to further investigate interactions in DMPPT systems.

Chapter 3 PV Emulator

In this thesis the following terms will be used to distinguish between hardware based physical replication and computer based software representation of PV:

PV Emulator Power electronic hardware that can physically reproduce the output of a PV cell, a module, or an array from user controlled input variables, including the irradiance level.

PV Simulator Software based computer representation of a PV cell, a module, or an array that has no physical output.

This chapter describes typical PV emulation methods and gives examples of PV emulators (PVEs), both commercially available and presented in the academic literature.

3.1 Purpose of a PVE

Controlled repeatable testing of PV system power conditioning devices (PCDs) is difficult to achieve through the use of real PV modules. Testing using a real outside array involves complicated methods to compensate for variations in the conditions, such as the irradiance and temperature.

Indoor testing using a real PV array with controllable lighting conditions is impractical for an array of appreciable output power due to the physical size of the array. This requires a large amount of space, as well as power for lighting and cooling of the system.

To perform repeatable controlled tests on PV system PCDs a PVE is normally used. PVEs consist of a controllable DC power supply (CDCPS) and a computational control method to keep the output values on the desired PV characteristic curve. A high level block diagram of a typical PVE system is given in Figure 3.1.

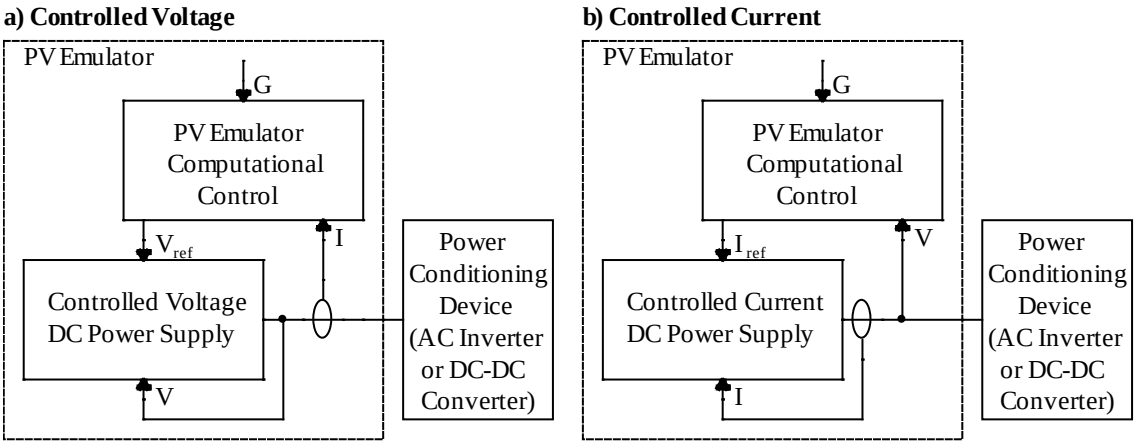


Figure 3.1: High level PVE system block diagram

The non-linearity of a PV characteristic creates a problem in a PVE system. Figure 3.2 shows that between I_{sc} and the top of the knee the rate of change of V with respect to I is high, whereas between the bottom of the knee and V_{oc} the rate of change is low. This introduces a variable gain to the feedback loop of the system.

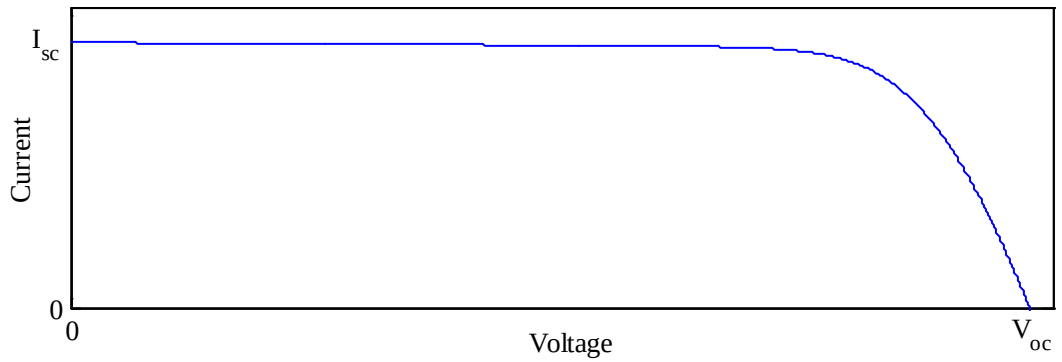


Figure 3.2: I-V characteristic of a PV module

The block diagrams in Figure 3.1 indicate that the CDCPS is either voltage or current controlled. The chosen variable depends on a number of factors including the design of the power supply and the requirements of the PVE. Voltage control is usually chosen since most PCDs either operate around the maximum power point (MPP) whilst running or at open circuit whilst idle.

Examples of the various computational methods of PVE control are: analogue scaling, analogue computation, real-time digital computation, and digital lookup computation. Each method is described in the following subsections.

3.1.1 Analogue Scaling

The typical system diagram for an analogue scaling method is given in Figure 3.3. The method involves the use of a sample PV cell, or photodiode, to generate the required characteristic. The irradiance level G is set using the controllable light source under which the sample PV cell is placed. The load value is measured and fed back via a variable DC source to the PV cell. The resulting output of the PV cell is amplified to the required reference level for the CDCPS of the PVE.

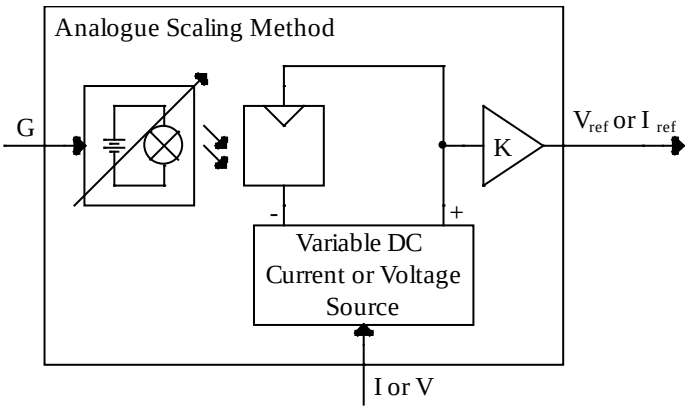


Figure 3.3: Diagram of analogue scaling method of PVE control

3.1.2 Analogue Computation

A typical system diagram of an analogue computation method is given in Figure 3.4. This method uses an analogue computation circuit that replicates the 1 or 2 diode model of a PV cell, seen in chapter 2, using physical diodes and resistors. G is usually set using a current, or voltage, representation of I_{ph}. The load value is measured and fed back to the computation circuit. The resulting output is amplified to the required reference level for the CDCPS of the PVE.

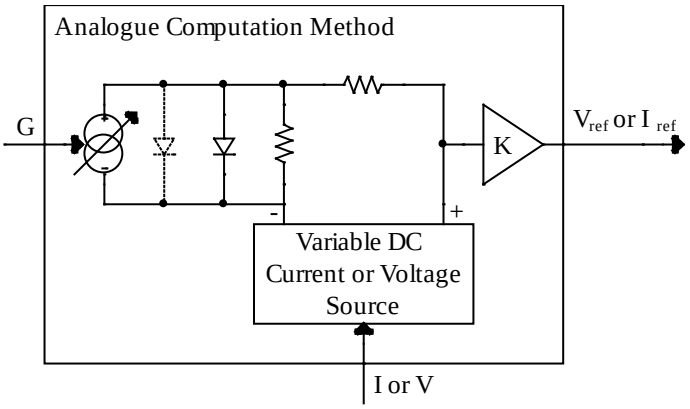


Figure 3.4: Diagram of analogue computation method of PVE control

3.1.3 Real-Time Digital Computation

The system diagram for a real-time digital computation method is given in Figure 3.5. This method uses a digital computer to apply the equations of the 1 or 2 diode model in real-time. The digital computer can be anything that can perform the required calculations fast enough to run in real time, including microprocessors and digital signal processors.

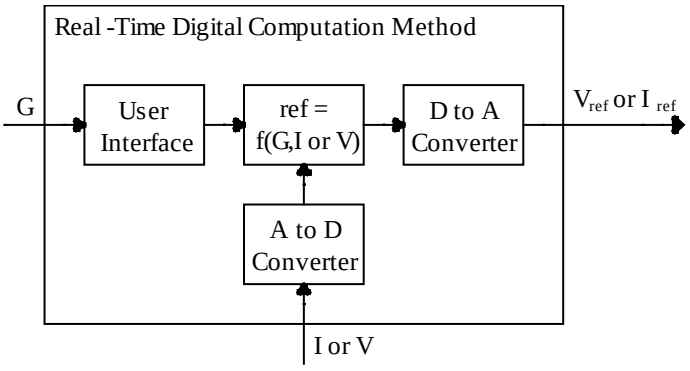


Figure 3.5: Diagram of real-time digital computation method of PVE control

G is set through a graphical user interface (GUI) on a PC, or a hardware user interface (HUI) using control knobs or buttons. The load value is measured and passed to the digital computer via an A to D converter. The digital computer applies the appropriate equations and passes the solution to a D to A converter. The resulting analogue signal is used as a reference for the CDCPS.

3.1.4 Digital Lookup Computation

The system diagram for a digital lookup computation method is given in Figure 3.6. This method uses a digital computer to pre-solve the equations of the 1 or 2 diode models across the operating range of the PV module or array that is being emulated. The irradiance level is set in the same ways as the real-time digital computation method. The resulting voltage and current values are stored in a lookup table.

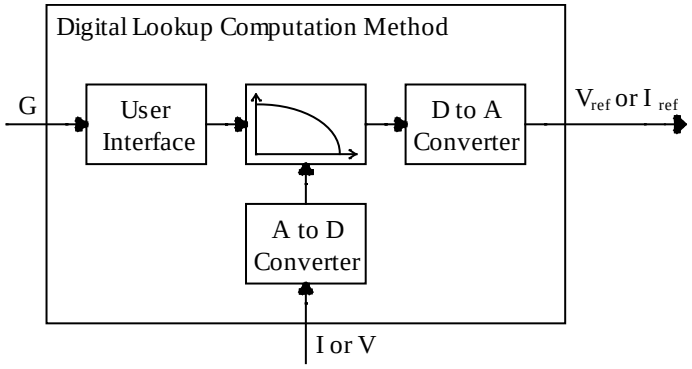


Figure 3.6: Diagram of digital lookup computation method of PVE control

The load value is measured and passed to the digital computer via an A to D converter. The digitised value is used as the input to the lookup table. The output of the lookup table is converted into an analogue signal which is used as the reference for the CDCPS.

3.1.5 Comparison of Methods

The main advantage of the analogue scaling method is the use of a sample PV cell to easily reproduce an accurate PV characteristic. However the flexibility of the system is limited as a sample cell would be required for each different PV module type. For emulation of partial shading conditions a number of sample cells and controllable light sources are needed, increasing both the cost and physical size of the system.

The analogue computation method does not need a controllable light source, only a basic analogue circuit, making it cheaper and easier to construct than the analogue scaling method. To emulate different PV modules the analogue circuit is ‘tuned’ to the

required characteristic using variable components making it more flexible. To emulate partial shading conditions the complexity and size of the computation circuit increases as a diode model representation would be required for each partition of the array.

The pre-calculation of the PV characteristics using the digital lookup method means that less processing speed and power are needed than with the real-time digital computation method, especially for emulating complex partial shading conditions. However the storage of lookup tables for the digital lookup method requires more memory than the real-time digital computation method, especially to implement a change in the PV system input parameters during the running of the emulator which needs at least 2 lookup tables.

The analogue computation methods can be constructed easily using basic analogue circuits and do not suffer from quantisation and discretisation errors associated with the digital methods. However digital methods are more flexible in terms of modelling different PV modules as the required characteristics can be stored in a digital database allowing the user to select a PV module.

The choice of PVE computation method depends on the required application. If needed to test the same PCD over a wide range of parameters, including PV module type, then the flexibility of a digital method would be preferable; for testing a variety of PCDs with the same characteristic, the reduced complexity of the analogue computation method is desirable.

3.2 Review of PVEs

This section provides an overview of the present state of PV emulators (PVEs). An analysis of some of the commercially available PVEs is provided along with a review of PVEs presented in literature.

3.2.1 Commercially Available PVEs

Agilent Technologies offer a number of off-the-shelf PVEs in their DC power supply range. The specifications are given in Table 3.1 with the cost at the time of writing. The E4350B and E4351B models [76] are to be discontinued in 2013 and are standalone units. The E4360 series [77] are modular power units that need to be assembled with a 'mainframe', the E4360A. The mainframe contains all of the PVE computational control and accepts up to 2 of the power supply units, the E4361A or 4362A.

PV Emulator Model	Rated Power (W)	Rated Voltage (V)	Rated Current (A)	Voltage Rise Time[1]	Voltage Settling Time[2]	Maximum Capacitive Load (μF)	Price
E4350B	480	60	8	not given	not given	2000	£6735
E4351B	480	120	4	not given	not given	2000	£6735
E4361A	510	65	8.5	< 8ms	28ms	2000	£5983[3]
E4362A	600	130	5	< 8ms	28ms	2000	£5983[3]

[1] Rise time is defined as the time taken for the output to change from 10% to 90% or 90% to 10% of the total change in voltage.
[2] Settling time is defined as the time taken for the output to settle within 0.1% of the total change in voltage.
[3] Price includes the cost of the required mainframe – each module has a cost of £3378

Table 3.1: Specifications of PVEs from Agilent Technologies

Magna-Power Electronics offer a software package, Photovoltaic Power Profile Emulation (PPPE) [78], which is used on a PC connected to one of their programmable DC power supplies to create a PVE. The use of a non-specialised DC power supply from the XR, TS, MS or MT series [79-82] means there are extensive power, current and voltage ranges available. The general specifications of each range are given in Table 3.2.

Power Supply Range	Available Powers (kW)	Load Transient Response[1]	Maximum Slew Rate[2]
XR	2, 4, 6, 8	2ms	100ms
TS	5, 10, 15, 20, 25, 30, 45	2ms	100ms
MS	30, 45, 60, 75	2ms	100ms
MT	100, 150, 250, 500, 750, 1000	2ms	100ms

[1] Recovery to within ±1% of regulated output for step change in load of 50% - 100% or 100% - 50%.
[2] For output change from 0 to 63%. High slew rate option available for all models; 4ms for 0 to 63% voltage change and 8ms for 0 to 63% current change.

Table 3.2: Specifications of programmable DC supplies from Magna-Power Electronics

The Agilent and Magna-Power Electronics PVEs all use the digital lookup computation method. However the Agilent PVEs are standalone units with a button based HUI, whereas the Magna-Power Electronics system uses a software based GUI that requires the use of a PC. The ways of generating the PV characteristics for the lookup tables are as follows.

The Agilent emulators have a default operating mode where a square PV characteristic is generated with a constant voltage or current either side of the MPP. Both the Agilent PVEs and PPPE software have a curve generating mode that allows the user to enter the lookup table data directly and a mode that generates a lookup table from the user input of the parameters V_{oc}, I_{sc}, V_{mpp}, and I_{mpp}. The PPPE software also allows the user to choose the PV module technology and enter reference parameters of irradiance, temperature, voltages and currents. Lookup tables are then generated from these reference values at new irradiance and temperature values entered by the user.

3.2.2 Overview of PVEs Presented in Literature

Academic papers on PVEs have been produced for over 30 years. The earlier papers generally describe PVEs with analogue computation methods such as in [83] and [84]. Due to the lack of high-speed, low-cost computers for use in a PVE system at the time that these papers were written, the use of an analogue method is necessary for producing a PVE with a fast response.

In [84] the analogue computation method is combined with a digital computation method with the option for the user to select between them. The paper states that the analogue method is more suited to testing the PCD response to transient events whereas the digital section is appropriate for long-term investigations.

Due to improvements in the speed of digital processors and controllers there have been numerous papers on PVEs using some form of digital computation control. For instance in [85] a PVE is developed that combines an off-the-shelf programmable DC power supply with a PC running a Labview based programme that provides digital lookup computation control of the emulator. However, the emulator is only tested with a static load with no mention of the dynamic performance of the PVE.

In [86] real-time digital computation control is implemented through a dsPIC digital signal controller. The power supply developed is specifically for the PVE and is based on the flyback topology with a high frequency transformer. An analytical model of the converter is used to derive a controller that provides a fast response, although the paper neither defines the speed of response that would be considered fast nor provides any data on the actual speed of the PVE response, again just providing test results with a static load.

3.3 Summary of Present State of PVEs

This chapter has defined the terms simulator and emulator in this work with the former providing a computer based replication of a PV system and the latter generating a physical reproduction of the PV electrical characteristic. A description of the purpose of a PV emulator (PVE) is given and the construction of a PVE as a combination of controllable DC power supply (CDCPS) with a means of control is demonstrated.

An overview of PV emulator (PVE) control techniques is provided with a comparison between them given. The advantages of the methods are outlined with a suggestion for the application that would be best suited for each. The techniques considered were: analogue scaling, analogue computation, real-time digital computation and digital lookup computation.

Two commercial PVEs have been studied in detail and although they have a respectable speed of response, the cost of the units makes them unattractive for academic research facilities.

Chapter 4 Development of PV Emulator Computation Control

A PV module emulator (PVME) is required for the testing of power conditioning devices (PCDs) described in Chapter 6. Chapter 3 has provided an overview of PV emulators (PVEs) and explains how they reproduce the electrical output of a desired PV characteristic curve through a combination of computational control and a controllable DC power supply (CDCPS). The development of computational control methods for use in the PVME and a conceptual PV array emulator (PVAE) are detailed in this chapter.

4.1 Analogue Computation Method

The PVME is required to test a power optimiser. The PVME must be able to reproduce the electrical output of a single PV module for a time-varying irradiance pattern to test the dynamic performance of the power optimiser. It should also allow emulation of a range of maximum power point (MPP) voltages V_{mpp} to determine whether the power optimiser maximum power point tracker (MPPT) algorithm accounts for variations in V_{mpp}.

From the above statements and from the reasoning given in the comparison of computational methods in Chapter 3 an analogue computation method was selected for the PVME. The development of an analogue computation circuit (ACC) for use with a CDCPS is described in this section.

4.1.1 Development of the ACC

The single diode model of a PV cell was introduced in Chapter 2 and is shown again in Figure 4.1 for reference. It can be seen that the photocurrent I_{ph} splits into the diode current I_d, the current through the parallel resistance I_p and the output current I. For a particular I_{ph} the diode voltage V_d and the output voltage V will depend on I.

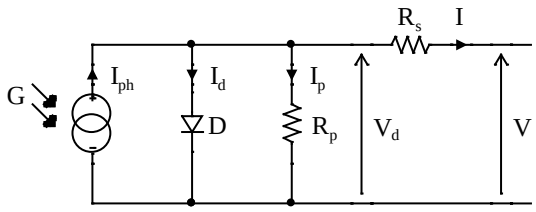


Figure 4.1: Single diode model of a PV cell

The purpose of the developed ACC is to reproduce the characteristics of the single diode model in Figure 4.1 by setting the reference for the output voltage (V_{ref}) of a CDCPS. The functional diagram of Figure 4.2 represents the computational stages required to achieve this.

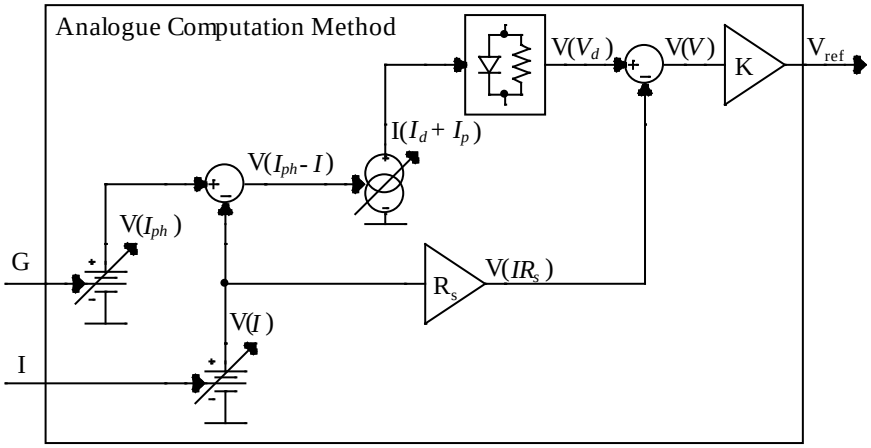


Figure 4.2: Functional diagram of the ACC

The user sets the irradiance level G as a voltage V(I_{ph}) that is proportional to I_{ph}. I is measured as a proportional voltage V(I) which is subtracted from V(I_{ph}). It can be seen in Figure 4.1 that the difference between I_{ph} and I is the sum of I_d and I_p. Therefore V(I_{ph}–I) is converted into a proportional current I(I_d+I_p). This current is passed through a parallel network of a diode and resistor to obtain V(V_d).

V(I) is multiplied by the series resistance R_s to represent the voltage drop across R_s. V(IR_s) is then subtracted from V(V_d) to give the voltage V(V) which is scaled by the factor K to the required V_{ref} of the CDCPS.

The ACC represented by Figure 4.2 has been constructed using op-amp circuits as depicted in Figure 4.3. The circuit includes variable resistors for tuning the ACC to a particular PV module.

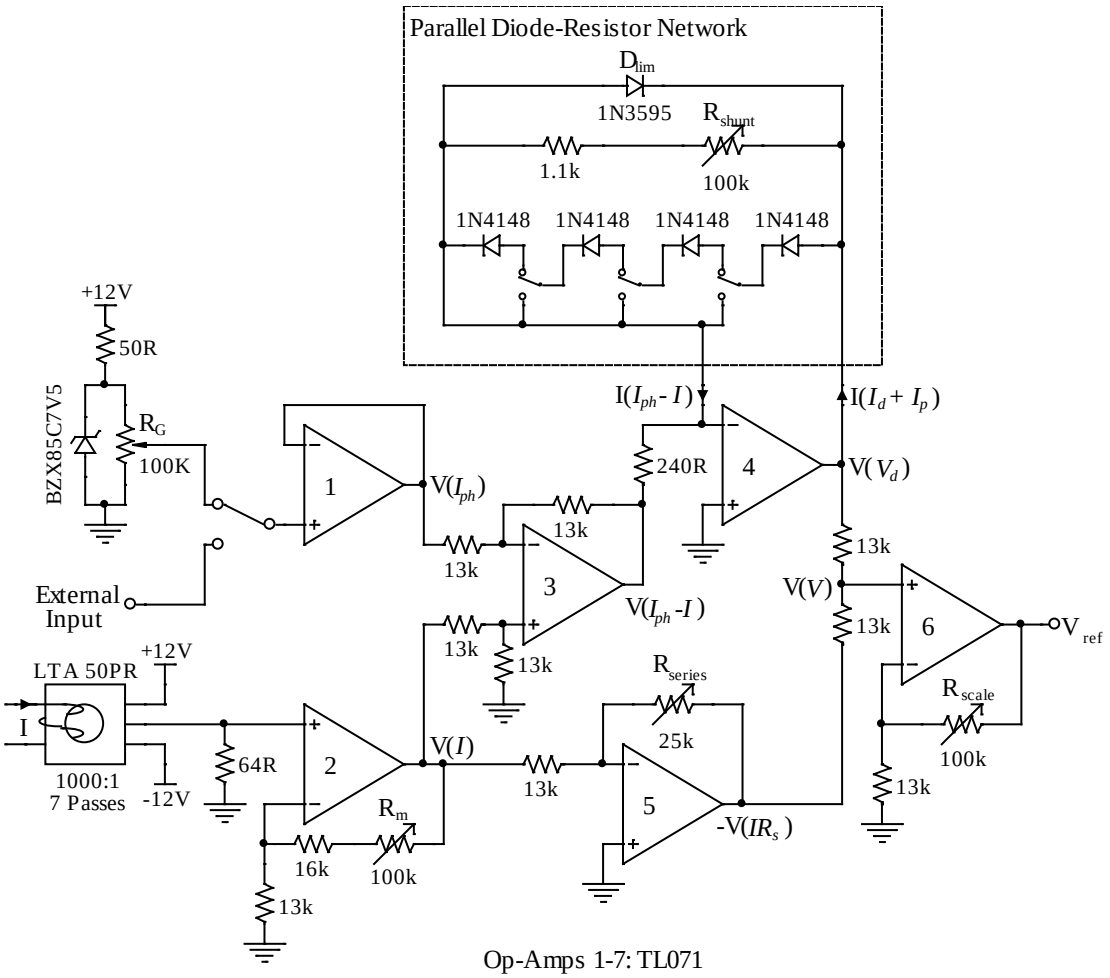


Figure 4.3: Circuit diagram of the ACC

In the ACC op-amp 1 provides V(I_{ph}) from the user input which can be switched between the potentiometer R_G or an external input. The external input allows emulation of a time varying irradiance.

A Hall-effect transducer is used to measure I. The gain of the measurement circuit of op-amp 2 determines the proportionality of V(I) and V(I_{ph}), and is set using the variable resistor R_m. The VA^{-1} ratio is set so that the required I_{sc} of the PVE results in a voltage

close to the maximum possible V(I_{ph}) of the user input circuit to reduce sensitivity to noise.

Op-amp circuit 3 generates the difference V(I_{ph}-I) as a negative voltage. The negative voltage drop across the input resistor of op-amp 4 draws I(I_{ph}-I), or I(I_d+I_p), through the feedback path of op-amp 4 containing the parallel diode-resistor network giving a positive output voltage of V(V_d). Since the CDCPS is voltage controlled and has no control over I, the diode D_{lim} prevents the output of op-amp 4 from going into negative saturation in the case where $I > I_{ph}$.

If a single diode in the parallel diode-resistor network is considered to represent a single PV module then a series connection of diodes indicates a string of identical PV modules. The developed ACC contains 4 such diodes with the ability to switch the desired number into the parallel diode-resistor network to emulate a PV string of between 1 and 4 modules. The value of the parallel resistance can be adjusted using the variable resistor R_{shunt} and is limited to a minimum value of 1.1kΩ.

The gain of op-amp circuit 5 is equivalent to multiplication of I by R_s and is set by the variable resistor R_{series}. Since the value of R_s is usually less than 1Ω an inverting amplifier is used. This provides a negative voltage -V(IR_s).

Since -V(IR_s) is already negative the subtraction of V(IR_s) from V(V_d) to obtain V(V) is performed by the non-inverting summing amplifier circuit of op-amp 6. The non-inverting amplifier is also used to scale V(V) to V_{ref} for the CDCPS where the scaling factor K is set by the variable resistor R_{scale}.

4.1.2 Performance of the ACC

The ACC was tuned for use in a PVME that has electrical characteristics similar to a BP Solar Saturn 7175 PV module (BP7175S). The PVME combines the ACC with a

CDCPS that has a voltage gain of 20. The electrical characteristics of the BP7175S taken from the datasheet in Appendix B are given in Table 4.1.

P_{mpp} (W)	V_{mpp} (V)	I_{mpp} (A)	I_{sc} (A)	V_{oc} (A)
175	36	4.9	5.2	44.2

Table 4.1: Electrical characteristics of the BP7175S

The system in Figure 4.4 was set up to determine the electrical characteristics of the ACC. The DC voltage supply was controlled manually so that I could be varied from 0A to the short circuit current I_{sc} of 5.2A. Readings of the resulting V_{ref} from the ACC and I were taken at suitable intervals.

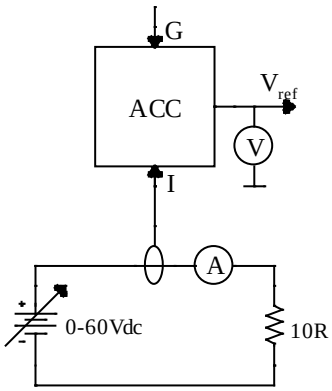


Figure 4.4: Test setup to find ACC characteristics

The expected performance of the ACC as part of a PVME has been derived from the test results by multiplying V_{ref} by the CDCPS gain of 20. Table 4.2 compares the estimated PVME electrical characteristics with the BP7175S datasheet values.

	P_{mpp} (W)	V_{mpp} (V)	I_{mpp} (A)	I_{SC} (A)	V_{OC} (A)
BP7175S	175.0	36.0	4.90	5.200	44.2
PVME	172.9	36.4	4.75	5.206	44.0

Table 4.2: Expected performance of the ACC in a PVME

The expected PVME values are all within ±1.5% of the values given on the BP7175S datasheet, apart from I_{mpp} which is approximately 3% less. Figure 4.5 confirms that the

measured I–V characteristic of the ACC closely matches the curve given on the BP7175S datasheet. The PVME is therefore expected to give an accurate representation of the BP7175S characteristic curves.

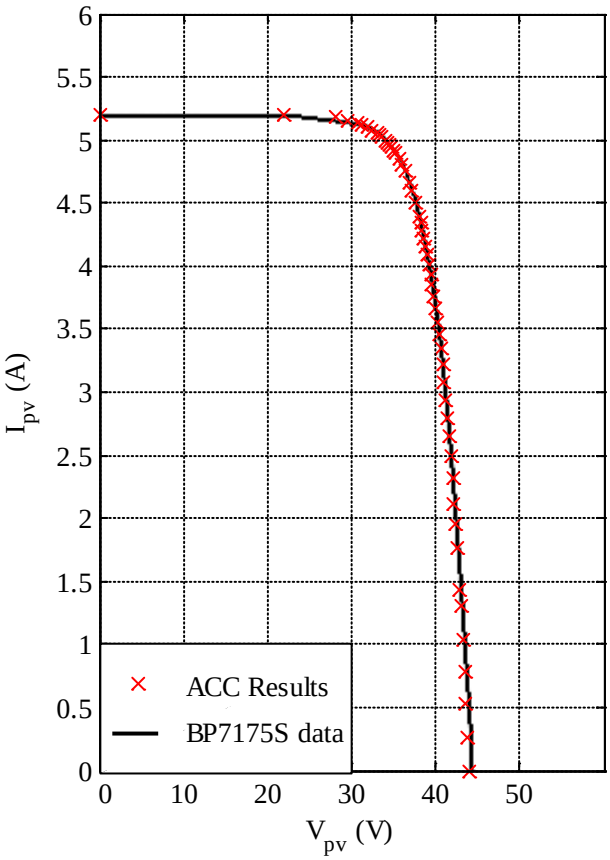


Figure 4.5: ACC Characteristic Curves

4.2 Digital Lookup Computation Method

A PV array emulator (PVAE) can be used to test the behaviour of a PV inverter that would require voltage and power levels greater than available from a PVME. In designing a controller for a PVAE, consideration should be given to emulation of partial shading conditions. The comparison of computation methods in Chapter 3 provides evidence that the digital lookup computation system (DLCS) is the optimum choice for emulation of PV arrays subjected to partial shading. Therefore a DLCS has been selected for control of a PVAE.

Figure 4.6 displays the block diagram of the DLCS design. The system uses a MATLAB based PV array simulator to generate lookup tables of the PV characteristics. The user can set the parameters for the PV array simulation through a MATLAB graphical user interface (GUI).

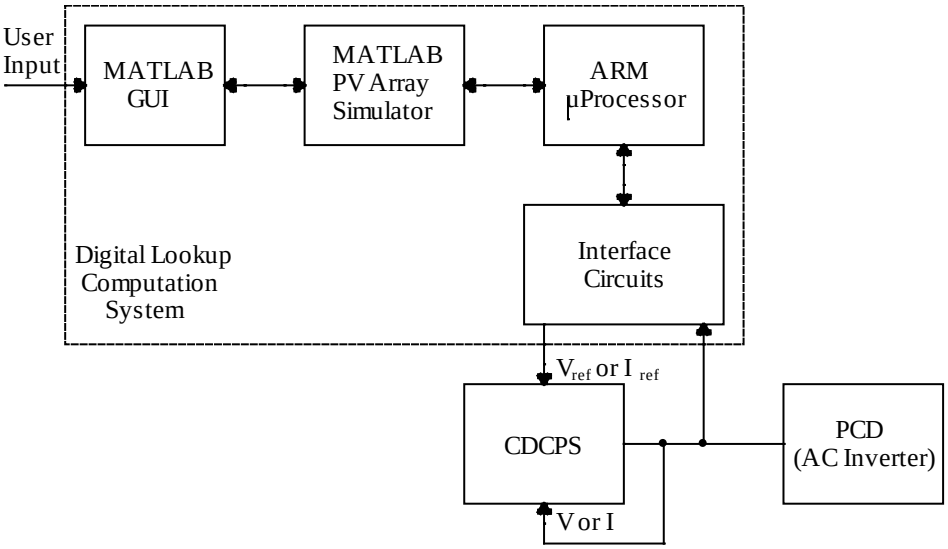


Figure 4.6: Block diagram of PVAE using a DLCS

Once generated, the lookup table can be loaded into a microprocessor for running the PVAE. The digital microprocessor interacts with the controllable DC supply (CDCPS) of the PVAE through the interface circuits. This section describes the design of each of the DLCS system components.

4.2.1 MATLAB Based Array Simulator and GUI

The DLCS design uses a MATLAB based PV array simulation programme 'PVArraySim'. PVArraySim has been developed to simulate PV arrays subjected to partial shading patterns determined by the user. The PV array configuration used in PVArraySim consists of parallel strings of series connected PV modules as illustrated in Figure 4.7. Both the number of parallel strings N_{str} and the number of PV modules per string N_{mod} are set by the user as this section goes on to explain.

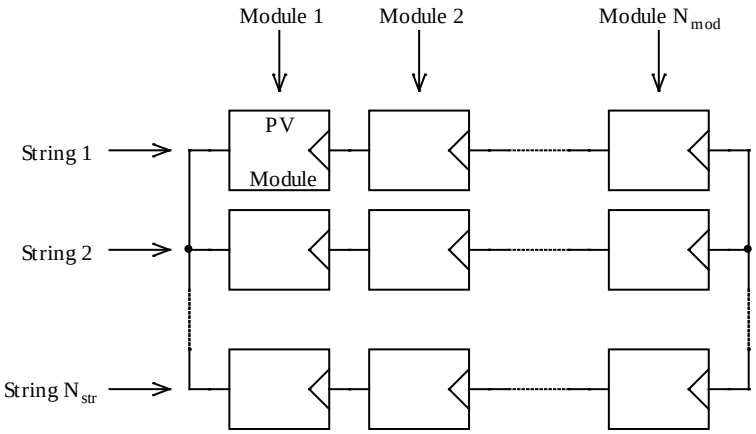


Figure 4.7: PV array configuration for PVArraySim

PVArraySim uses a GUI for user input of simulation parameters and generates a lookup table for the PVAE. The high level flow diagram of the main programme code is given in Figure 4.8 and the PVArraySim MATLAB programme provided on the accompanying CD.

PVArraySim uses a database of PV modules stored as a Microsoft Excel spreadsheet. The database is taken from the PV simulation programme PVSYST (v4.33) [87], a tool for analysing and predicting annual energy yield for a PV system based on the system's physical position, orientation and surrounding environment. The database includes the manufacturer and PV module model name along with the following parameters:

N_s	Number of cells in series
N_p	Number of cells in parallel
G_{ref}	Reference irradiance level
T_{ref}	Reference cell temperature
$V_{oc}\|_{ref}$	Open circuit voltage at reference irradiance and temperature
$I_{sc}\|_{ref}$	Short circuit current at reference irradiance and temperature
K_I	Short circuit current temperature coefficient
K_V	Open circuit voltage temperature coefficient
$R_p\|_{ref}$	Diode model parallel resistance at reference irradiance and temperature
$R_s\|_{ref}$	Diode model series resistance at reference irradiance and temperature
N_d	Number of bypass diodes

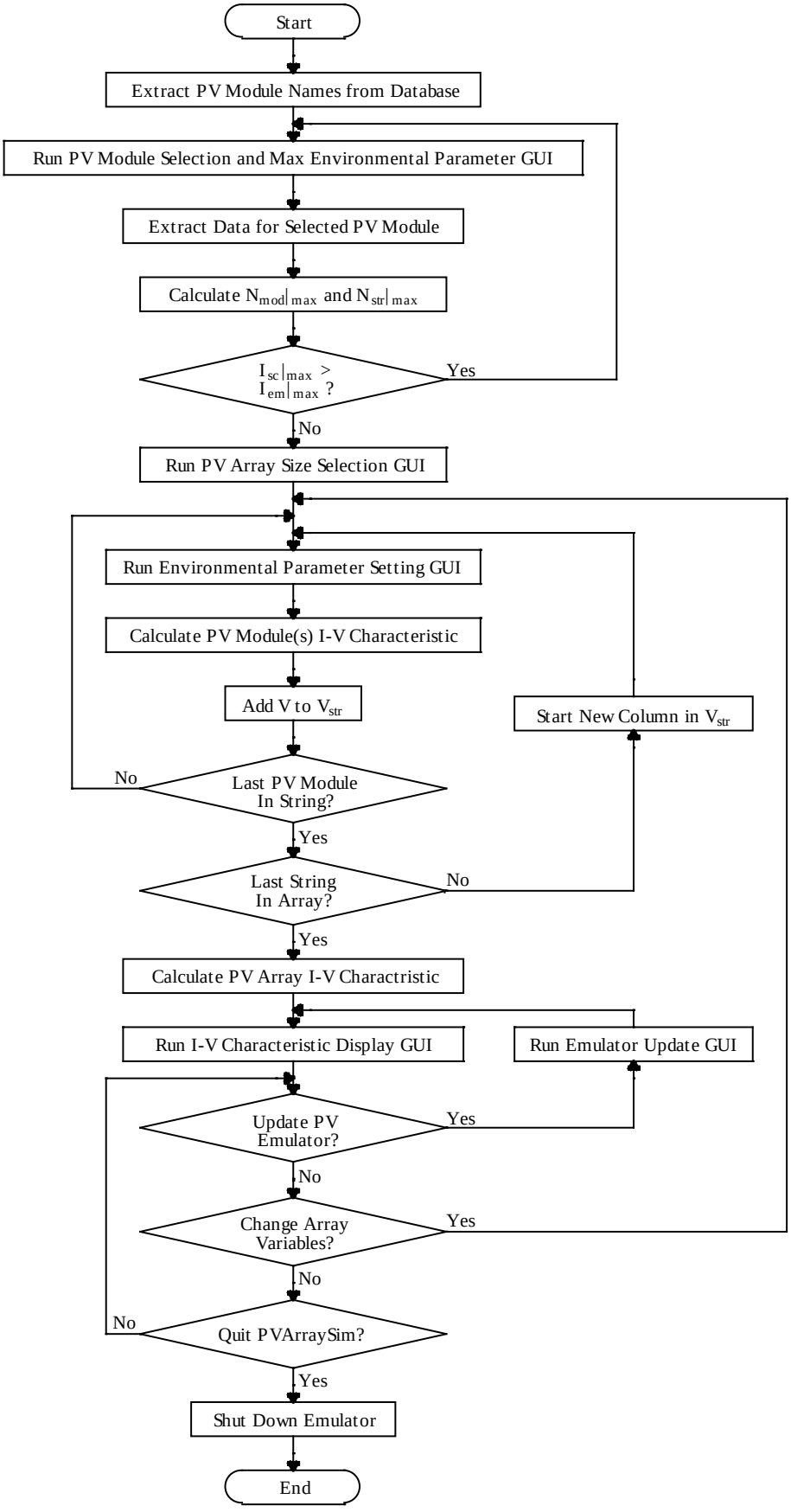


Figure 4.8: High level flow diagram for MATLAB programme PVArraySim

To allow the user to choose the PV module PVArraySim starts with extraction of lists of PV module manufacturer and model names from the Excel database. The lists are passed to the GUI PVArrayParams, for which the flow diagram is depicted in Figure 4.9. Since PVArraySim has been developed for simulating mismatch due to partial shading it does not allow an array comprised of different PV modules and only a single type of PV module model can be selected.

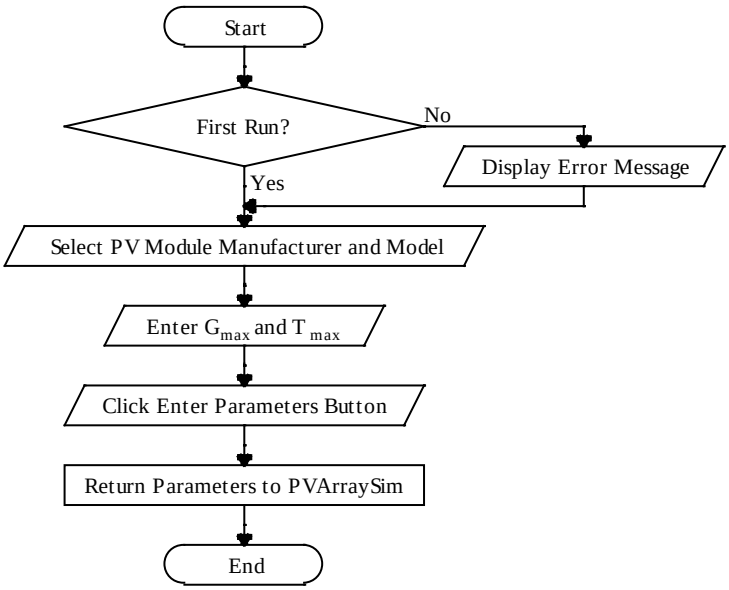


Figure 4.9: PVArrayParams GUI for selecting PV module

For calculating the maximum open circuit voltage $V_{oc}|_{max}$ and maximum short circuit current $I_{sc}|_{max}$ of the simulated PV modules the values for the maximum irradiance G_{max} and temperature T_{max} required during the simulation must also be entered in the PVArrayParams GUI whilst the minimum temperature T_{min} is set to -10°C. PVArrayParams returns $V_{oc}|_{max}$ and $I_{sc}|_{max}$ along with the selected PV module model to PVArraySim once the 'Enter Parameters' button is pressed.

The model parameters of the selected PV module are extracted from the Excel database for use in the PV simulation. The maximum number of series connected PV modules

per string $N_{mod}|_{max}$ and the maximum number of strings connected in parallel $N_{str}|_{max}$ are then calculated.

The limit $N_{mod}|_{max}$ is set by the maximum emulator output voltage $V_{em}|_{max}$ and $V_{oc}|_{max}$. The resulting value is the maximum number of series connected PV modules per string and so is rounded down to the nearest integer value.

$$N_{mod}|_{max} = \frac{V_{em}|_{max}}{V_{oc}|_{max}} \quad \textbf{(4.1)}$$

Since K_V is negative $V_{oc}|_{max}$ occurs at T_{min} as shown by equation (4.2). All other PV module parameters are taken from the database. Chapter 2 explained that the effect of irradiance on V_{oc} is deemed to be negligible.

$$V_{oc}|_{max} = V_{oc}|_{ref} + K_V(T_{min} - T_{ref}) \quad \textbf{(4.2)}$$

If $N_{str}|_{max}$ is less than 1 the combination of G_{max} and T_{max} entered has resulted in a PV module $I_{sc}|_{max}$ that is too large for the emulator. In this case PVArraySim loops back to the PVArrayParams GUI where the user is notified of the error and prompted to re-enter suitable G_{max} and T_{max} levels.

The limit $N_{str}|_{max}$ is set by the maximum emulator output current $I_{em}|_{max}$ and $I_{sc}|_{max}$. The resulting value is the maximum number of parallel strings of PV modules and is therefore rounded down to the nearest integer value.

$$N_{str}|_{max} = \frac{I_{em_{max}}|_{max}}{I_{sc_{max}}|_{max}} \quad \textbf{(4.3)}$$

The PV module parameters extracted from the database are used to calculate $I_{sc}|_{max}$ which occurs at G_{max} and T_{max}.

$$I_{sc}|_{max} = I_{sc}|_{ref}\frac{G_{max}}{G_{ref}}\left(1 + K_I(T_{max} - T_{ref})\right) \quad \textbf{(4.4)}$$

Once a suitable combination of PV module, G_{max} and T_{max} has been selected and PVArraySim has calculated the values of $N_{mod}|_{max}$ and $N_{str}|_{max}$, the ArraySizeParams GUI described by the flowchart of Figure 4.10 is run. If the user enters values for N_{mod} and N_{str} that are both integers within the limited range these values are returned to PVArraySim. If the values entered by the user are not appropriate then the user is notified and prompted to re-enter the values.

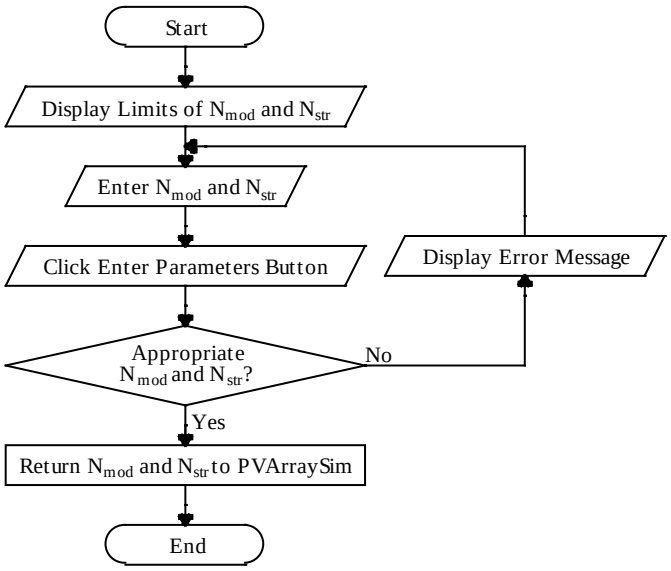


Figure 4.10: ArraySizeParams GUI for setting PV array size

After the PV array configuration parameters of module type and array size have been entered the user defines the environmental parameters for the simulation on a per-module, sub-string or string basis. The environmental parameters are entered through the SysVarEntry GUI, defined by the flow diagram in Figure 4.11. The PV module voltage values V of the I-V characteristic are calculated at PV module current values I from 0A to $I_{sc}|_{max}$ in 1000 equal steps. The iterative generalised Newton's method described in [67] is used to determine the characteristic described by the single-diode model equation, derived from Chapter 2.

$$I_{ph} - I - I_o\left(e^{\left(\frac{V+IR_s}{V_{th}}\right)} - 1\right) - \frac{V+IR_s}{R_p} = 0 \qquad \textbf{(4.5)}$$

The photo-generated current I_{ph}, dark saturation current I_o, thermal voltage V_{th}, series resistance R_s and parallel resistance R_p are converted from the reference levels to the level determined by the environmental parameters using the equations given in Chapter 2.

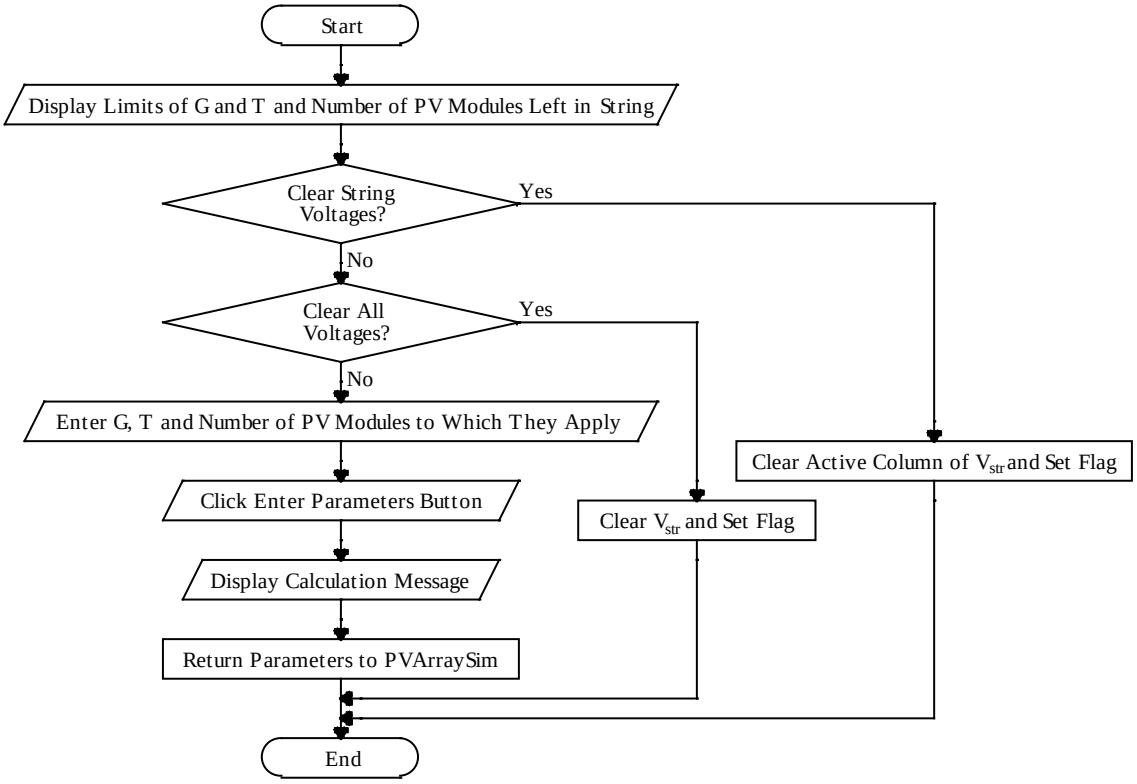


Figure 4.11: SysVarEntry GUI for entering environmental parameters

Since the voltage values for each PV module were calculated at the same string current values, the string voltage V_{str} is the sum of the module voltages. The variable V_{str} holds the voltage values for each string in a separate column. SysVarEntry allows the user to cancel the previously calculated voltage values, either for just the present string or for the whole array. As indicated in Figure 4.11 the appropriate voltage values are cleared from V_{str} and a flag is set to tell PVArraySim to reset the PV module count variables.

If the simulated PV array consists of only a single string then the array characteristic is given by V_{str} and I. However, if the array contains multiple strings then the characteristic needs to be determined. Since the strings are in parallel the array current

I_{arr} will be the sum of the string currents I_{str}. To calculate this sum the generated string characteristics need converting to have equivalent voltage values.

The conversion process is performed by linear interpolation and extrapolation of I_{str} so that they fit a general set of array voltage V_{arr}. The V_{arr} values run from 0V to the maximum string voltage $V_{str|max}$ in 1000 equal steps. The sum of I_{str} is determined at each value of V_{arr} to give I_{arr} with any points that result in a negative I_{arr} value removed. The PV array characteristic is then defined by V_{arr} and I_{arr}.

The ARM microprocessor in the DLCS uses a novel lookup table method as is described in the next subsection. The method uses either the effective load resistance R_{eff} or effective load conductance G_{eff} as the input to the lookup table depending on the controlled output variable of the PVAE being voltage or current respectively. This allows operation of the PV emulator in both voltage and current control mode so that operation across the entire I-V characteristic is possible.

The array characteristic is used to generate both lookup table formats for downloading into the microprocessor. Therefore the number format must also be changed from floating point variables to quantised integer variables that can be transmitted via RS232 and stored in the microprocessor.

Both R_{eff} and G_{eff} will have a set range of values as illustrated in the following subsection. To transform the array I-V characteristic to the lookup table format linear interpolation and extrapolation are used to find the corresponding digital voltage values V_{dig} and digital current values I_{dig} in the same manner as for calculating I_{str}.

PVArraySim runs the DisplayIVCurve GUI of Figure 4.12 that displays the simulated characteristics and parameters of the PV array. DisplayIVCurve waits for the user to press 1 of 3 buttons that allow the environmental parameters to be altered, the UpdateEmulator GUI to be run or to quit PVArraySim. Figure 4.8 indicates that to alter

the environmental parameters, PVArraySim loops back to the appropriate section. PVArraySim has been programmed to do this when neither the Update Flag nor Quit Flag are set. If the Update Flag is set then PVArraySim will run UpdateEmulator whereas if the QuitFlag is set the programme will tell the emulator that the programme is finishing before it ends.

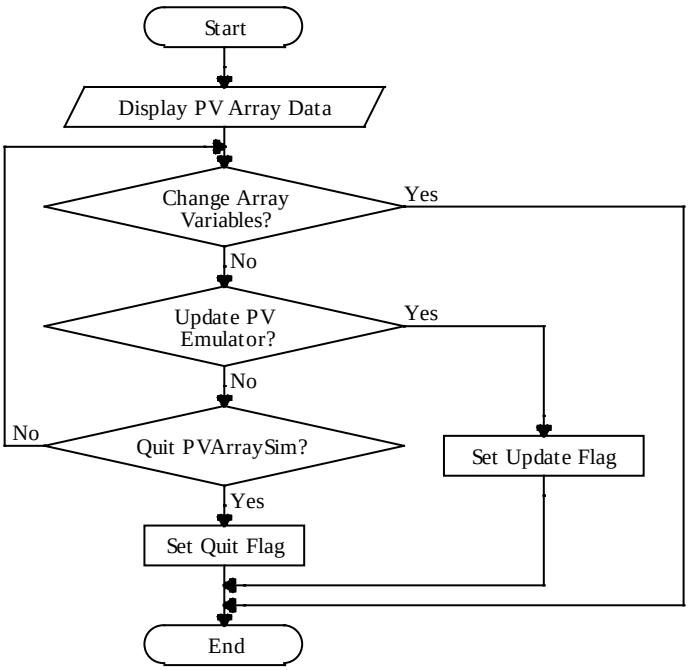


Figure 4.12: DisplayIVCurve for displaying PV array characteristics

A trial run of the MATLAB simulator PVArraySim produced a realistic I-V curve for a mismatched string of four BP7175S PV modules as shown in the screenshot of Figure 4.13. As well as displaying the I-V curve it can be seen that the P-V and P-I curves are also presented along with the MPP values. This information is useful for the user whilst testing with the PVAE.

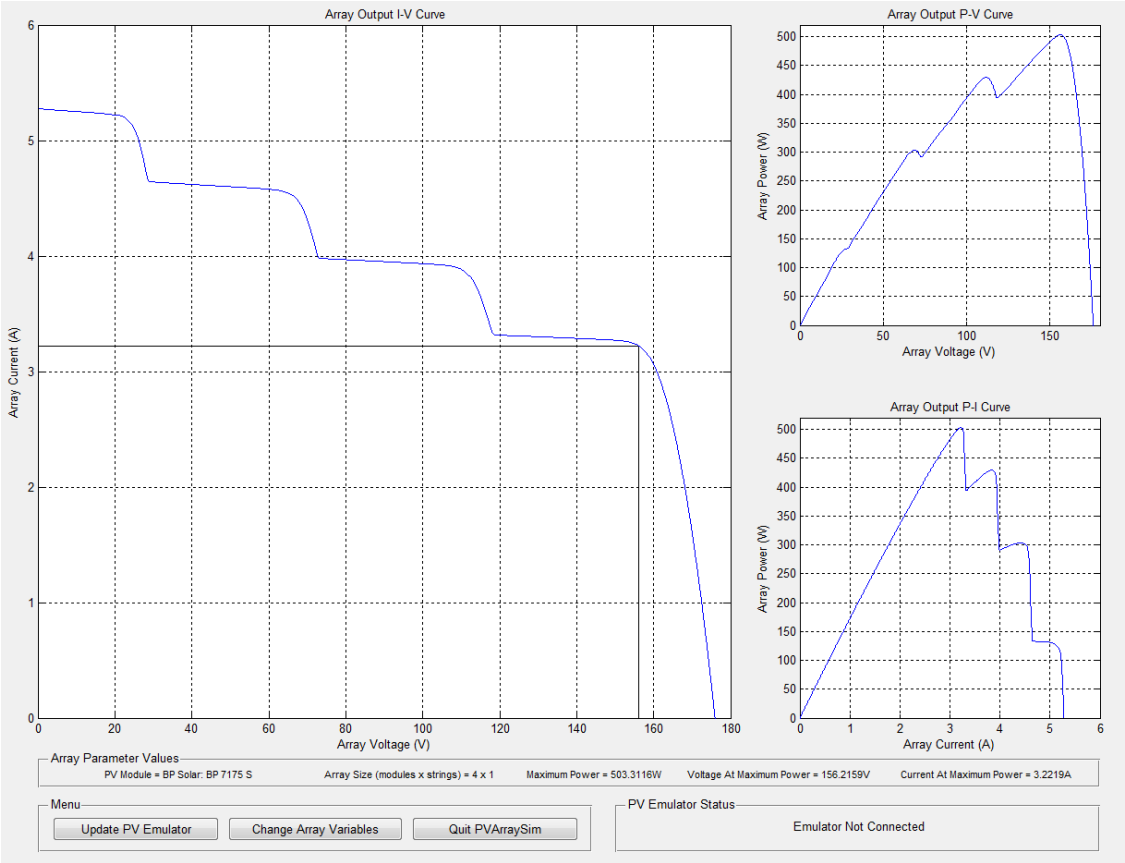


Figure 4.13: Screenshot of DisplayIVCurve GUI

4.2.2 Microprocessor System

To complete the digital lookup computation system (DLCS) of Figure 4.6 the lookup tables generated by the MATLAB programme described in the previous section need to be applied to the controllable DC power supply (CDCPS). A microprocessor system can be used to provide the interface between the MATLAB programme and the CDCPS with the generated lookup tables downloaded into the microprocessor via an RS232 serial interface.

A typical microprocessor usually has an on-chip 10 bit successive approximation analogue to digital (A/D) converter with the possibility of multiplexing analogue input channels. This can be used for taking voltage and current measurements from the power electronics using the appropriate transducer interface circuits. These circuits will

provide electrical isolation from the power circuits for protection of the microprocessor whilst scaling the measurement signal to the A/D converter range.

Although the A/D converter has a 10 bit resolution it is possible to mask out the least significant bits (LSBs) in software. There are two advantages to this: reducing the size of the lookup tables by around half per masked out bit, thus reducing download time, and reducing the sensitivity to noise on the measurement signal. However this comes at a cost of resolution of the measurement voltage $V_{m|res}$ as shown in Table 4.3 for a typical 3V A/D converter.

Number of bits	$V_{m\|res}$ (mV)
6	47.62
7	23.62
8	11.76
9	5.87
10	2.93

Table 4.3: Measurement resolution of on-chip 3V A/D converter

A size of 8 bits is appropriate since this gives good noise rejection of >10mV at the A/D input whilst still allowing an accurate operation.

An on-chip pulse width modulation (PWM) module is also usually included in a microprocessor. This can be used as part of a digital to analogue (D/A) conversion scheme for producing an analogue reference signal for the CDCPS. The PWM output from the microprocessor is passed through an optocoupler that provides electrical isolation from the power circuits for protection. The signal is then passed to an active filter to remove the AC components of the signal and leave the DC average value. The filter can also scale the signal to the range required by the CDCPS. The PWM should have as high a frequency as possible so that the effect of the filter bandwidth on the system speed of response is minimised.

The MATLAB simulation data is converted into two lookup tables. The first gives a

reference for the emulator current I_{em} as a function of G_{eff} to allow the current to be controlled up to short circuit. The second gives a reference for the emulator voltage V_{em} as a function of R_{eff} to allow the voltage to be controlled up to open circuit.

The load conductance or resistance is used as the lookup table input variable as opposed to the usual current or voltage since this reduces the instability caused by the interdependency of the voltage and current [88] and the input to the table is now only dependent on the load value. However, the value for R_{eff} or G_{eff} would be derived from the measurements of emulator voltage and current so care needs to be taken to prevent any energy storage in the system from confusing the DLCS by presenting a false load reading.

The digital values for the current I_{dig} and voltage V_{dig} are binary integers and are dependent on the analogue values I_a and V_a, the maximum analogue value of the emulator and the number of bits n used in the A/D conversion:

$$V_{dig} = V_a \frac{2^n - 1}{V_{em}|_{max}} \qquad \textbf{(4.6)}$$

$$I_{dig} = I_a \frac{2^n - 1}{I_{em}|_{max}} \qquad \textbf{(4.7)}$$

To obtain the digital value of the resistance R_{dig} the quotient of V_{dig} to I_{dig} is calculated. An expression relating the analogue resistance R_a to R_{dig} is derived by dividing (4.6) by (4.7) and re-arranging:

$$R_a = R_{dig} \frac{V_{em}|_{max}}{I_{em}|_{max}} \qquad \textbf{(4.8)}$$

Since R_{dig} is an integer value the analogue resistance resolution ΔR_a is given by:

$$\Delta R_a = \frac{V_{em}|_{max}}{I_{em}|_{max}} \qquad \textbf{(4.9)}$$

For a PVAE capable of supplying hundreds of volts but less than 10A the resolution in resistance will be poor. Therefore, a shift of s bits can be introduced to V_{dig} when calculating the digital resistance to provide a better resolution for the analogue resistance:

$$R_{dig} = \frac{2^s V_{dig}}{I_{dig}} \quad \textbf{(4.10)}$$

$$\Delta R_a = \frac{V_{em}|_{max}}{2^s I_{em}|_{max}} \quad \textbf{(4.11)}$$

However, as s is increased the number of lookup table values $N_{l\text{-}up}$ required to describe the possible unique values of R_{dig} will also increase requiring more memory for storage and a longer time for downloading from MATLAB.

To avoid dividing by zero when I_{dig} is zero, the calculation of R_{dig} is skipped and the emulator reference voltage V_{ref} is set to the open circuit voltage V_{oc}. The same arguments given for the resistance also apply to the conductance except that I_{dig} is divided by V_{dig} and the current reference is set to I_{sc} when V_{dig} is zero.

To observe the characteristics of the two lookup table formats an example I-V curve, intentionally made complex with various levels of mismatch, has been converted to both lookup tables and are plotted in Figure 4.14. The plots show a close match to the desired curve, except at close to short circuit for the R_{eff}-to-V_{em} lookup table and close to open circuit for the G_{eff}-to-I_{em} lookup table where the table data rapidly diverges.

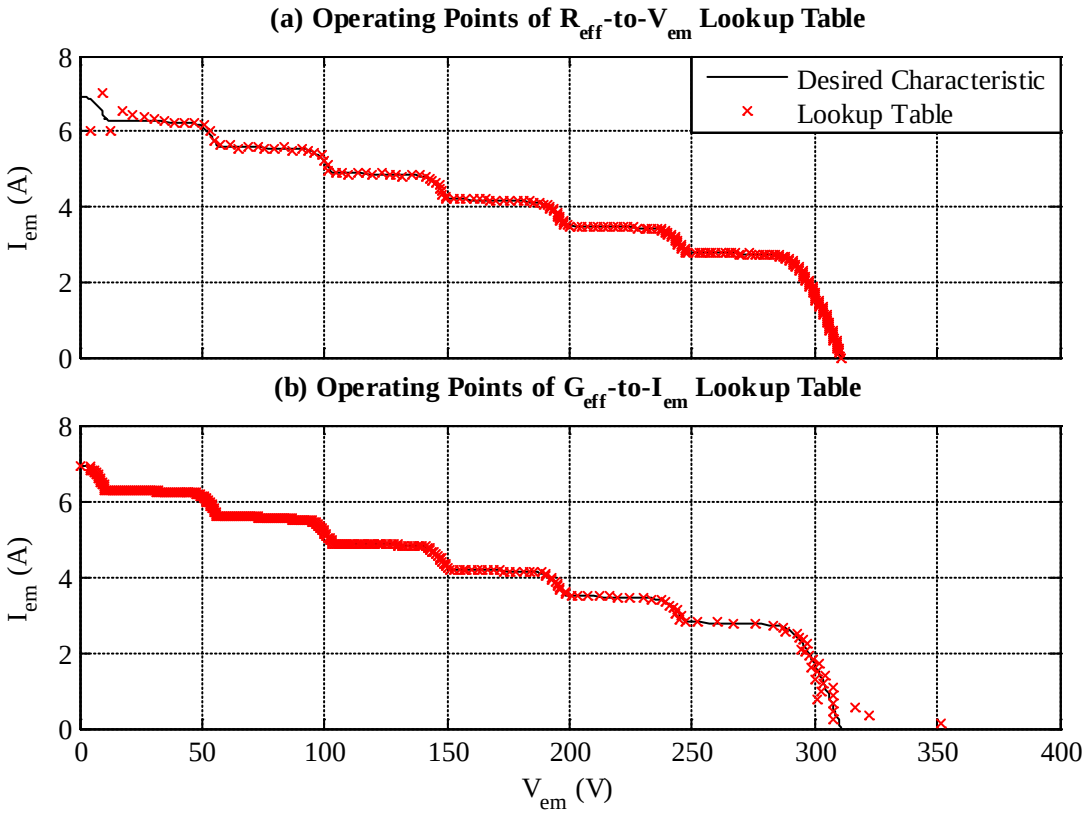


Figure 4.14: Operating points of lookup table formats for example I-V curve

To avoid the areas of divergence in Figure 4.14 and allow operation across the whole I-V characteristic a control technique that switches between the two tables can be used. The controlled output variable will depend on the effective value of the connected load and the point of operation on the I-V characteristic. To avoid continuous switching between the two lookup tables the control law should include some form of hysteresis.

4.3 Summary of Control of a PVE

This Chapter provides detailed descriptions of the development of two types of computational control for a PV emulator (PVE): an analogue computation circuit for a PV module emulator (PVME) and a digital lookup computation system (DLCS) for a PV array emulator (PVAE).

The reasons given for selecting an ACC for use with a PVME are the requirement of a fast PVE for testing per-module power optimisers and the flexibility to emulate a range

of I-V characteristics. Details on the design of the ACC are given and the practical testing has demonstrated an accurate reproduction of a static I-V characteristic.

The next section explains that the primary reason for designing a DLCS for a PVAE is the flexibility it offers for emulation of partial shading conditions within a PV array. The DLCS is split into two sections: a MATLAB based PV array simulator, and a microprocessor with interface circuits.

The flow diagrams of the MATLAB simulator were presented to illustrate the development of the simulation programme PVArraySim. The programme is broken down into sections that use graphical user interfaces (GUIs) to allow the user to enter the desired PV array configuration and conditions. Once the I-V curve has been generated a GUI displays the curve and allows it to be downloaded to the microprocessor or lets the user re-enter the environmental conditions. A screenshot displaying an I-V curve from a trial run shows a realistic mismatched characteristic.

A novel lookup table method was designed for use in a microprocessor. This method was based on using the effective load resistance or conductance as the input variable for the lookup table to improve the stability. However, care must be taken when applying this method in a real PVE since energy storage devices may present a false effective load.

Chapter 5 PV Emulator with Controllable DC Power Supply

Chapter 4 has described the development of two computational methods for a PV emulator (PVE): the analogue computation circuit (ACC) for use with a PV module emulator (PVME) and the digital lookup computation system (DLCS) for use with a PV array emulator (PVAE). Both the ACC and DLCS require a controllable DC power supply (CDCPS) to produce the electrical power output of the PVE. The PVAE is flexible in that it is used for testing any PV inverter (PVI) of 3kW or less whereas the PVME is used for testing power optimisers such as the SolarMagic (SM).

The maximum power point (MPP) tracking of PCDs means that they behave as an active dynamic load. The essential first criterion for correct operation of the PVE is a response that is fast enough to not confuse the PCD's maximum power point tracker (MPPT). The absolute limit for the settling time of the PVE output is less than the minimum MPPT update time of the PCD under test.

MPPTs of certain PVIs, especially those with an I-V scanning procedure, cause the inverter to operate in both the open circuit and short circuit regions of a PV module or array. The second criterion for correct operation of the flexible PVAE is therefore the ability to operate across the whole I-V characteristic.

This chapter investigates the suitability of various CDCPSs for use in both the PVME and PVAE systems. Each PVE system was therefore subjected to a test for each criterion:

a) A static load test, to determine the operation of the system across the I-V characteristic.

b) A dynamic passive load test, to obtain the response time of the PVE output.

c) Once the PVE was shown to operate to the specified standard, an appropriate PCD device was connected to observe the performance with an active load.

A description of the CDCPSs investigated is given in this chapter along with analysis of the test results.

5.1 Commercial Power Supply

A Wayne Kerr AP100-90 was combined with the ACC developed in chapter 3 to assess the suitability for use as a PVME. This section gives a description of the tests performed on the PVME and the limitations that were observed.

5.1.1 PVME Tests using an ACC

The AP100-90 is a 3kW 100V 90A DC power supply. The power supply can accept external control reference voltages for the voltage and/or current. The range of the control voltages is 0V to 5V which corresponds to the maximum range of the selected parameter. This gives the power supply a 'DC gain' of 20 for the voltage output and 14 for the current output.

Test a) The PVME was set up for performing a static load test as shown in Figure 5.1. A switch was included to obtain a reading at open circuit. With the switch closed the rheostat was varied and measurements of output voltage and current were taken at suitable intervals.

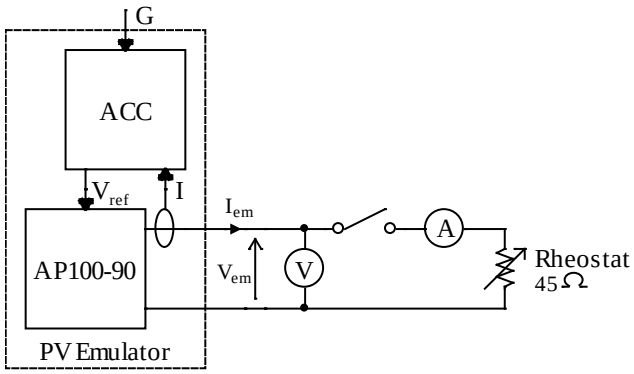


Figure 5.1: Setup for PVME test using a static load

The data points of the resulting characteristic are plotted in Figure 5.2 along with the expected characteristic taken from the results of the ACC tests in Chapter 3. The results show that for static load conditions the PVME is able to accurately reproduce the I-V characteristic from open circuit to around the MPP.

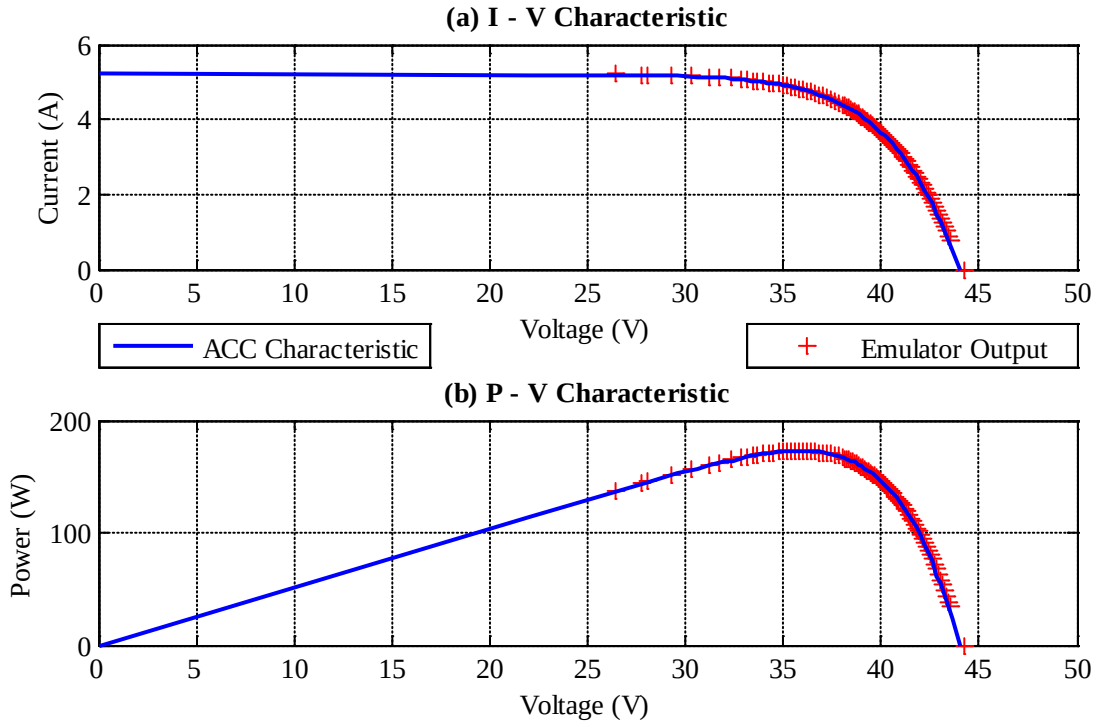


Figure 5.2: Static load test of PVME using an AP100-90 and ACC

The accuracy of the PVME is confirmed in Table 5.1 which shows that the electrical parameters are within 3% of the BP 7175S PV module.

	P_{mpp} (W)	V_{mpp} (V)	I_{mpp} (A)	I_{sc} (A)	V_{oc} (A)
BP 7175S	175.0	36.0	4.90	5.200	44.2
PVME	172.67	36.2	4.77	see below	44.2

Table 5.1: Comparison of PVME output and BP7175S electrical parameters

However, readings could not be taken in the short circuit region as the system became unstable and oscillations occurred in the output and reference. This is demonstrated in the waveforms of Figure 5.3 which were taken at around 25.5V where the oscillations first occur.

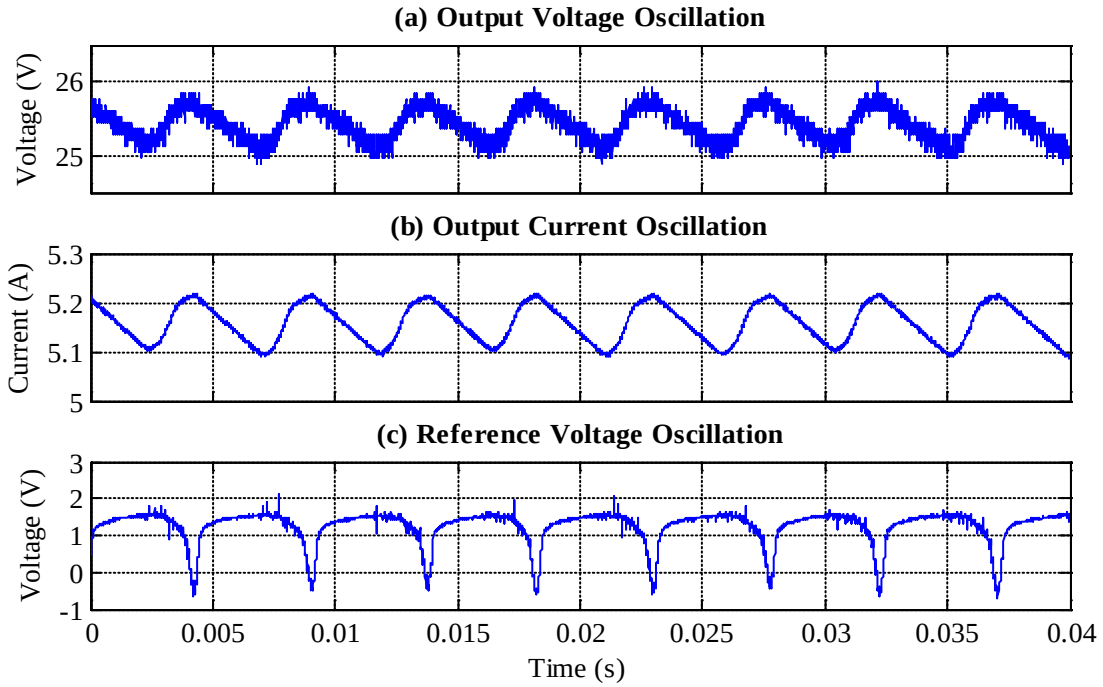


Figure 5.3: Oscillations in PVME system operating in short circuit region

The instability is due to an increasing gain in the PVME system control loop indicated in Figure 5.4 caused by the non-linearity of the ACC I–V characteristic. However, the PVME has been used to test an SM power optimiser which operates from open circuit to around the MPP region avoiding the problem area at short circuit.

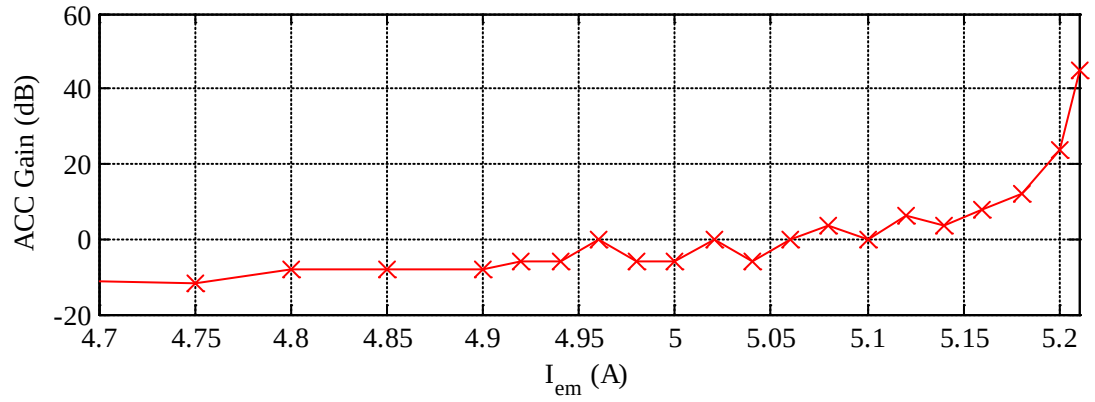


Figure 5.4: ACC gain as a function of I_{em}

Test b) The PVME system was set up for performing a dynamic passive load test as shown in Figure 5.5. R1 and R2 are rheostat type resistors to allow the load resistance to be set. Due to the inductive nature of the wirewound rheostats a negative voltage spike

will be generated when the switches turn off and break the current path. The diodes D1 and D2 are required to provide a path for the current and limit the voltage spike so the switches aren't damaged by an excessive reverse potential.

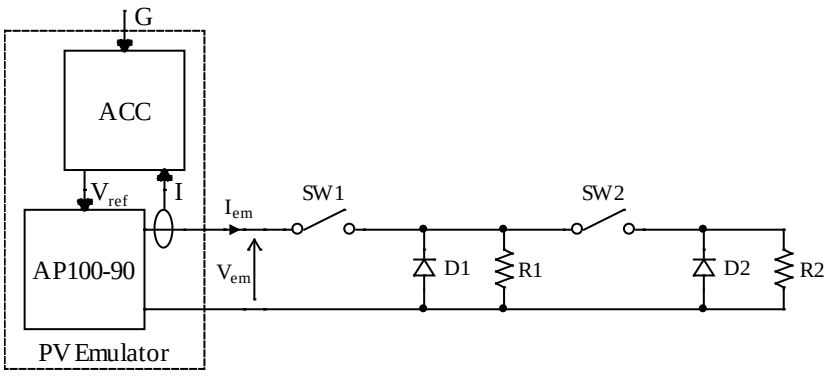


Figure 5.5: Setup for PVME test using a dynamic passive load

R1 and R2 are chosen as 7.7Ω and 290Ω respectively to give 2 points of operation within 0.25V of the PVME MPP. The step changes in load defined in Table 5.2 were applied using a MOSFET switch. The response time of the PVME is defined as the time for the output voltage to settle within 0.1V of the final value.

Initial Load	End Load
R1 = 7.7Ω	Open Circuit
Open Circuit	R1 = 7.7Ω
R1 = 7.7Ω	R1 // R2* = 7.5Ω
R1 // R2* = 7.5Ω	R1 = 7.7Ω

** // indicates a parallel connection of the resistors.*

Table 5.2: Load values for PVME test of step response in load

The results of the load change from MPP to open circuit and back are displayed in plots (a) and (b) of Figure 5.6 respectively. From around 0s to 0.08s graph (a) shows a linear increase in the PVME output voltage (V_{em}). This implies that the AP100-90 has an internal current limiter that charges the output capacitance with a constant current. The apparent step of around 1.5V at 0s indicates a delay before the current limit is applied.

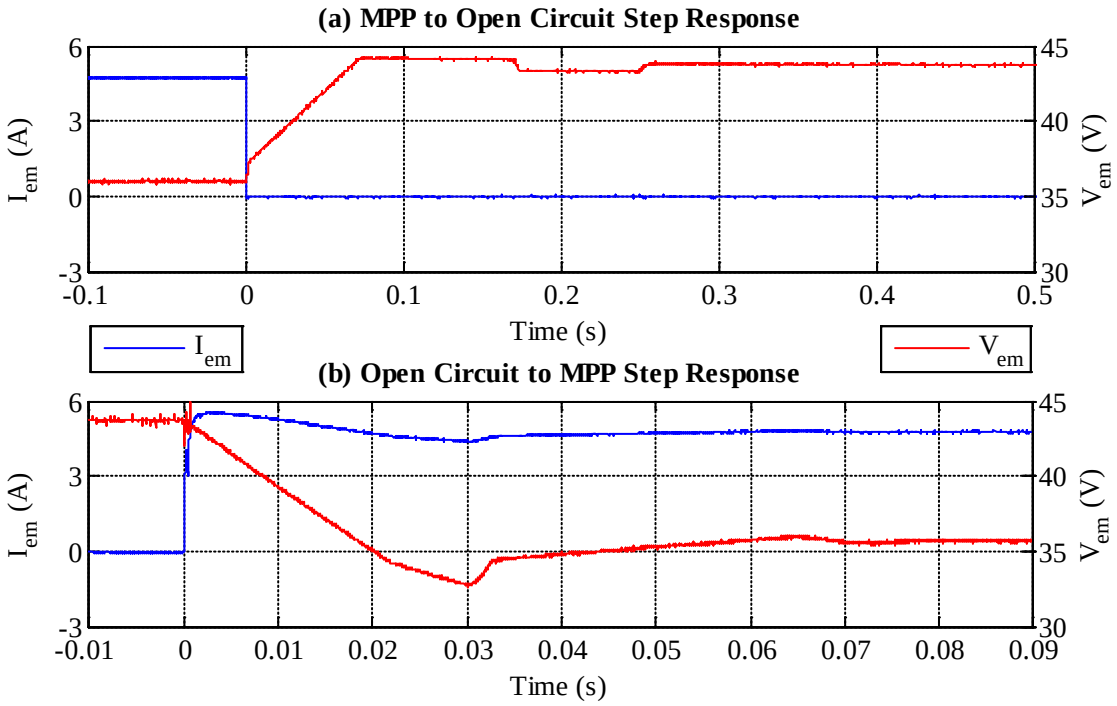


Figure 5.6: Time response of PVME to steps in load resistance

There is a slight overshoot in V_{em} that over-charges the capacitors and, since there is no load current, they are discharged through the AP100-90 internal circuitry. There is an anomaly around 0.18s to 0.25s where there is a depression in the voltage after which the voltage has settled within 0.1V of the final value. Therefore the PVME response time for a step in load from MPP to open circuit is around 0.25s. The PVME response time for a step in load from open circuit to MPP, depicted in graph (b), is around 0.07s. This is the time it takes for V_{em} to settle within 0.1V of the final value.

Figure 5.7 shows the time response of the PVME to a step change in load around the MPP giving a more realistic indication of how the system will operate with an MPPT load.

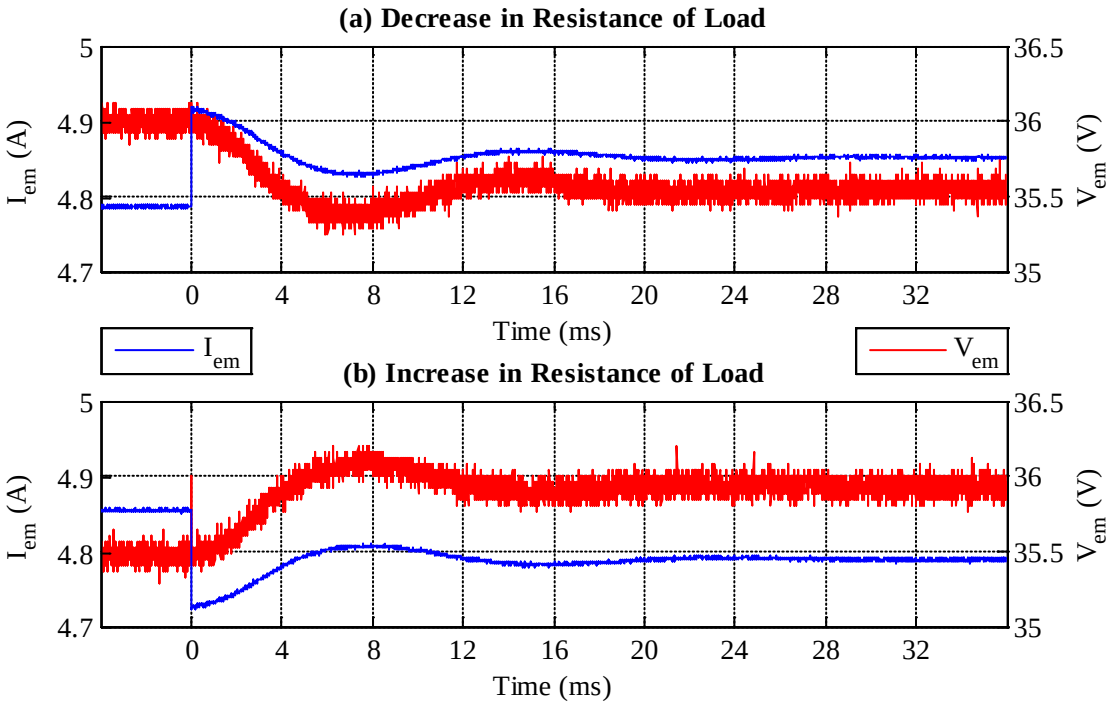


Figure 5.7: Time response of PVME to a load step around MPP

A step change in voltage of the size seen in Figure 5.7 is close to what is seen for the SolarMagic active load test results in section 5.2.4, shown here in Figure 5.8 for reference. In both plots of Figure 5.7 V_{em} has settled to within 0.1V after around 12ms.

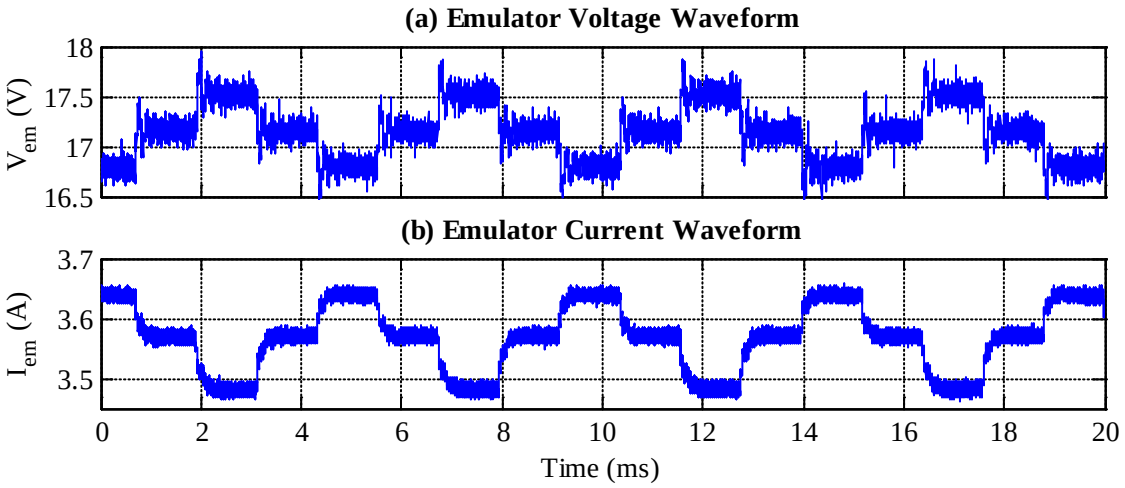


Figure 5.8: PVME waveforms for dynamic active load test

Test c) The PVME was to be used for testing an SM power optimiser. The test results in Chapter 5 report an MPPT update time of 1.2ms for the SM. The AP100-90 PVME system was not likely to function correctly as the response time is around 12ms.

The PVME was tested with an SM to observe what happens when a PVE response time is greater than the MPPT update time of the PCD under test. The test was set up in the configuration of Figure 5.9 with a constant voltage load for the SM. The load voltage V_{out} is regulated using a DC power supply.

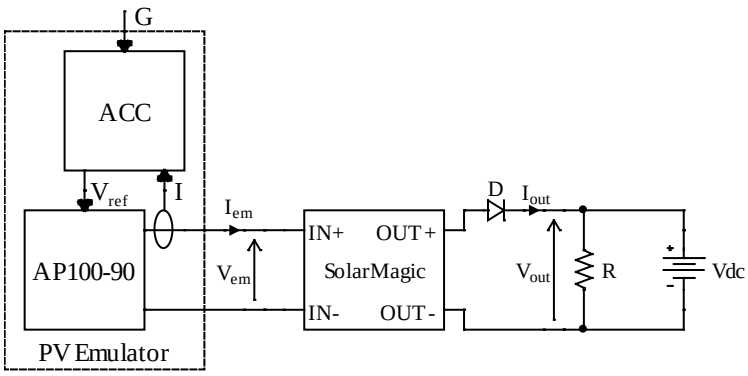


Figure 5.9: Setup for PVME test using a dynamic active load

The resistor R was sized appropriately so that current is always drawn from the DC supply across the whole SM output range. This ensures that V_{out} is always regulated by the DC supply. The blocking diode D is required in case the SM output voltage is below the regulated voltage level. Without D the SM may be damaged by reverse current flow. The size of R is determined by the maximum current that the SM is able to provide at V_{out}, as dictated by the P_{mpp} of the PVME characteristic. A margin of 1A above the maximum current is allowed to ensure that power is always drawn from the DC supply and it is therefore able to regulate the voltage. The SM output voltage level was chosen to be 30V as this is close to the V_{mpp} of the PVME characteristic. The resulting waveforms for the SM voltages and currents are displayed in graphs (a) and (b) of Figure 5.10 respectively.

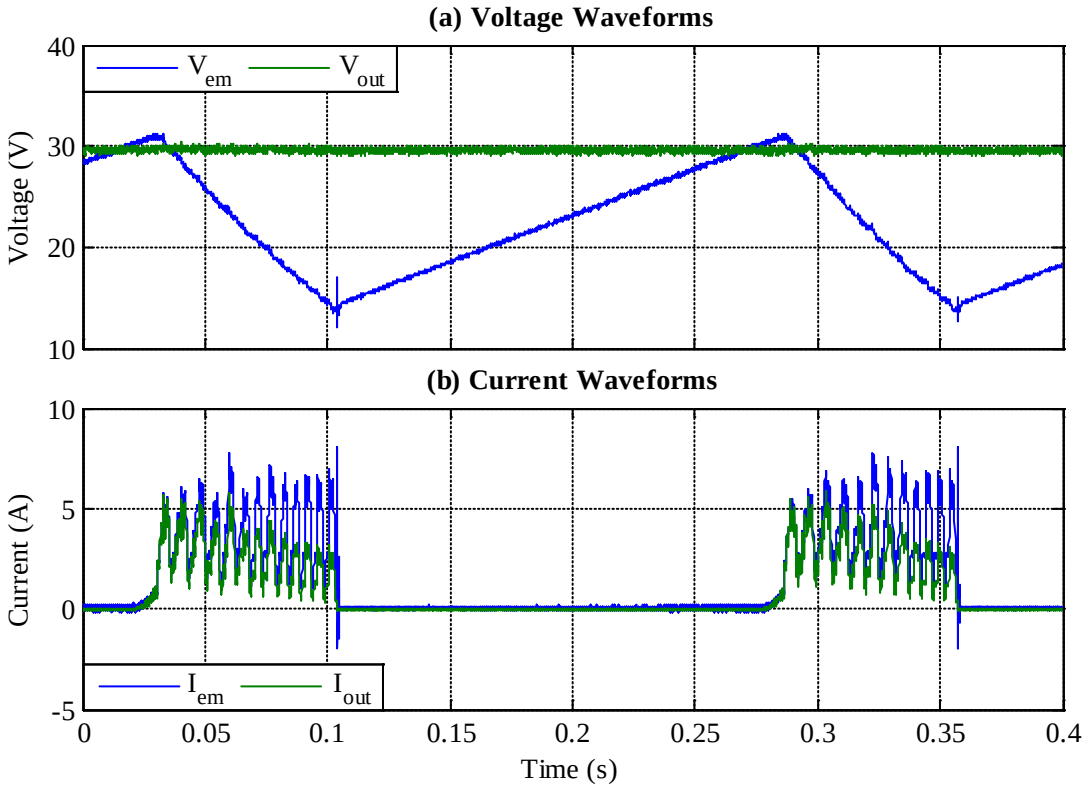


Figure 5.10: Waveforms for the PVME test using a dynamic active load

The SM specification in Appendix B states a minimum operating V_{mpp} of 15V. The current waveforms in plot (b) show that after 0.1s and 0.35s both I_{em} and I_{out} drop to 0A, indicating that the SM has turned off. This corresponds to V_{em} in plot (a) reaching a minimum just below 15V.

Observations made during testing indicate that for start-up of the SM the input voltage must be higher than the load voltage. This can be seen as a rise in the currents at the same time that V_{em} reaches a maximum just above V_{out}.

Figure 5.11 shows the output current and power for the PVME and SM after turn-on. Because of the ripple caused by the switching of the SM power electronics it is difficult to analyse the 4 waveforms in detail. To remove the ripple due to switching from the waveforms displayed in Figure 5.11 the data was post-filtered.

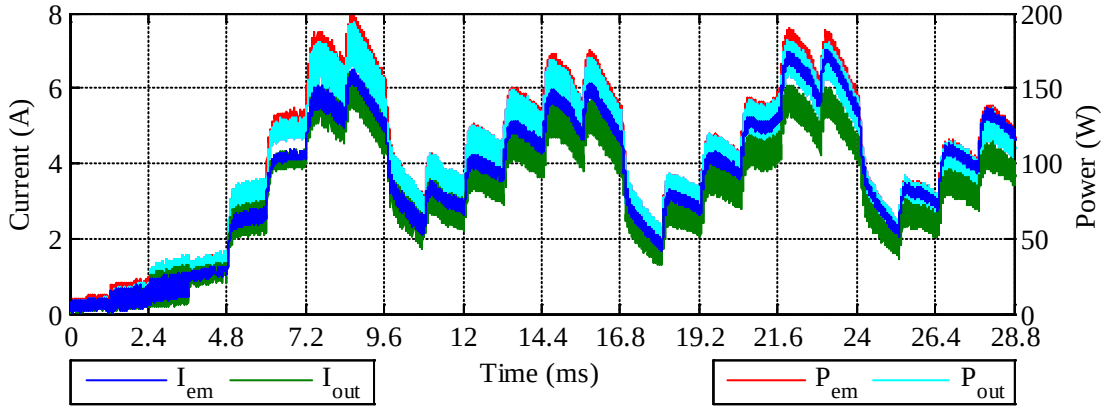


Figure 5.11: Unfiltered SM waveforms of I and P after turn-on

The fast Fourier transform (FFT) of I_{out} was used to determine the switching frequency. The FFT displayed in Figure 5.12 clearly shows a peak indicating a switching frequency of 26.5kHz.

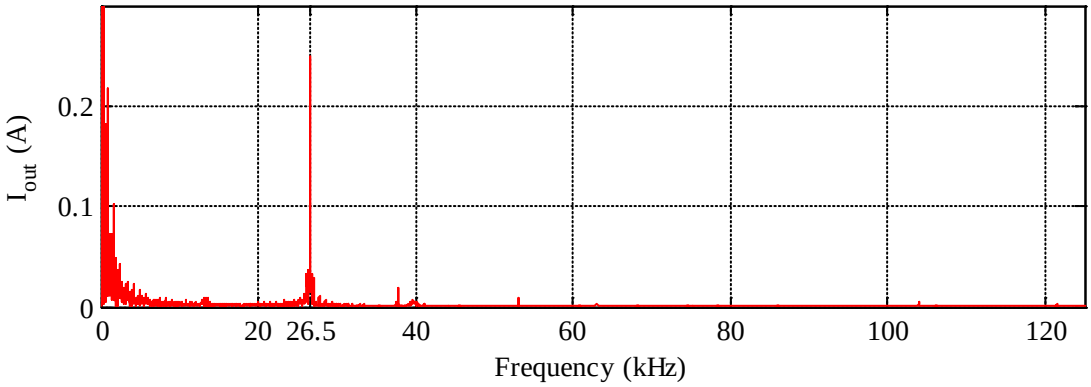


Figure 5.12: FFT of SM output current

The data, filtered using a low-pass filter with cut-off frequency of 10kHz, is plotted again in Figure 5.13 so that the overall shapes of the waveforms are clearly visible. The MPPT period of the SM can be seen as a step-change every 1.2ms.

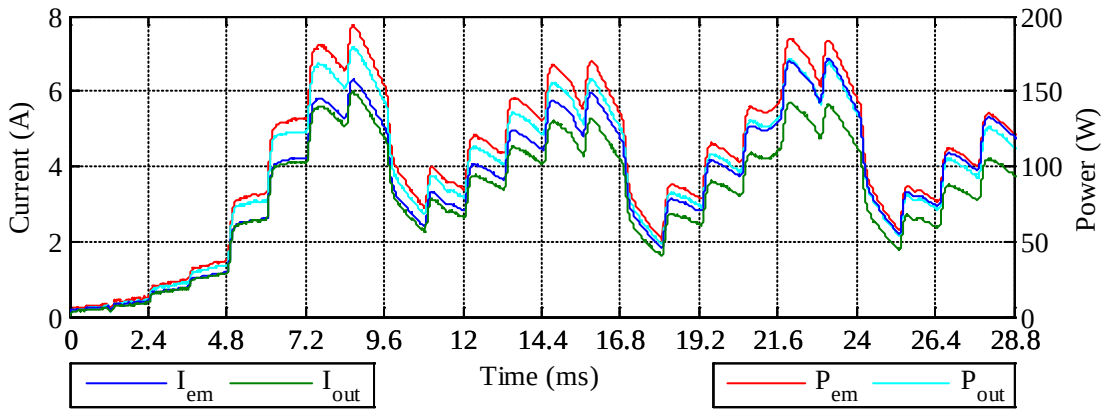


Figure 5.13: Filtered SM waveforms of I and P after turn-on

5.1.2 Limitations of an Off-the-Shelf CDCPS

The results of the static load test in Figure 5.2 show that a PVE comprising an off-the-shelf CDCPS and an ACC can accurately reproduce a PV characteristic from open circuit to around the MPP. This is sufficient for testing PCDs that only operate in this region.

However, the static load test also showed that the system becomes unstable in the short circuit region due to the high gain of the ACC as shown in Figure 5.4. A more complicated control system, such as a variable gain controller, would be required for the CDCPS to ensure that the system remains stable across the entire PV characteristic. It can then be used for testing all PCDs, including those that operate in the short circuit region.

It was observed from the dynamic load tests that the PVE system would not function with the SM connected as the output voltage does not respond fast enough for the MPPT. Therefore the main limitation of an off-the-shelf CDCPS is the dynamic performance. Most off-the-shelf CDCPS units are based on a switching regulator to improve efficiency. Since the switching would result in a ripple on the output voltage a

capacitive filter is used at the output. This reduces the speed of response which may be acceptable for other applications of the CDCPS.

However, as the test results indicate, for a PVE a CDCPS needs to be able to respond to a change in reference within the MPPT period of the connected PCD. This will prevent 'MPPT runaway' where the PVE output is unable to maintain the PV characteristic as the MPPT increasingly draws more power.

Therefore for a PVE it is necessary to develop a dedicated CDCPS. The two main criteria, namely operation across the entire PV characteristic and a response speed less than the PCD MPPT period, can be ensured through proper design of the CDCPS. The next section describes the development of such a CDCPS.

5.2 Developed CDCPS

The previous section described the problems associated with the use of an off-the-shelf DC power supply as the CDCPS of a PVE. An inadequate response time due to the need for output filtering was found to cause incorrect operation of the PVE. To remove the need for filtering and improve performance through a faster speed of response the linear regulator output approach is preferred as illustrated in Figure 5.14.

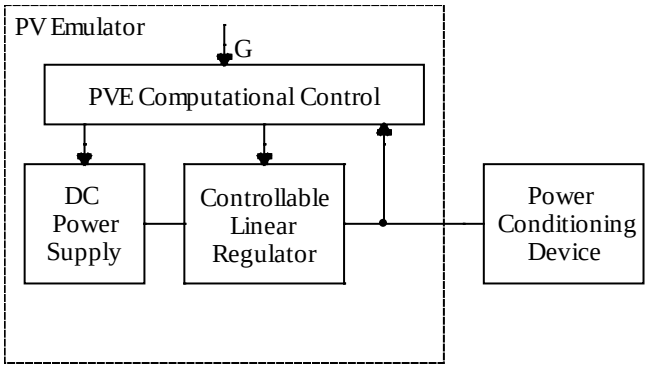


Figure 5.14: System block diagram for PVE with linear regulator

For a PVME the voltage and power levels are sufficiently low for the regulator stage to be designed to cope with the maximum power dissipation. The DC power supply can

therefore be set to a constant voltage. However, the higher voltage and power levels of a PVAE would produce excessive power dissipation in the regulator if the supply voltage was kept constant. Therefore the input supply should be of a controlled switched topology so the supply voltage can be varied without excessive power dissipation.

The design and development of a linear regulator and a controlled rectifier for use in a PVAE system are described in the remainder of this chapter. To emulate typical residential sized PV arrays the PVAE specifications are 3kW, 360V and 8A.

5.2.1 Linear Regulator Design

The linear regulator designed for use in a PVAE is based on a single series connected transistor. An IGBT is preferred to a BJT/Darlington as the IGBT gate has a higher input resistance and lower power consumption for driving the device; it is preferred to a MOSFET due to the voltage levels of a PVAE. The IGBT used in the regulator was the GT100DA60U.

Figure 5.15 shows the system diagram of the linear regulator; the linearisation and PI control circuits are described in later subsections.

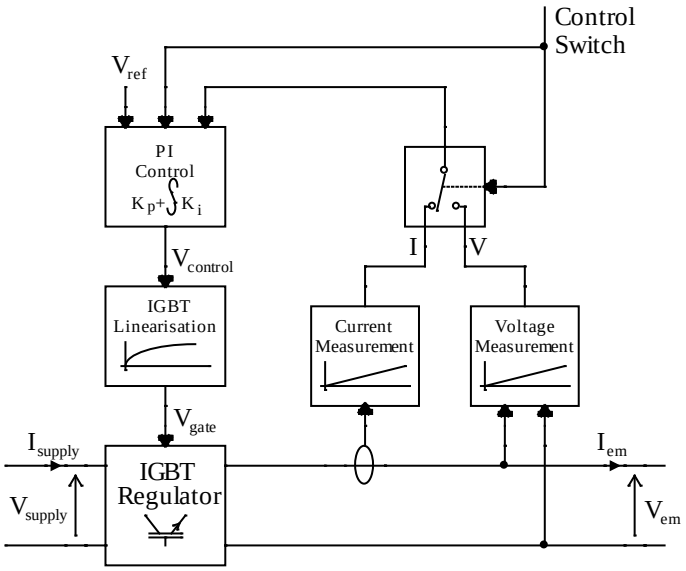


Figure 5.15: Diagram of IGBT regulator system for PVAE

The function of the control switch is explained with the PI control circuit. The voltage measurement and current measurement circuits contain an analogue optocoupler and a Hall-effect transducer respectively in order to isolate the control circuits from the power circuit.

For controlling the output voltage, the voltage across the regulator is varied. To allow a variation in the voltage requires a current flow through the IGBT. For operation at open circuit a parallel 'dummy load' is therefore included to draw a current of at least a few milliamps, as shown in the regulator power circuit of Figure 5.16. If the dummy load was not included there would be no current flowing at open circuit and the loss of control would lead to the undesirable effect of wind-up of the integral control. The diode D protects against reverse voltage across the IGBT of the regulator.

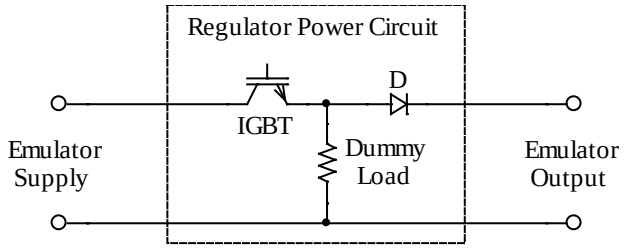


Figure 5.16: IGBT regulator power circuit for PVME

The linear regulator also aids in the minimisation of the ripple generated by the preceding switched rectifier. The ripple specification for the switched rectifier filter is therefore less critical allowing a faster response from the filter. The faster response is important for reducing the power dissipation in the regulator during transient events where a reduction in V_{em} is required and also reducing the current through the controlled rectifier for events where an increase in V_{em} is required.

5.2.2 IGBT Linearisation

The gate-emitter voltage V_{ge} to collector current I_c characteristic of an IGBT is not given by the manufacturer since it is normally assumed that the device will be used as a switch. Therefore the circuit in Figure 5.17 was used to find the IGBT characteristic required for designing the linear regulator. The collector-emitter voltage V_{ce} was supplied using a Farnell AP60-50 power supply and V_{ge} from a standard bench-top 20V DC power supply.

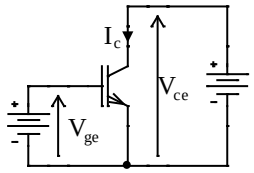


Figure 5.17: Circuit used to find the V_{ge} to I_c transfer characteristic of the IGBT

To obtain the characteristic up to the PVAE maximum current of 8A V_{ge} was set to the IGBT threshold voltage V_{th}, defined as the voltage at which I_c is 1mA, and adjusted at appropriate intervals with the resulting I_c recorded. The results of the tests are given in Figure 5.18.

In order to determine the effect of V_{ce} on the characteristic the test was repeated for V_{ce} values of 10V and 15V. Comparison of the V_{ce} = 10V and V_{ce} = 15V curves show that a higher V_{ce} increases the V_{ge} to I_c gain.

It can be observed in Figure 5.18 (b) that over a wide range of V_{ge} the logarithmic relation agrees with a straight line fit but exhibits a deviation from the exponential characteristic at higher V_{ge} for both values of V_{ce}. However for V_{ce} of 10V the deviation occurs as I_c increases above 5A, whereas for V_{ce} of 15V the deviation occurs earlier as I_c increases above 3A.

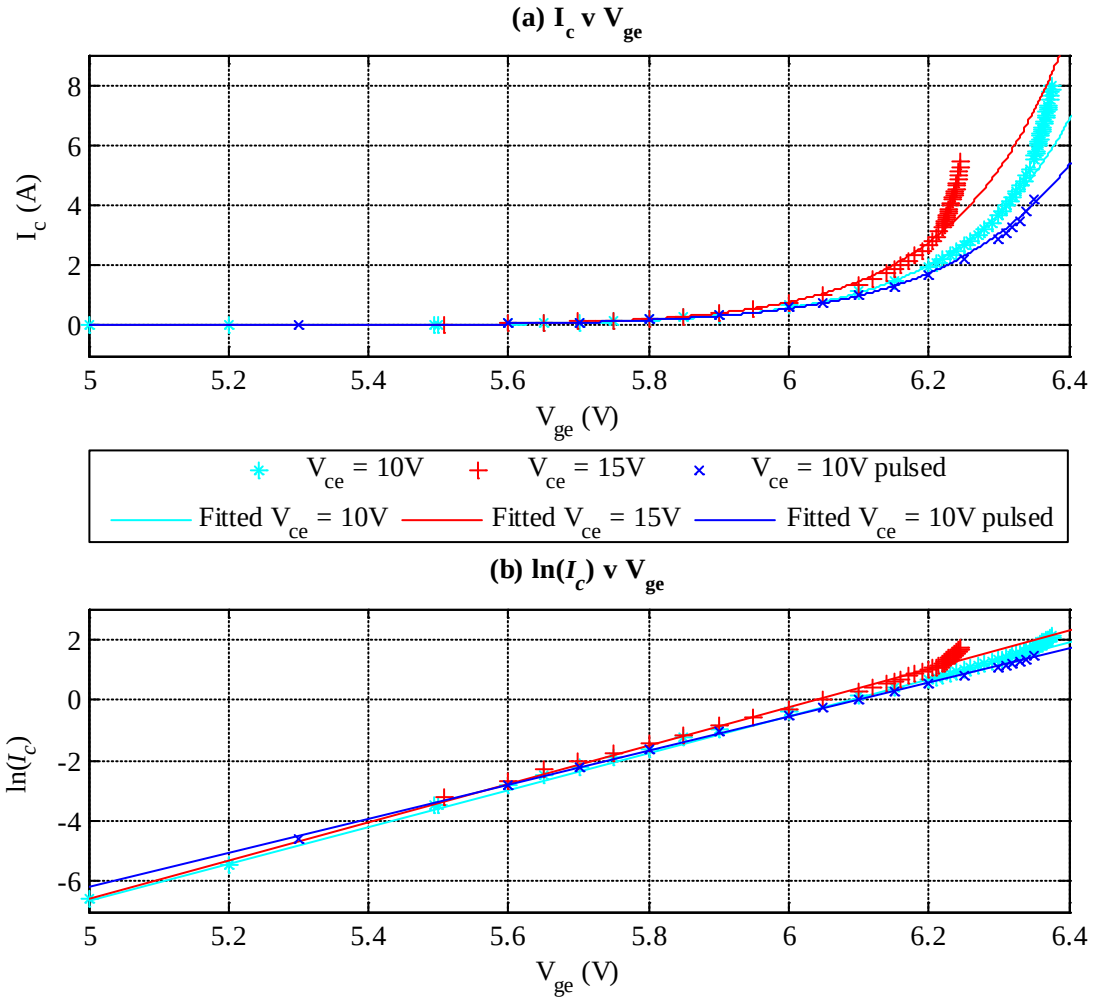


Figure 5.18: V_{ge} to I_c transfer characteristics of IGBT

The manner in which the increases in I_c occur with increased power dissipation in the IGBT implies that the V_{ge} to I_c relationship is also affected by the temperature. The increase in the V_{ge} to I_c gain agrees with the thermal properties of bipolar junction devices.

To minimise the effect of increased temperature due to the power dissipation in the IGBT the test was run again but in a 'pulsed' fashion. This involved setting V_{ge} with the collector-emitter supply turned off. The collector-emitter supply is then turned on just long enough to obtain a reading for I_c. The pulsed test was performed at a V_{ce} of 10V with the resulting data plotted in graph (b) showing a more constant slope than for continuous operation at the same V_{ce}.

The resulting transfer characteristics in graph (a) of Figure 5.18 show that the V_{ge} to I_c gain of the IGBT varies across the operating range in what appears to be an exponential trend. When plotted as the natural logarithm of I_c against V_{ge} in graph (b) a linear relation can be seen across a wide range confirming the exponential characteristic.

The dependence of I_c on V_{ge} is described by equation (5.1). The constants a and b are derived from a straight line approximation of the relationship between V_{ge} and $\ln(I_c)$ where a is the gain and b is the offset.

$$I_c = e^{(aV_{ge} + b)} \qquad \textbf{(5.1)}$$

Since the linear regulator system in Figure 5.15 forms a negative feedback control loop around the IGBT, with V_{ge} as the control variable and I_c as the output variable, the variation in gain due to the exponential relationship would complicate the controller design. A linearisation circuit has therefore been developed to minimise the variation in gain and approximate a linear relationship with the constant gain K_{lin}.

$$I_c = K_{lin}V_{control} \qquad \textbf{(5.2)}$$

By equating (5.1) and (5.2) an expression can be derived for the IGBT linearisation block in Figure 5.15 that relates V_{ge} to the control voltage $V_{control}$. To achieve a linear relationship between $V_{control}$ and I_c a logarithmic relationship is required between V_{ge} and $V_{control}$.

$$V_{ge} = \frac{\ln(K_{lin}V_{control}) - b}{a} \qquad \textbf{(5.3)}$$

The schematic of a linearisation circuit that realises equation (5.3) and minimises the variation in gain between $V_{control}$ and I_c is shown in Figure 5.19.

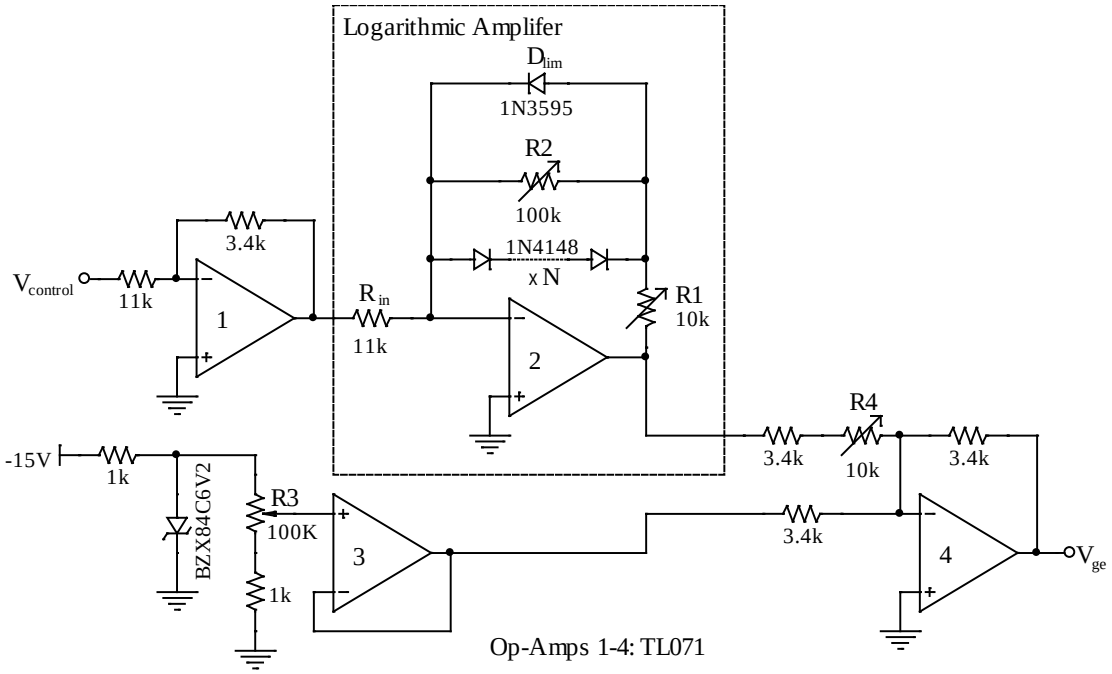


Figure 5.19: IGBT linearisation circuit

The linearisation circuit is based around a logarithmic amplifier that uses the logarithmic relationship between the voltage of a diode V_d and the diode current I_d. A series connection of N diodes is used to give an appreciable output voltage and reduce the sensitivity of the signal to noise pick-up. The V_d to $\ln(I_d)$ characteristic of the 1N4148 diodes used in the circuit was obtained experimentally and plotted in Figure 5.20 along with the line of best fit.

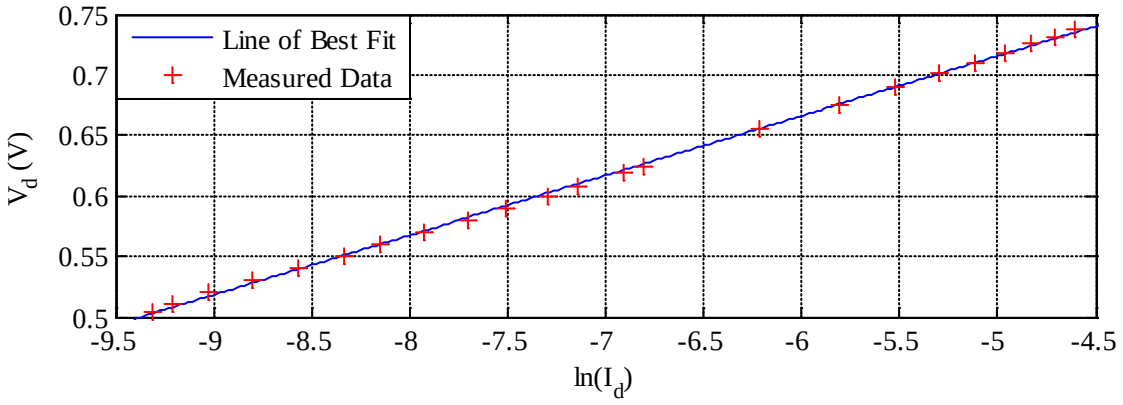


Figure 5.20: V_d against $\ln(I_d)$ characteristic of a 1N4148 diode

The linearisation circuit has been designed for a $V_{control}$ range of -12V to 0V. The diode D_{lim} in Figure 5.19 clamps the output of the logarithmic amplifier to just below 0V for positive values of $V_{control}$. To minimise its effect during normal operation the diode selected for D_{lim} was the low-leakage 1N3595. The variable resistors R1 and R2 allow tuning of the logarithmic amplifier characteristic to provide a close match to the IGBT characteristic.

The V_d to ln(I_d) relationship for a 1N4148 diode was derived from the line of best fit in Figure 5.20 with a_d and b_d being the gain and offset respectively.

$$V_{diode} = a_d \ln(I_{diode}) - b_d \quad \textbf{(5.4)}$$

Neglecting the tuning resistors R1 and R2, the dependence of V_{ge} to $V_{control}$ in the linearisation circuit can be derived. Since the gain of op-amp circuit 1 (K_1) and $V_{control}$ are both negative the natural logarithm is applied to a positive value. The output voltage V_3 of op-amp circuit 3 gives an offset to V_{ge} and is set using the potentiometer R3. In op-amp circuit 4 the gain K_4 is applied to the logarithm signal and can be varied using R4.

$$V_{ge} = -K_4 N \left(a_d \ln \left(\frac{K_1 V_{control}}{R_{in}} \right) - b_d \right) + V_3 \quad \textbf{(5.5)}$$

Expressions for tuning the linearisation circuit to the exponential characteristic of the IGBT can be derived by equating (5.3) and (5.5).

$$\frac{K_1}{R_{in}} = K_{lin} \quad \textbf{(5.6)}$$

$$K_4 N b_d + V_3 = -\frac{b}{a} \quad \textbf{(5.7)}$$

$$\frac{1}{K_4 N a_d} = -a \quad \textbf{(5.8)}$$

Equation (5.6) shows that the ratio of K_1 to R_{in} is important for matching the linearisation circuit to the IGBT. To calculate R_{in} using (5.6) a value for K_1 is required with K_1 determined by the limits of the op-amp 1 output voltage V_1 and $V_{control}$. Since K_1 is negative and V_1 positive $V_{control}$ must be negative and therefore the minimum value $V_{control}|_{min}$ is used.

$$K_1 = \frac{V_1|_{max}}{V_{control}|_{min}} \qquad \textbf{(5.9)}$$

Re-arranging and equating (5.7) and (5.8) eliminates the K_4N term and an expression for V_3 can be obtained that is entirely dependent on the constants of the IGBT and 1N4148 diode characteristics.

$$V_3 = \frac{b_d - ba_d}{aa_d} \qquad \textbf{(5.10)}$$

A value for N is selected to give an appropriate level for V_2 as described above. The chosen value for N is used in (5.8) to determine the gain K_4.

The linearisation circuit was tested by applying a triangular waveform to $V_{control}$ as shown in Figure 5.21.The range of $V_{control}$ is −12V to 0V, which corresponds to the I_c range of 8A to 0A. When the circuit was tested it was observed that oscillations in V_{ge} and I_c occurred around the IGBT threshold. These oscillations were removed through the use of a low pass RC filter at the IGBT gate.

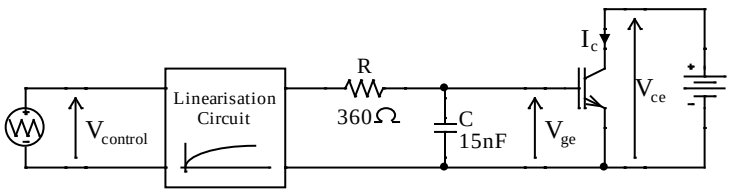


Figure 5.21: IGBT linearisation test circuit

The resulting waveform for I_c is shown in Figure 5.22. $V_{control}$ is applied at 0 seconds but the V_{ce} supply is switched on just before 1ms. The resulting successive peaks in I_c

increase in magnitude whilst maintaining a linear relationship. This is most likely due to the power dissipation in the IGBT leading to a rise in temperature and causing an increase in the V_{ge} to I_c gain, as was illustrated in Figure 5.18.

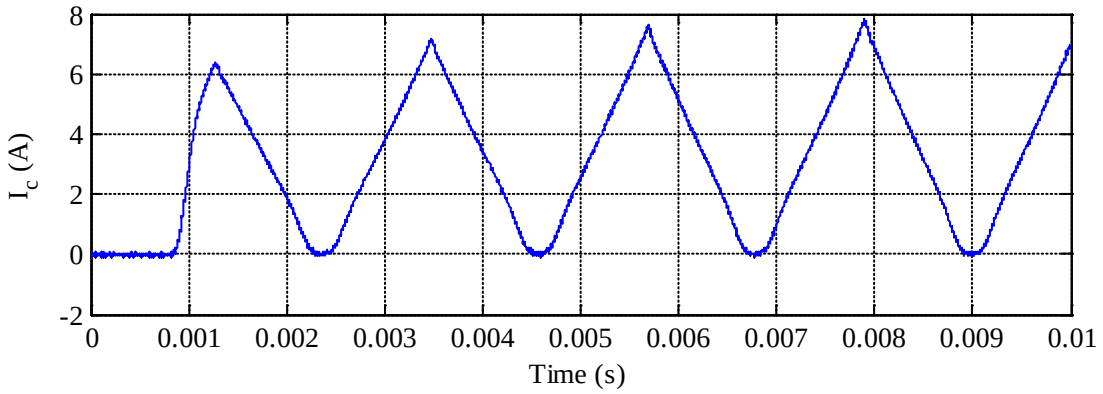


Figure 5.22: I_c waveform of linearised IGBT

The test was run again for the $V_{control}$ range of −10V to 0V to limit the power dissipation and temperature increase in the IGBT. The resulting $V_{control}$ to I_c characteristic has been plotted with the desired linear characteristic in Figure 5.23.

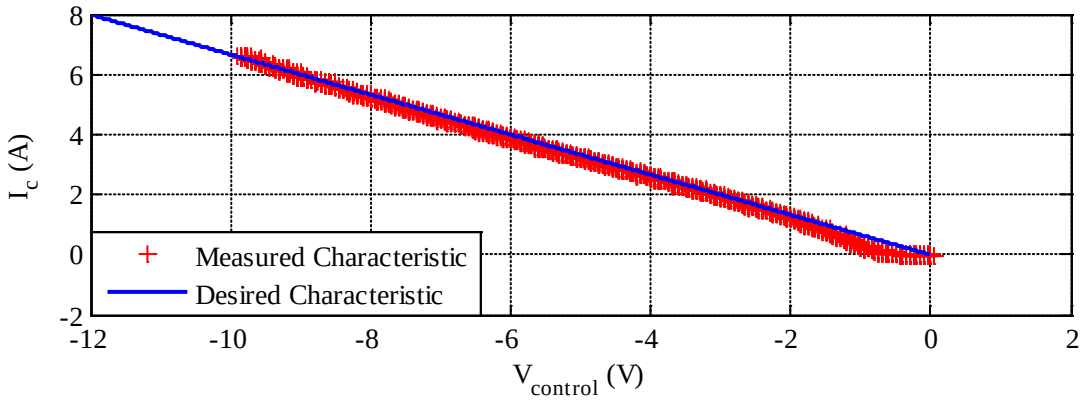


Figure 5.23: I_c to $V_{control}$ characteristic for the linearised IGBT

The results show that the linearisation circuit provides a near perfect linear characteristic with only a minor deviation at output currents of less than 1A. However, since the IGBT is to be used as part of a linear regulator in a PV emulator (PVE) the

output current will usually be at least 1A under normal steady state operating conditions and the slight non-linearity will have very little effect.

5.2.3 Closed-Loop Control of Linear Regulator

The previous subsection has described the linearisation of the control voltage $V_{control}$ to output current I_c open loop characteristic of the IGBT used in the linear regulator. It was noted that using the developed linearisation circuit produced a very good approximation to a linear relationship but a deviation in either temperature or V_{ce} would change the gain.

The dummy load of the regulator, shown in Figure 5.16, is designed to draw at most a few tens of milliamps at open circuit. Since the I-V characteristic of a PV module is very steep at open circuit, the IGBT collector current I_c will increase rapidly to a few amps with a deviation from open circuit and the PV emulator (PVE) output current I_{em} will be approximately the same as I_c. Therefore, I_c and I_{em} will be considered the same quantity from here on.

To keep the output current I_{em} or output voltage V_{em} of the regulator at a value set by the reference voltage $V_{ref,}$ despite variations in temperature and V_{ce}, a negative feedback proportional and integral (PI) controller is used as part of the regulator system, displayed again for reference in Figure 5.24.

Since controlling I_{em} or V_{em} to 0 would result in the IGBT switching off entirely, the ability to switch between controlling I_{em} and V_{em} has been added to allow the regulator to operate across the entire I-V characteristic in a PVE.

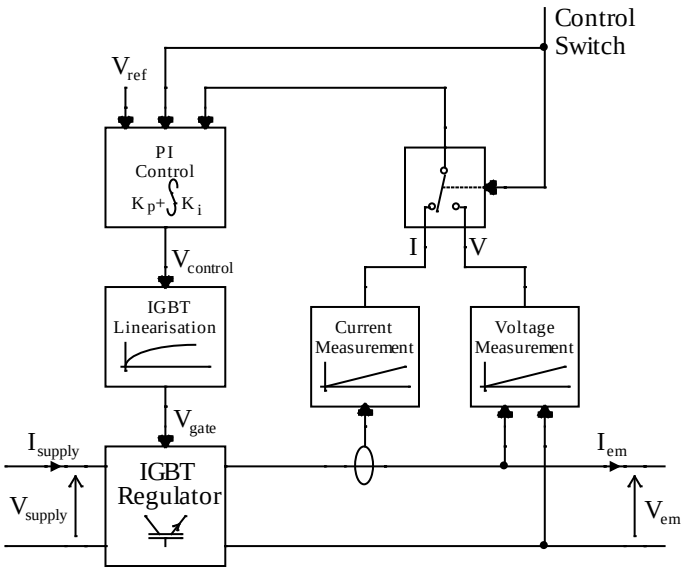


Figure 5.24: Diagram of IGBT regulator system for PVME

The regulator gains for the two control modes are different. Therefore, to optimise the PI gains for controlling V_{em} and I_{em} individually, the control switch also alters the gains of the integral amplifier (op-amp 2) and proportional amplifier (op-amp 3) in the PI control circuit of Figure 5.25. The gains are set for each control variable using the well-known Ziegler-Nichols method presented in [89] at the point of maximum open-loop gain (short circuit for I_{em} and open circuit for V_{em}) to ensure system stability.

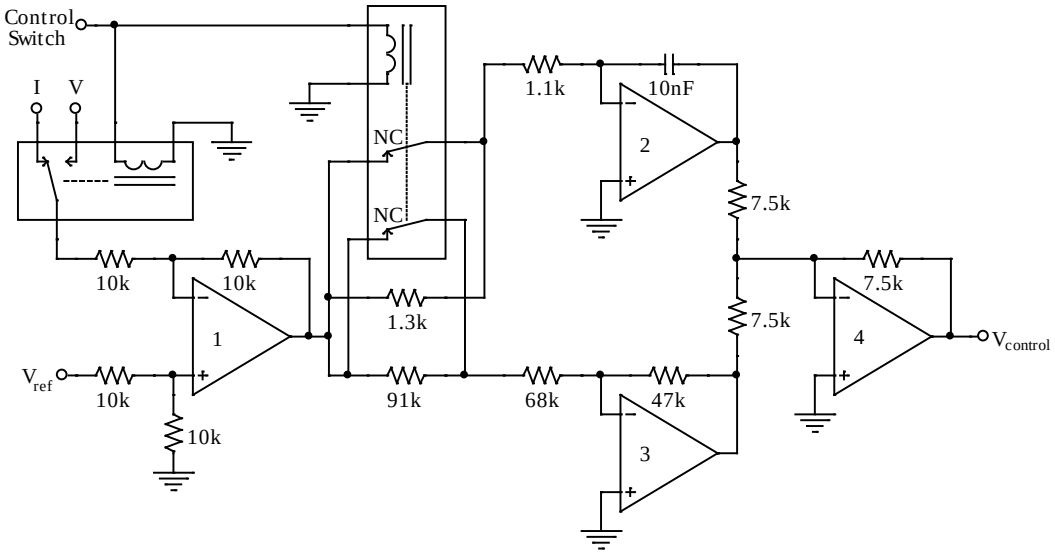


Figure 5.25: PI control circuit for linear regulator

The response of the regulator to a step change in reference is shown in Figure 5.26.

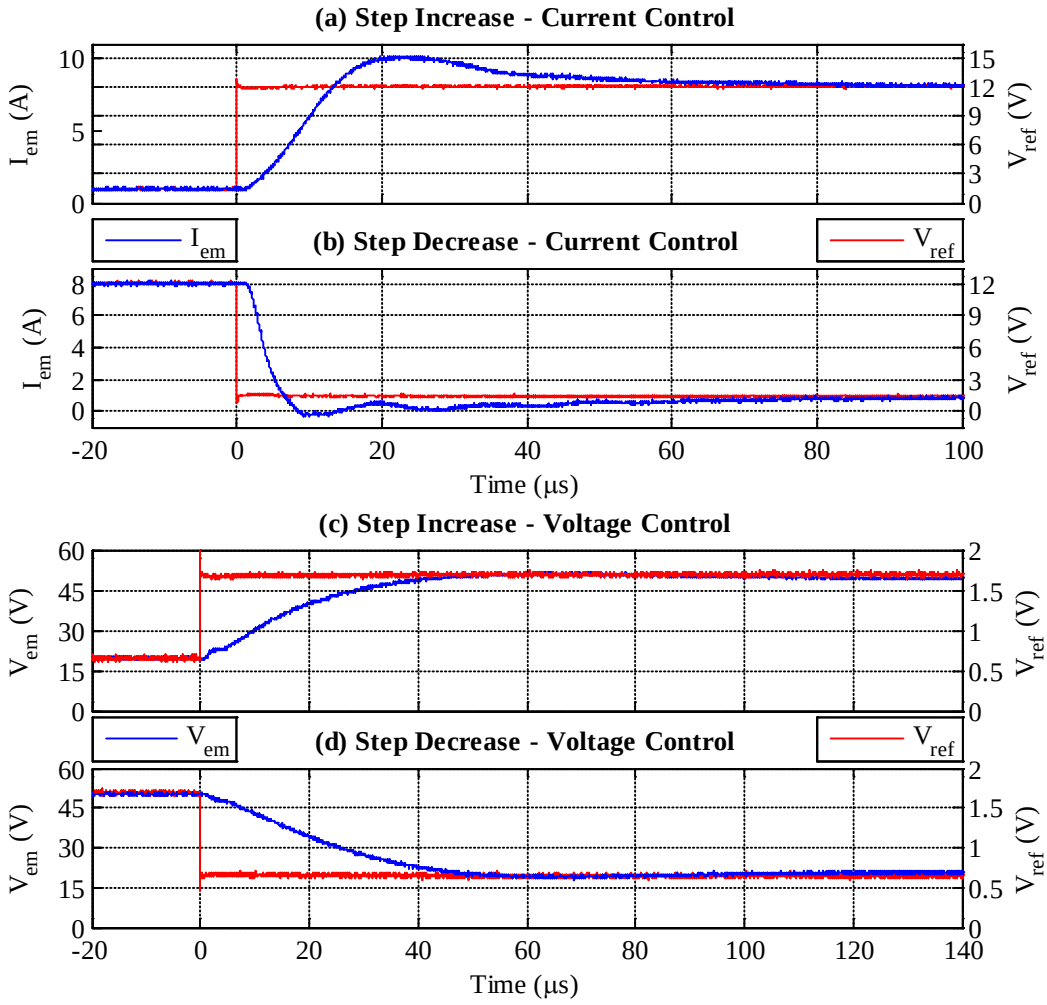


Figure 5.26: Response of linear regulator to change in reference

It can be seen that the closed-loop time response of the linear regulator system is less than 100µs for both I_{em} and V_{em} control. This response time is sufficiently fast to enable use of the regulator in a PVE for testing with fast maximum power point tracker (MPPT) algorithms, such as those used in DC power optimisers (DCPOs).

5.2.4 PVME Tests using an ACC

To test the use of the developed regulator in a PVE, the PVME system shown in Figure 5.27 was set up using the ACC from Chapter 4. The control switch (not shown) was set to keep the regulator in voltage control since the ACC provides a reference for V_{em} (computed from the measured I_{em}) to maintain the desired I-V characteristic.

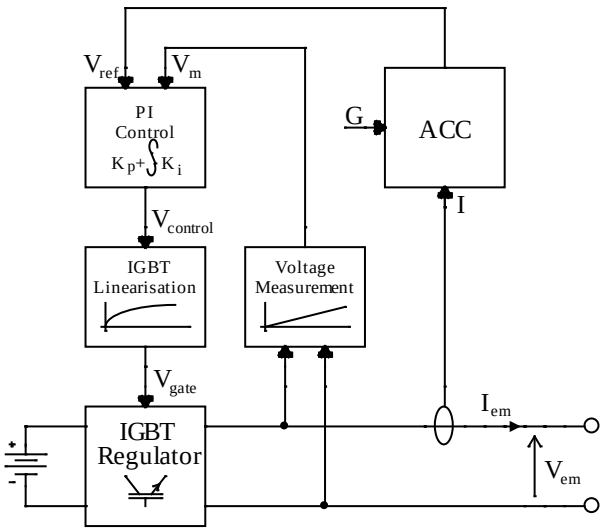


Figure 5.27: Setup of PVME combining linear regulator and ACC

Test a) A static load test was performed using the same setup as with the commercial power supply in Section 5.1, shown again in Figure 5.28. The PVME was configured to emulate a BP MSX60 PV module under STC.

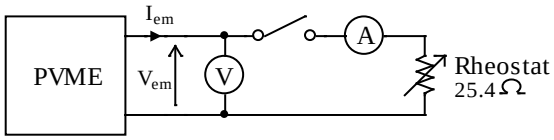


Figure 5.28: Static load test

The accuracy of the PVME static test was verified by comparing the main operating points of the results with the MSX60 values from the manufacturer's datasheet in Appendix B as displayed in Table 5.3. The results are seen to be within 2% of the manufacturer's data.

	P_{mpp} (W)	V_{mpp} (V)	I_{mpp} (A)	I_{sc} (A)	V_{oc} (V)
MSX60	60	16.8	3.56	3.87	21
PVME	60.7	17.1	3.55	-	21

Table 5.3: Comparison of electrical parameters

To show that the PVME is able to reproduce the I-V characteristic the results were plotted against the curve provided on the datasheet in the graph of Figure 5.29.

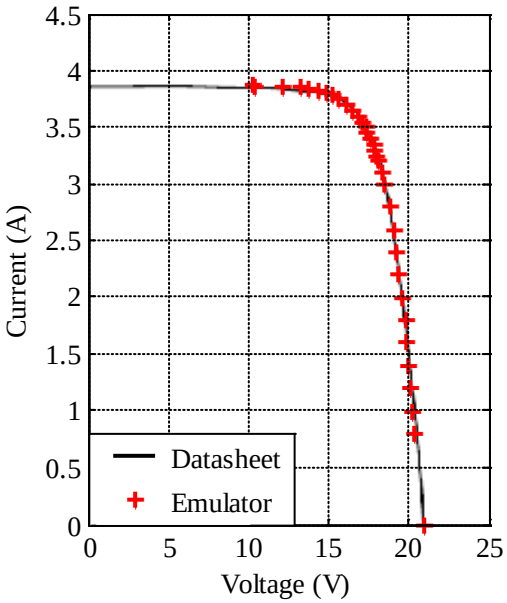


Figure 5.29: Comparison of PVME data with MSX60 datasheet I-V curve

The results verify that the PVME based on a linear regulator is able to reproduce a desired I-V curve that is at least as accurate as the commercial power supply when the PVME is connected to a static load.

Test b) As with Test a), the same setup used in Section 5.1 is used here as shown in Figure 5.30.

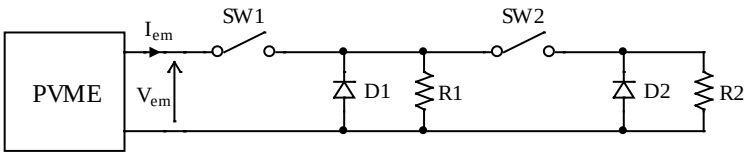


Figure 5.30: Dynamic passive load test

The resistor values used in the test are indicated in Table 5.4 and the response time is considered to be the time taken for the output voltage to settle within 0.1V

Initial Load	End Load
R1 = 4.9Ω	Open Circuit
Open Circuit	R1 = 4.9Ω
R1 = 4.9Ω	R1 // R2 = 4.82Ω
R1 // R2 = 4.82Ω	R1 = 4.9Ω

Table 5.4: Load values for PVME test of step response in load

Figure 5.31 displays the results of the load change between MPP and open circuit and vice-versa.

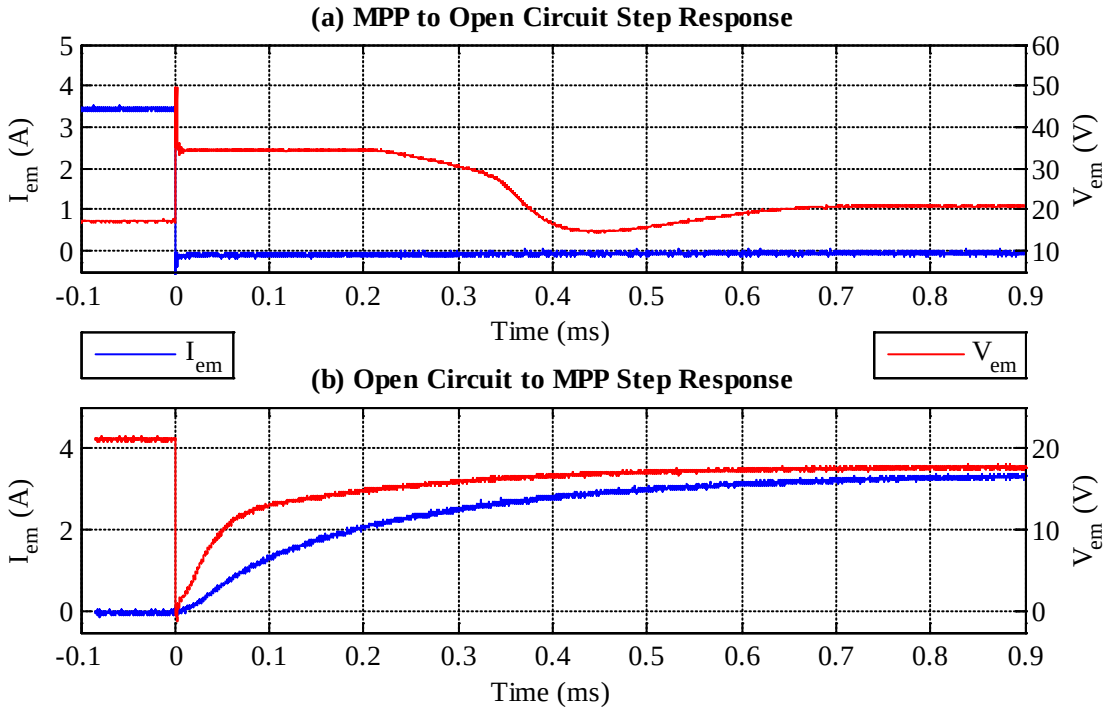


Figure 5.31: Time response of PVME to steps in load resistance

Due to the inductive nature of the wirewound rheostats used, a spike in the PVME output voltage can be seen as the current drops to 0A at the point of switching in graph (a). V_{em} then settles to a value just below the level of the DC voltage supply V_{supply} of the regulator. V_{em} remains at just under the supply voltage due to a delay in the changing of the IGBT resistance which will be much smaller than the open circuit dummy resistance whilst operating at MPP.

The delay in changing the IGBT resistance can be seen in the control signals of Figure 5.32, where even though V_{ref} jumps up to the required level, the integral part of the PI controller prevents $V_{control}$ from changing instantaneously. Initially, any change in IGBT resistance has little effect on V_{em} since the resistance of the IGBT is much smaller than the dummy resistance. This period (0-0.2ms) of constant V_{ref} and almost constant

V_{em} leads to a linear decrease in $V_{control}$. At 0.2ms the IGBT resistance becomes appreciable and V_{em} starts to decrease. There is a slight undershoot just before 0.4ms and V_{em} settles to within 0.1V of V_{oc} at around 0.65ms.

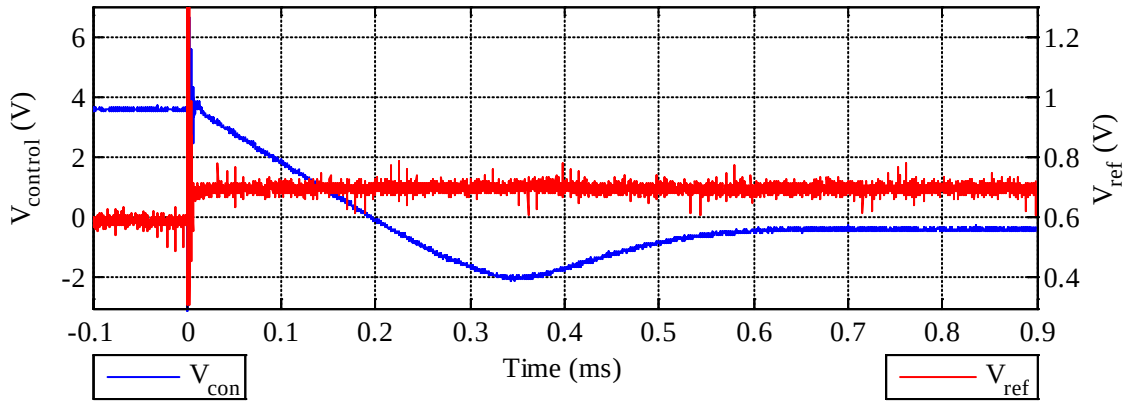


Figure 5.32: Control signals for MPP to open circuit step response

A step in V_{em} at the instance the load is switched is also seen in graph (b) of Figure 5.31 only this time V_{em} drops to 0V due to the IGBT resistance being much larger than the load. However, since the increase in I_{em} is opposed by the load inductance it will rise at a slower rate than V_{em} causing a slower response in V_{ref} from the ACC as seen in Figure 5.33. Due to the slower change in V_{ref} there is no overshoot and V_{em} settles to V_{mpp} in around 0.7ms.

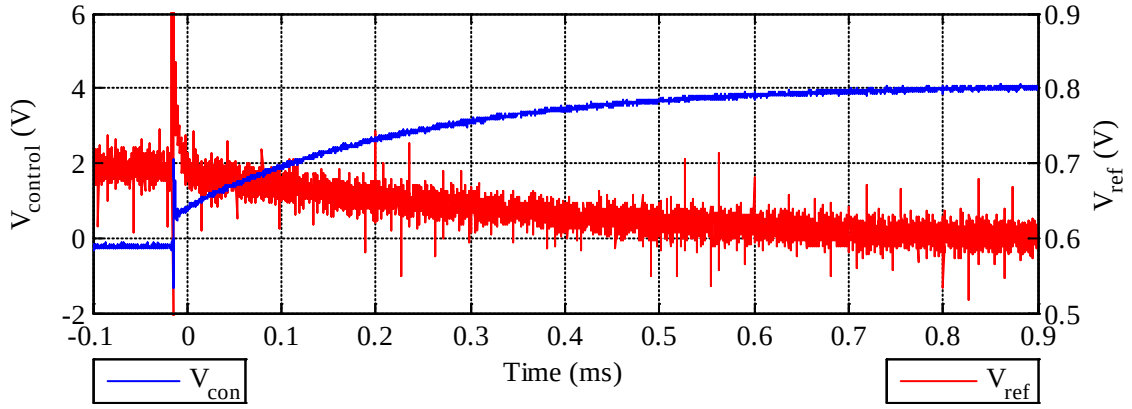


Figure 5.33: Control signals for open circuit to MPP step response

Since the MPPT algorithm of a PCD is unlikely to impose such a large step change in load the data obtained from a step response about the MPP is a better indicator of the

PVME's dynamic performance than a step change to and from open circuit. Therefore, to better evaluate the dynamic performance of the PVME, both a step decrease and a step increase in the load resistance about the MPP are recorded and plotted in Figure 5.34

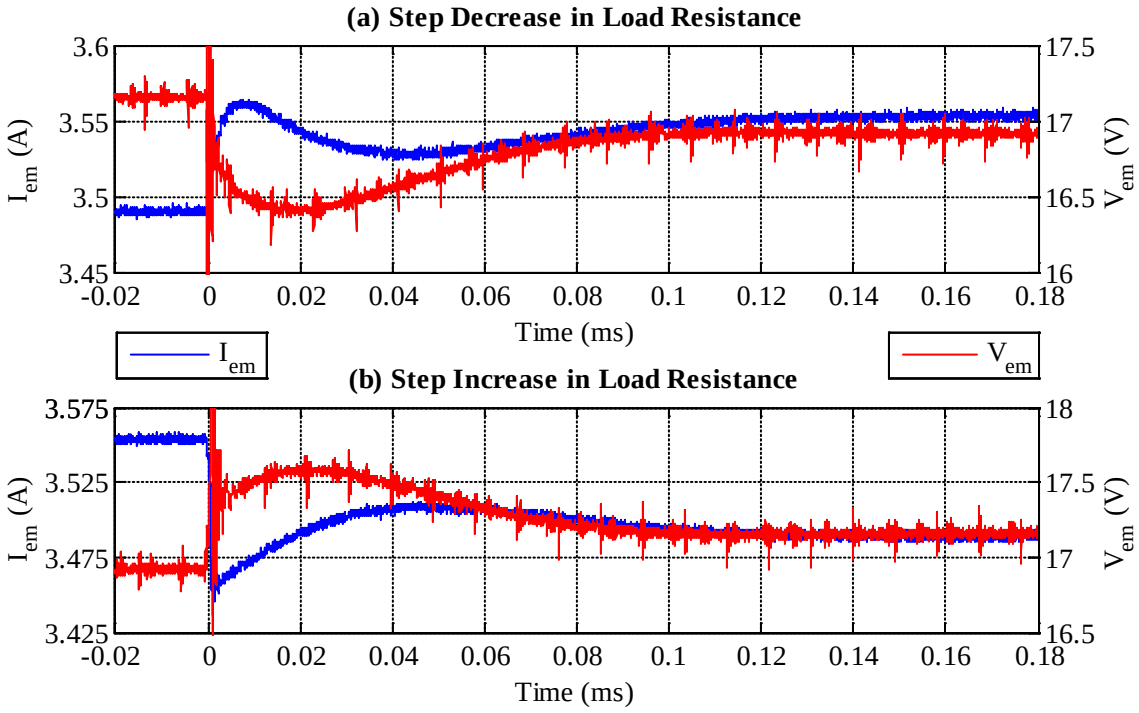


Figure 5.34: Time response of PVME to a load step around MPP

Both graph (a) and graph (b) show an almost identical voltage response to the step in load but in opposite directions with the decrease in load resistance causing a reduction in V_{em} and vice-versa. There is a large overshoot of V_{em} (approx. 3 times the step size) before the controller responds and V_{em} settles at around 0.1ms. Such a fast response should be adequate for all MPPT algorithms.

Test c) To test the stability of the PVME when operating with an active load using MPPT control the test system of Figure 5.35 was set up as described in Section 5.1 but with an output voltage V_{out} of 10V.

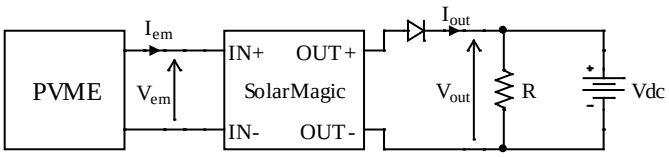


Figure 5.35: Setup for PVME test using dynamic active load

The resulting waveforms of the emulator output are given in Figure 5.36. A stable operation of the PVME with the SM connected is indicated by the pattern of V_{em} and I_{em} as they move back and forth across the MPP.

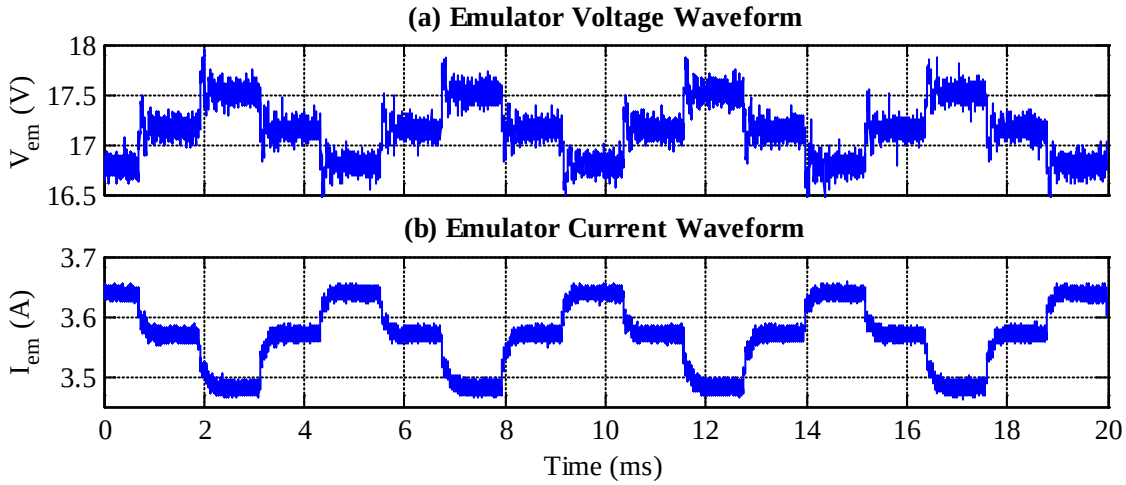


Figure 5.36: PVME waveforms for dynamic active load test

The stable MPPT is also illustrated in the plot of Figure 5.37 where the SM operating points are compared with the static I-V curve of the emulator. This shows 3 ‘clouds’ of SM data points around the MPP where each cloud is caused by the switching ripple and dynamic overshoot at each of the 3 MPPT operating levels seen in Figure 5.36.

It has been demonstrated that the PVME based on the developed linear regulator not only produces an accurate static I-V characteristic but, due to the fast action of the regulator, also maintains the accuracy even with a fast active MPPT load, such as an SM power optimiser.

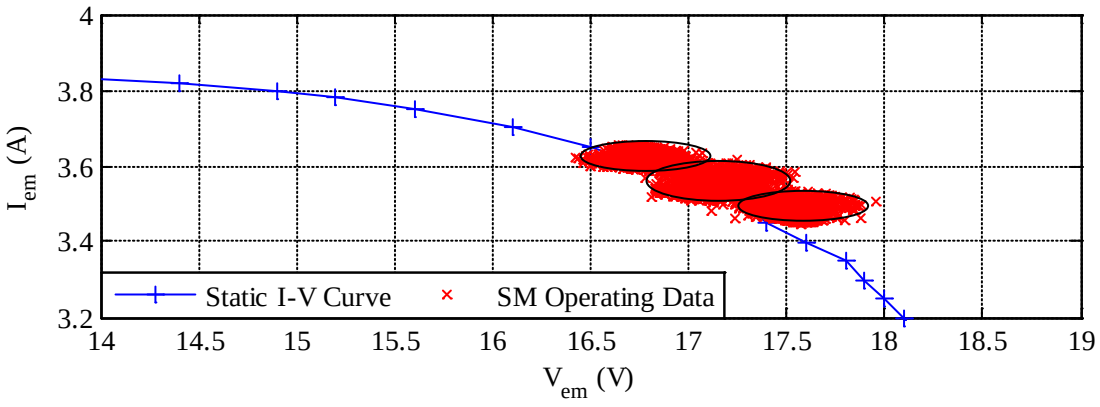


Figure 5.37: PVME static I-V curve with SM operating points

5.2.5 Switched-Mode DC Source Design

As mentioned at the start of this section, the higher voltage and current levels required in a PV array emulator (PVAE) mean that a constant DC voltage source is not suitable for use with a linear regulator as it would cause excessive power dissipation within the regulator that would damage the device used if not designed correctly. It is therefore necessary to use a switched-mode DC voltage source (SMDCVS) to reduce the DC source voltage level and limit the power dissipation in the linear regulator output stage.

To emulate a typical residential sized PV array the SMDCVS would be capable of supplying 3kW at a maximum 380V and 8A, powered from the $415V_{line}$ 3-phase mains. The setup would include a 3-phase isolation transformer that provides galvanic isolation for reasons of safety and also allows a modular emulator for arrays larger than 3kW by connecting together more than one PVAE. The transformer has independent secondary windings to allow series connection of single phase rectifiers thus increasing the maximum voltage achievable whilst providing redundancy of the rectifier components.

The SMDCVS converts the AC output of the transformer to the variable DC voltage required for the linear regulator. Two designs for the SMDCVS have been considered in this study. The two designs are a thyristor-controlled rectifier and a diode-rectifier/buck-converter combination.

a. Thyristor-controlled rectifier:

The thyristor-controlled rectifier consists of three full-bridge single-phase converters connected in series as shown in the block diagram of Figure 5.38.

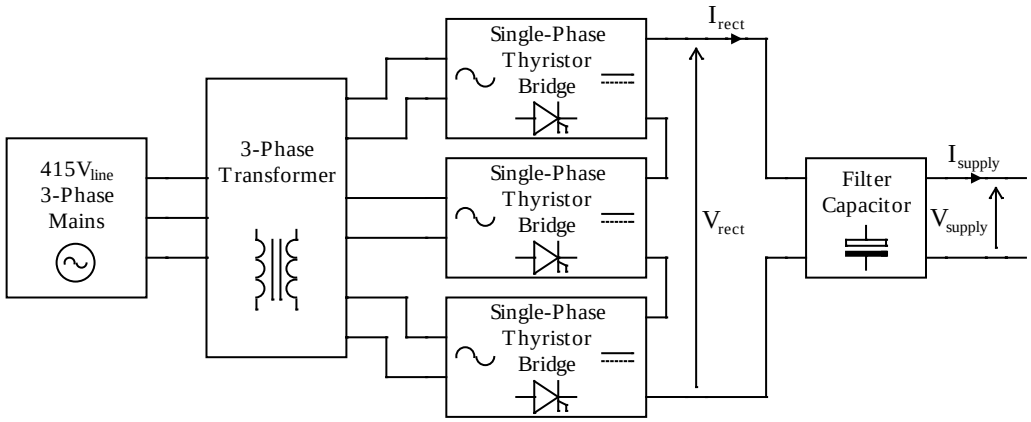


Figure 5.38: Block diagram of thyristor controlled rectifier system

The unfiltered DC output of the rectifier V_{rect} contains a periodic ripple with a fundamental frequency of 300Hz and amplitude dependent on the firing angle α as indicated by Figure 5.39.

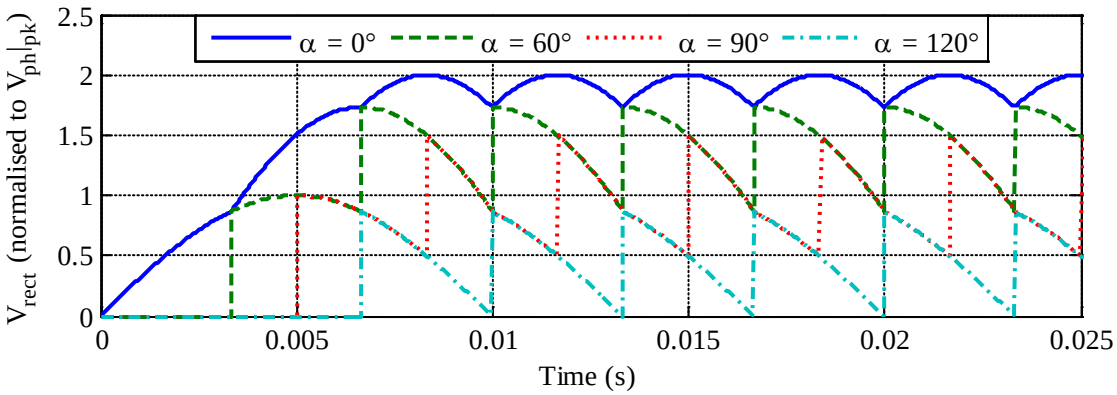


Figure 5.39: Unfiltered output voltage of thyristor rectifier

The peak to peak amplitude of the ripple mainly varies with the sine of α except for close to 0° where the ripple approaches the equivalent diode bridge value of approx. $0.25V_{ph}$ as shown in Figure 5.40.

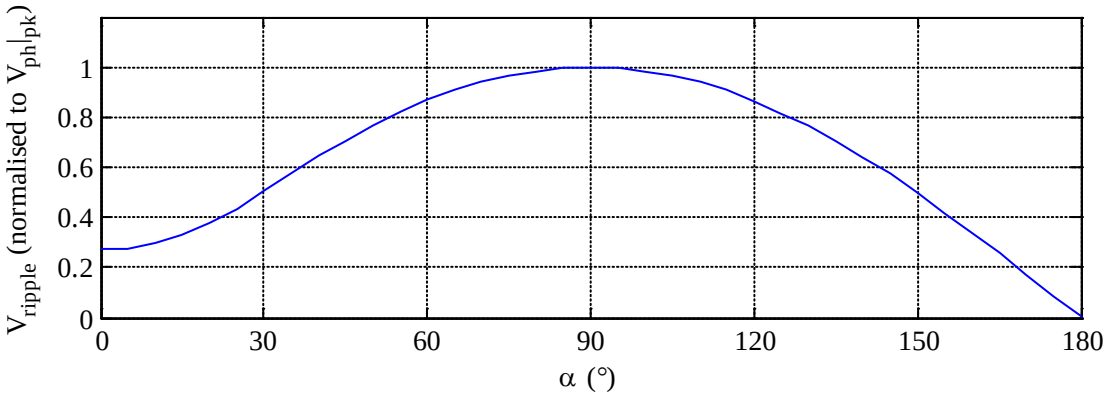


Figure 5.40: Variation of peak to peak voltage ripple with α

The worst-case peak to peak amplitude of the ripple occurs at 90° and is the same value as the peak amplitude of V_{ph}, which would be approx. 340V from a $415V_{line}$ 3-phase supply. Therefore, a filter capacitor is required to reduce the severity of the voltage variation with some ripple acceptable since the regulator is fast enough to remove it from the emulator output.

The filter capacitor is sized for the worst case ripple amplitude ($\alpha = 90°$, I_{em} = max.) so that the average IGBT voltage V_{igbt} is low enough to remain within the power rating at maximum current whilst maintaining at least the minimum IGBT voltage V_{op} for operation of the regulator across the entire ripple cycle as indicated by Figure 5.41.

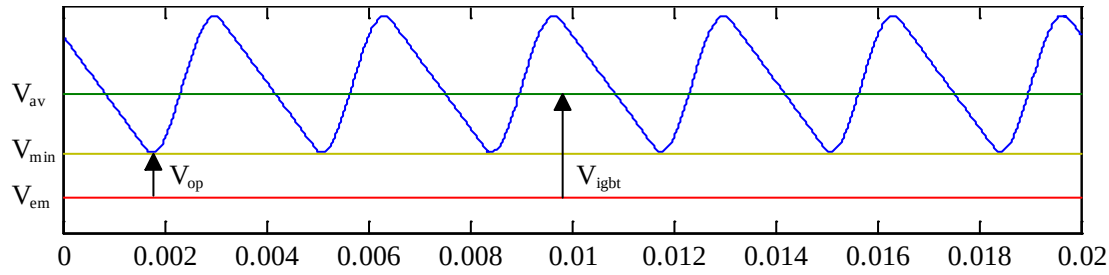


Figure 5.41: Limitations of ripple voltage

To minimise the ripple in V_{supply} the filter capacitor value can be increased. However, the greater the value of filter capacitance, the slower the response of the SMDCVS becomes. The filter capacitor size is therefore a trade-off between response speed and ripple reduction.

To achieve an increase in V_{supply} across the capacitor, a charging current needs to be fed from the mains through the transformer and thyristors. Since there is a low impedance path the current can become excessive and damage the thyristors. Some form of protection is required to limit the capacitor charging current, either in the form of a charging circuit or a method of controlling the thyristors to provide a gradual increase in V_{supply}. The speed at which V_{supply} can be increased is limited by the I^2t rating of the thyristors.

To decrease V_{supply}, charge needs to be removed from the capacitor. In the basic circuit the output current I_{supply} provides the means for extracting this charge but I_{supply} is load dependent and is limited to 8A. Therefore, the capacitor may take some time to discharge, especially under light loads.

To improve the speed of response for a reduction in V_{supply} a discharge circuit can be employed, such as the one presented in Figure 5.42. When there is a need to discharge the capacitor quickly the switch can be turned on to provide an extra path of low resistance. The resistor is required to protect the switch by dissipating the energy released from the capacitor.

The speed at which V_{supply} is reduced depends on the sum of I_{supply} and $I_{discharge}$. The switch current rating I_{sw} and the resistor value R are sized for the worst case where I_{supply} is 0A, V_{supply} is maximum and the desired voltage is 0V. In this case R is derived to provide a response time less than the specified maximum and I_{sw} is found from the maximum V_{supply} and the calculated value of R.

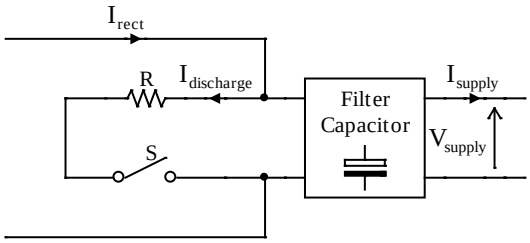


Figure 5.42: Discharge circuit for filter capacitor

b. Diode-rectifier/buck-converter

As mentioned above, the alternative method considered is the use of a diode rectifier – buck converter topology as illustrated in Figure 5.43. In this case the transformer and diode bridges are set up in a similar manner as the thyristor controlled rectifier to provide the unregulated DC voltage V_{rect} to the buck converter. This voltage is reduced by high frequency (>20kHz) chopping action of the buck-converter to provide V_{supply}.

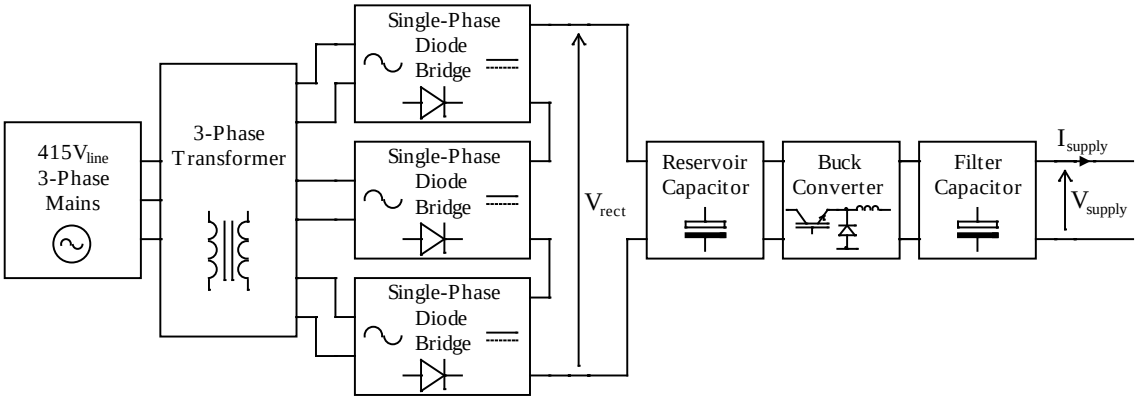


Figure 5.43: Block diagram of buck converter system

Since the buck converter operates at a much higher frequency than the thyristor controlled rectifier, less energy storage is required at its output. This means that a smaller filter capacitor can be used. The lower capacitance will improve the response speed of the SMDCVS, removing the need for special charging and dis-charging circuits. The buck-converter also requires only a single switch which, compared with 12 thyristors, simplifies the control and drive circuitry.

5.3 Summary of CDCPS design for a PVE

In this chapter an investigation into the suitability of controllable DC power supplies (CDCPSs) for use in a PV emulator (PVE) has been presented. The inept performance of commercial CDCPSs in terms of stability and speed of response has been demonstrated, and it was concluded that for PVE applications a specific CDCPS should be designed.

To create a PV module emulator (PVME) with a very fast response a linear regulator stage based on an IGBT was designed using a constant DC input source. Such a circuit was constructed for testing using the analogue computation circuit described in Chapter 4. The PVME system was shown to have a response speed of around 100µs, adequate for testing PV module level power conditioning devices (PCDs).

In view of the higher voltage levels involved in a PV array emulator (PVAE), minimisation of the power rating of the regulator IGBT prevents the use of a constant DC input voltage to the regulator. It has therefore been proposed that to control the voltage drop across the IGBT over the required voltage range of a PVAE a switched-mode DC voltage source (SMDCVS) is used as indicated by the block diagram in Figure 5.44.

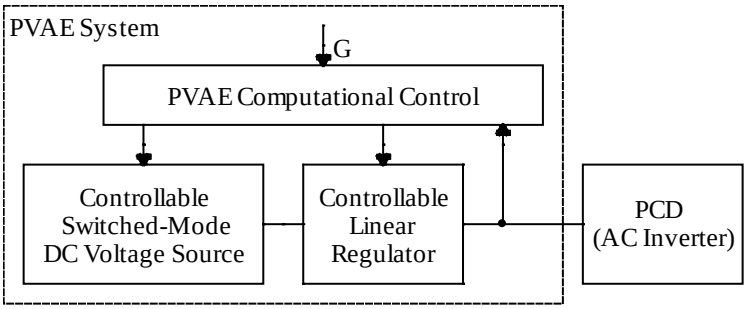


Figure 5.44: Block diagram of PVAE system including the SMDCVS

A comparison has been presented between two types of SMDCVSs suitable for this purpose: a thyristor-controlled rectifier and a diode-rectifier/buck-converter combination. It was concluded that the buck-converter would be preferable since the single switch reduces the complexity and the higher frequency switching facilitates a faster response time.

Chapter 6 Testing of Power Conditioning Devices

Experimental data from real PV system power conditioning devices (PCDs) has been obtained to check performance and verify the PV system simulation models developed in Chapter 7. Data was acquired for a SolarMagic (SM) DC power optimiser (DCPO), an SMA SB700 PV inverter and a combination of these devices as part of a PV system. The tests were designed to obtain an understanding of the PCDs' maximum power point tracker (MPPT) algorithm parameters and the dynamic characteristics of the PCDs' power electronics.

Tests were undertaken on a single PV module in a solar emulator, the PV emulators described in Chapters 4 and 5, and a 700W outdoor PV system. A description of the tests and an analysis of the results obtained are provided in this chapter.

6.1 Indoor Testing of an SM

To determine the operating characteristics of an SM DCPO, controlled indoor testing was needed. Whilst it is not possible to determine the exact MPPT algorithm used inside the SM since it is applied through the use of a microcontroller, an approximation can be derived from observing the input and output waveforms of the SM voltage, current and power. An assumption has been made of the system parameter varied by the algorithm as well as the timing and magnitude of the variation.

The values of the dynamic components in the SM's power electronics circuit have also been estimated by looking at the waveforms over a shorter time period. The component values are then adjusted so that the overall dynamic response of the model is the same as for the real system. The waveforms are obtained from tests with a real PV module in a solar emulator and, to extend the range of testing, a PV module emulator as well. These tests are presented in this section.

6.1.1 SM Testing with a Solar Emulator

The solar emulator described in [90], and shown in Figure 6.1, is a device that can be controlled to emulate the irradiance of the sun. It consists of an array of halogen bulbs, supplied by a DC power supply, inside a mirror lined box with cooling fans to prevent excessive temperatures. At the bottom of the box there is space to insert a PV module for testing.

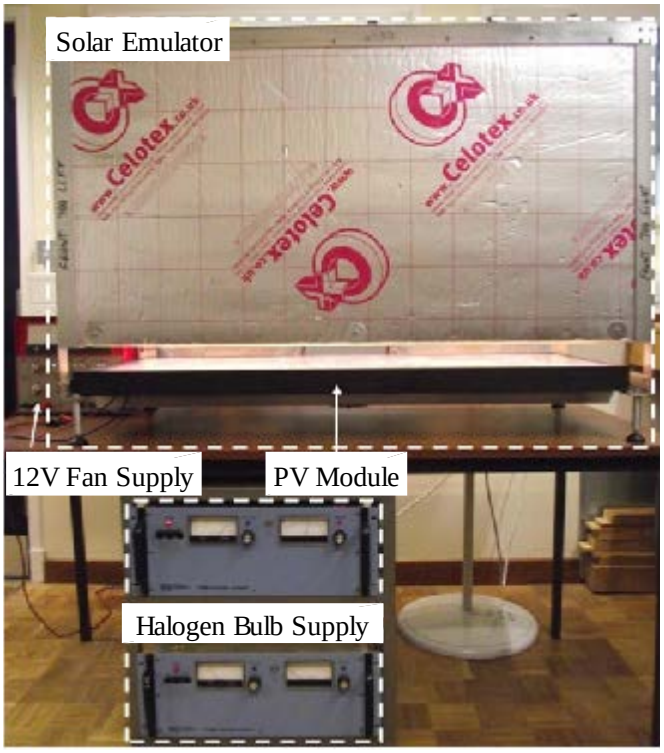


Figure 6.1: Solar emulator setup

A BP MSX 60 PV module was used during testing with the solar emulator. The electrical parameters, taken from the MSX 60 datasheet in Appendix B, are displayed in Table 6.1.

P_{mpp} (W)	V_{mpp} (V)	I_{mpp} (A)	I_{sc} (A)	V_{oc} (V)	K_{Voc} (mV/°C)	K_{Isc} (%/°C)	K_P (%/°C)
60	16.8	3.56	3.87	21	-80 ±10	0.065 ±0.015	-0.5 ±0.05

Table 6.1: Electrical parameters of MSX 60 PV module at 1kWm^{-2} and 25°C

Initial tests were run to find the characteristic curves of the PV module at 3 different levels of irradiance (G) and determine a suitable level for testing with the SM. For reference, the electrical operating limits of the SM taken from the datasheet in Appendix B are given in Table 6.2.

Min V_{mpp} (V)	Max V_{mpp} (V)	Max I_{mpp} (A)	Min P_{mpp} (W)	Max P_{mpp} (W)	Max V_{oc} (V)	Max V_{out} (V)	Max I_{out} (A)
15	40	8.5	5	230	50	43	8.5

Table 6.2: Electrical limits for the SM

The output of the PV module is connected to a rheostat type variable resistor. The value of the resistor is chosen so that the main point of interest, the MPP, lies within its range. Irradiance levels are chosen to give an I_{sc} of 1A, 2.4A, and 3.8A to test across the effective operating range of the MSX 60. It is deemed that at levels lower than I_{SC} = 1A the maximum available power of the PV module is too low for meaningful testing of the SM.

Chapter 2 indicates that an increase in G results in a slight increase in V_{mpp}. The value of the required resistor is therefore selected for the case of I_{sc} = 1A as this is large enough for all 3 tests. A variable resistor of value 26Ω and current rating of 8A was used for testing. The results of the tests are displayed as graphs in Figure 6.2.

To better observe the effect of varying the module conditions the I-V curves in plot (a) have been normalised to the available I_{sc} and V_{oc} for each irradiance level and re-plotted in graph (b). It can be seen that the normalised plots do not overlap entirely, with a higher irradiance reducing the steepness of the curve between the MPP and open circuit.

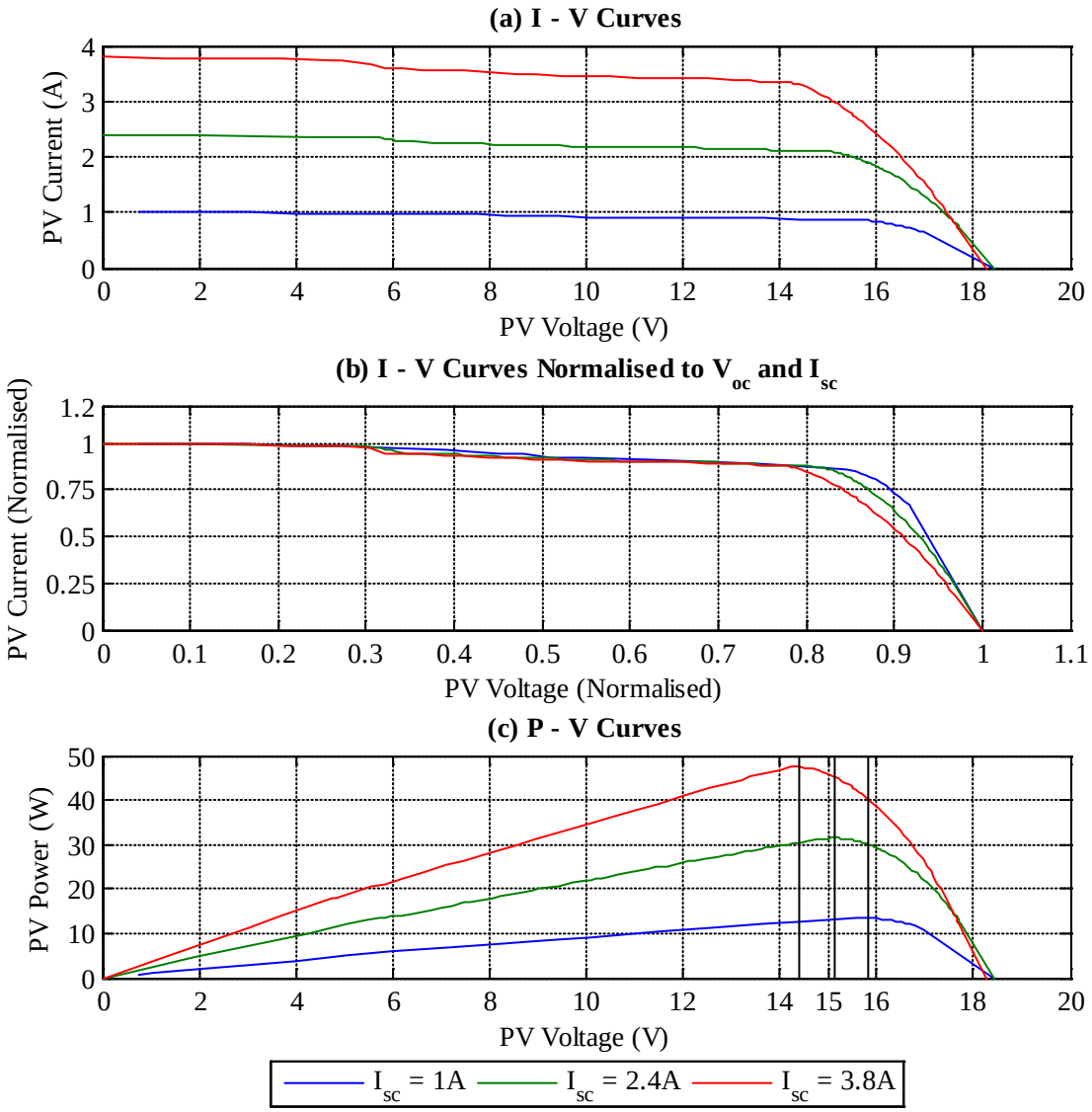


Figure 6.2: Characteristic curves of MSX 60 PV module using the solar emulator

Plots (a) and (b) demonstrate an unexpected deviation in the I – V curves between the MPP and short circuit with the deviation more pronounced at higher levels of irradiance. To investigate whether cell temperature plays a part in this behaviour, a further test was carried out. To reduce the time taken to measure the curve, thus decreasing the possibility of temperature variations during the test, an electronic load was used. To obtain a more accurate representation of the PV characteristics the electronic load was used in conjunction with a datalogging system to obtain a better resolution of current and voltage.

The configuration of the electronic load is illustrated in Figure 6.3 and consists of an IGBT placed across the output of the PV module. To measure the I – V curve the conductance of the IGBT is varied by applying a linear ramp gate signal to take the IGBT from saturation, with V_g above V_{on}, to the off state, with V_g below the threshold voltage V_{off}.

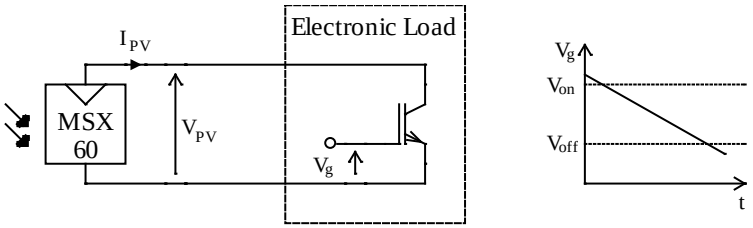


Figure 6.3: Electronic load test setup and applied gate voltage signal

To obtain the temperature variation across the PV module, as well as time, a measurement system was set up with temperature sensors applied to the PV cells indicated in Figure 6.4. Since the arrangement of cooling fans is symmetrical across the length of the PV module the temperature distribution is assumed to be symmetrical and measurements are taken from one half. The PV module has been modified to include 4 bypass diodes, with a diode connected across each string designated by a dashed line in Figure 6.4.

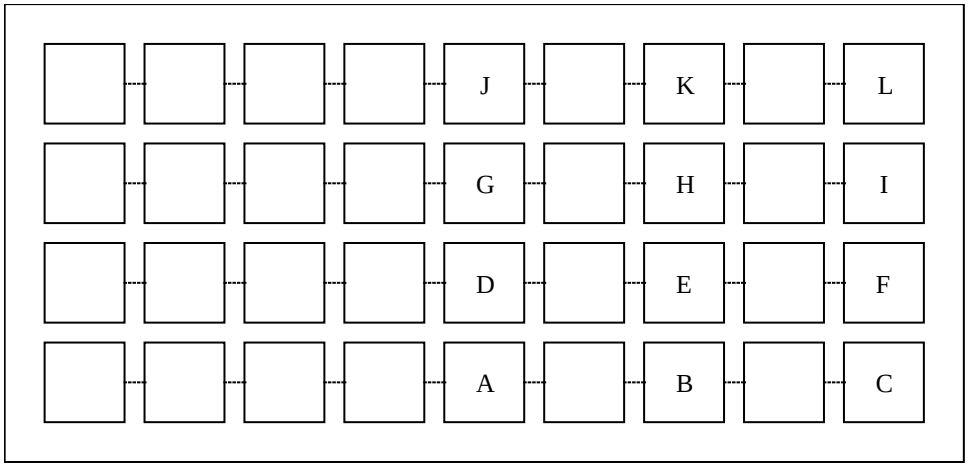


Figure 6.4: MSX 60 PV cell temperature sensor locations (top view)

The PV characteristics were measured with the solar emulator set to give a short circuit current of 3A, as shown in Figure 6.5. A step in the I – V characteristic can be seen around 6V. This implies that 2 of the bypass diode strings have a higher short circuit current than the other 2 strings for which the bypass diodes are in operation. The step could be due to a variation in the PV cell temperature during the measurement of the PV characteristic.

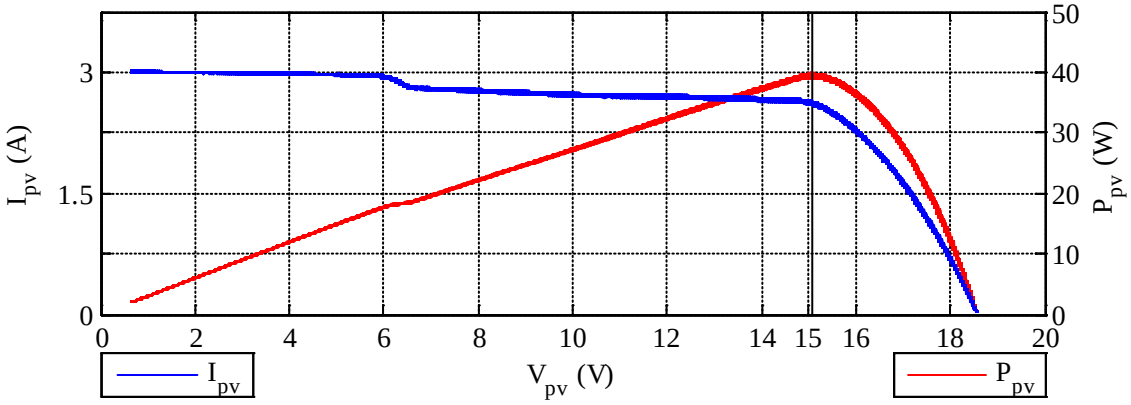


Figure 6.5: Characteristic curves of the MSX 60 using an electronic load

To determine whether the cell temperatures were constant during the test, the temperatures are plotted against the PV voltage in Figure 6.6. These plots show a steady cell temperature across the test range and so a change in temperature during the test can be discounted as a cause of the disturbance in the I – V curve.

However, there are variations in temperature between the PV cells that may have an effect on the characteristic. The I_{sc} of each bypass diode string will be limited by the cell with the worst case operating conditions, in this instance the lowest temperature. The average cell temperatures are displayed in Table 6.3 for analysis. The greatest difference in minimum cell temperature is approximately 6°C between strings 2 and 4.

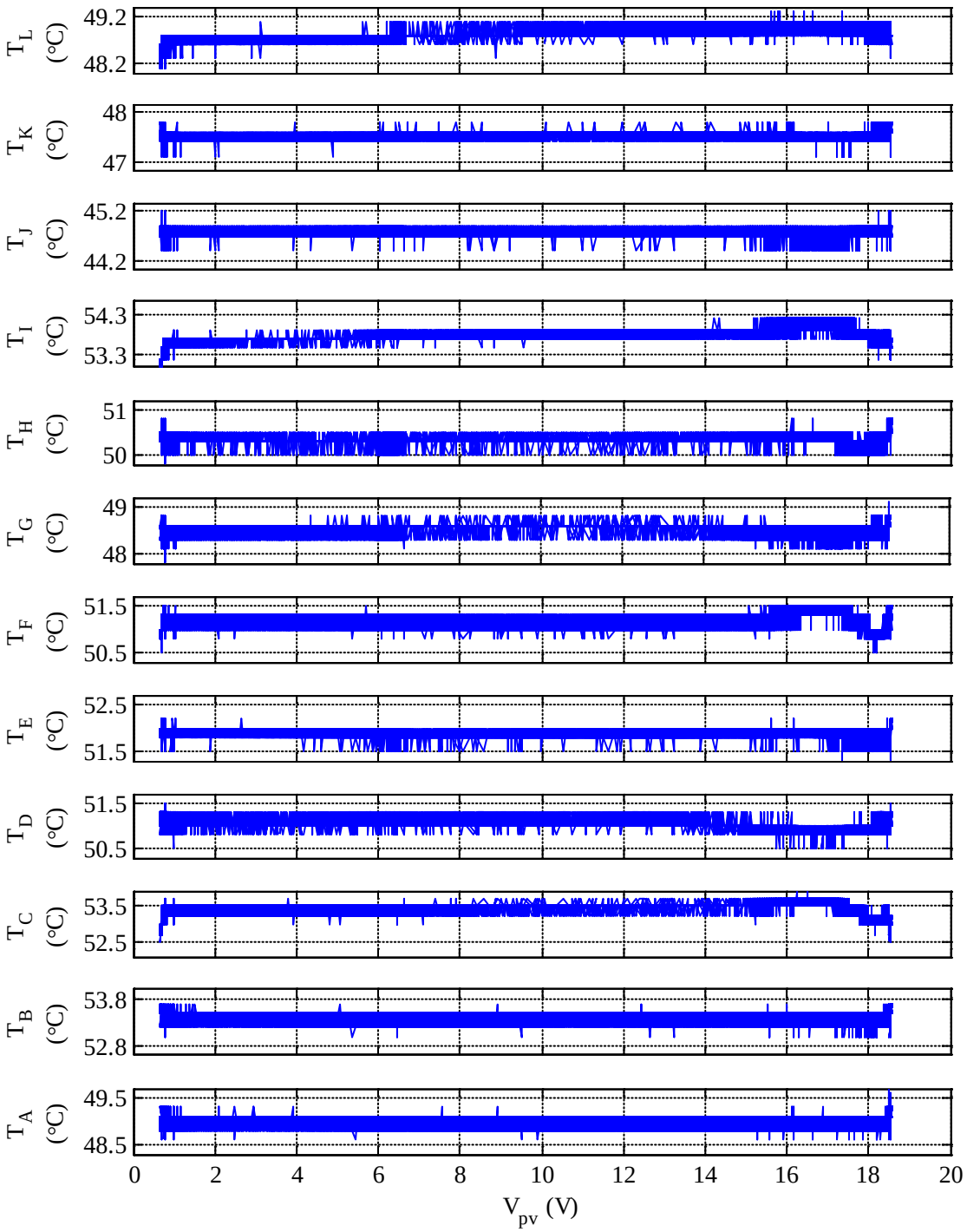


Figure 6.6: MSX 60 PV cell temperature variations during I – V characteristic test

String 1 A – B – C	String 2 D – E – F	String 3 G – H – I	String 4 J – K – L
49.068°C	**51.072°C**	**48.585°C**	**44.825°C**
53.422°C	51.876°C	50.437°C	47.599°C
53.175°C	51.176°C	53.606°C	48.781°C

Table 6.3: Average PV cell temperatures during I – V characteristic test

Table 6.1 gives the short circuit current temperature coefficient K_{Isc} of the MSX 60 as 0.065% per ^{o}C, which at an I_{sc} of 3A would result in a difference of around 12mA between strings 2 and 4. This difference appears to be too low to account for the step in the I – V curve. Also, as mentioned, the position of the step at 6V implies that 2 bypass strings have a higher I_{sc} whereas Table 6.3 shows strings 1 to 3 are within 1.5°C and string 4 is lower. The temperature variations are therefore assumed to have a minimal effect on the I – V curve and the main cause of the disturbance is likely to be a non-uniform irradiance pattern in the solar emulator.

Despite the cooling fans of the emulator, a rise in G results in an elevated operating temperature T for the PV cells. The increase in T counteracts any effect from G on V_{mpp} due to the PV module's negative temperature coefficients K_{Voc} and K_P. Figure 6.2 (c) and Table 6.4 shows that the temperature effect dominates since the highest solar emulator irradiance level has the lowest V_{mpp}.

I_{sc} (A)	I_{mpp} (A)	P_{mpp} (W)	V_{mpp} (V)	V_{oc} (V)
1	0.851	13.45	15.81	18.44
2.4	2.08	31.47	15.13	18.45
3.8	3.3	47.49	14.39	18.25

Table 6.4: Operating points of MSX 60 PV module using the solar emulator

To comply with the SM minimum operating voltage of 15V the tests are carried out at two irradiance levels that give I_{SC} = 1A and 1.25A respectively. These points are chosen to give an adequate margin of 0.5V between the minimum V_{mpp} of the SM and the V_{mpp} of the PV module to ensure normal operation of the SM. The operating points at these light levels are given in Table 6.5 with the I-V and P-V characteristics plotted in Figure 6.7.

I_{SC} (A)	I_{mpp} (A)	P_{mpp} (W)	V_{mpp} (V)	V_{OC} (V)
1	0.85	13.45	15.81	18.44
1.25	1.05	16.51	15.74	18.52

Table 6.5: MSX 60 PV module operating points at SM test levels

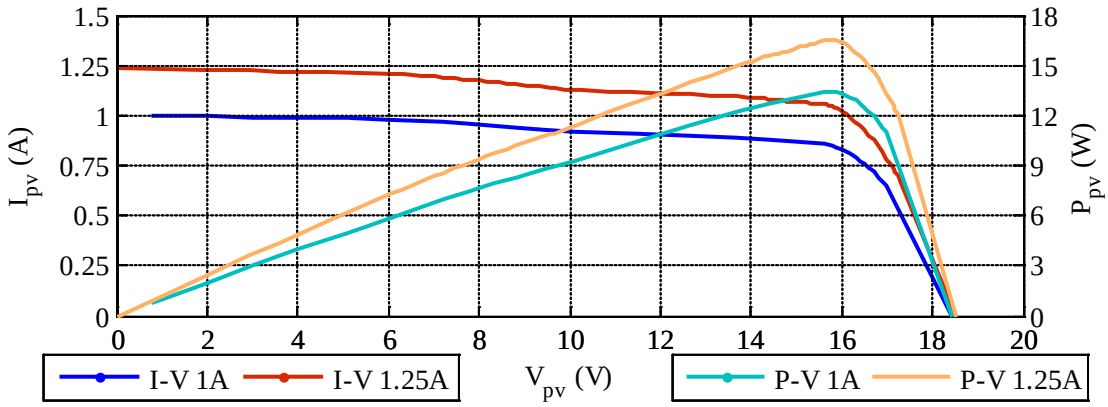


Figure 6.7: Characteristic curves of MSX 60 PV module at SM test levels

A diagram of the setup for testing the SM is shown in Figure 6.8. The controllable current source and bulb represent the solar emulator. The MSX 60 PV module in the emulator is connected to the input of the SM via a manually operated isolation switch. The output of the SM is then connected to the load.

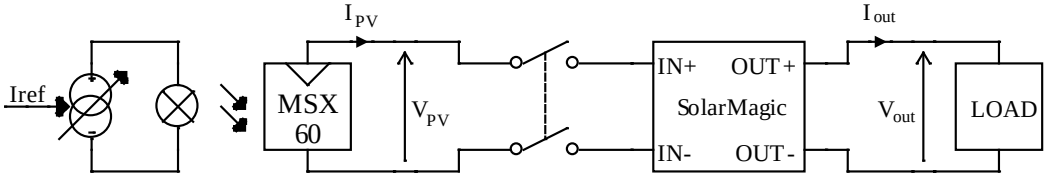


Figure 6.8: Setup for SM testing using a solar emulator

Different types of load are used to see how they affect the behaviour of the SM. These are either a resistor or constant voltage load. The constant voltage load is set up as described for the testing of the PV emulators in Chapter 5 and is shown again in Figure 6.9.

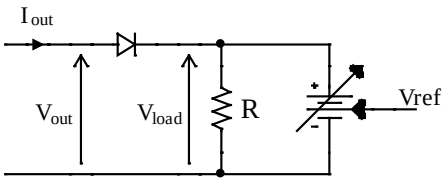


Figure 6.9: Constant voltage load

The power supply used is a Farnell AP60-50 and is set up to be voltage controlled through the application of an external reference signal. This allows a step change in the load voltage to be applied. To ensure that a high enough current is drawn at both voltage levels, the dissipating resistor R is selected for the lower voltage level.

Table 6.6 gives a summary of the calculated steady state test parameters for testing of the SM using the solar emulator. The tests are designed so that V_{out} is close to 0.5, 1 and 2 times the V_{mpp} of the MSX 60. Assuming 100% efficiency of the SM the corresponding I_{out} values are 2, 1, and 0.5 times the I_{mpp} respectively. To find V_{load} the voltage drop across the blocking diode is assumed to be 1V. The resistive load values are calculated from V_{out} and P_{mpp}.

Reference	Light Level	Load	V_{out}	Load Value	Start-Up
A	I_{sc} = 1A	Voltage	7.905V	6.9V (2.6Ω)	No
B	I_{sc} = 1A	Voltage	15.81V	14.8V (8Ω)	No
C	I_{sc} = 1A	Voltage	31.62V	30.6V (21.5Ω)	No
D	I_{sc} = 1.25A	Voltage	7.87V	6.8V (2.2Ω)	No
E	I_{sc} = 1.25A	Voltage	15.74V	14.7V (7.2Ω)	No
F	I_{sc} = 1.25A	Voltage	31.48V	30.5V (20Ω)	No
G	I_{sc} = 1.25A	Voltage	17.6V	16.6V (8 Ω)	Yes
H	I_{sc} = 1A	Resistive	7.905V	4.1Ω	No
I	I_{sc} = 1A	Resistive	15.81V	18.6Ω	No
J	I_{sc} = 1A	Resistive	31.62V	74.8Ω	No
K	I_{sc} = 1.25A	Resistive	7.87V	3.3Ω	No
L	I_{sc} = 1.25A	Resistive	15.74V	14Ω	No
M	I_{sc} = 1.25A	Resistive	31.48V	58Ω	No

Table 6.6: Calculated SM test conditions using the solar emulator

6.1.2 Results of Testing with the Solar Emulator

The previous subsection described the testing of an SM using a solar emulator as a controllable PV source. The relevant results of this testing are highlighted and analysed in this subsection.

As stated at the beginning of this chapter the tests on the SM are required to obtain an understanding of its operation and enable a computer simulation model to be constructed. To create an initial steady state model of the SM, three properties need to be established: the MPPT update period, the power electronics switching frequency (f_s) and the dynamic response of the power electronics circuit. The MPPT start-up process for the SM is also observed.

To determine whether the SM uses a fixed MPPT update the MSX 60 voltage waveforms of the constant V_{out} tests (A-F) are compared in Figure 6.10. The results confirm a constant MPPT update period of 1.2ms across the range of testing. This is likely to be the case for all areas of operation of the SM.

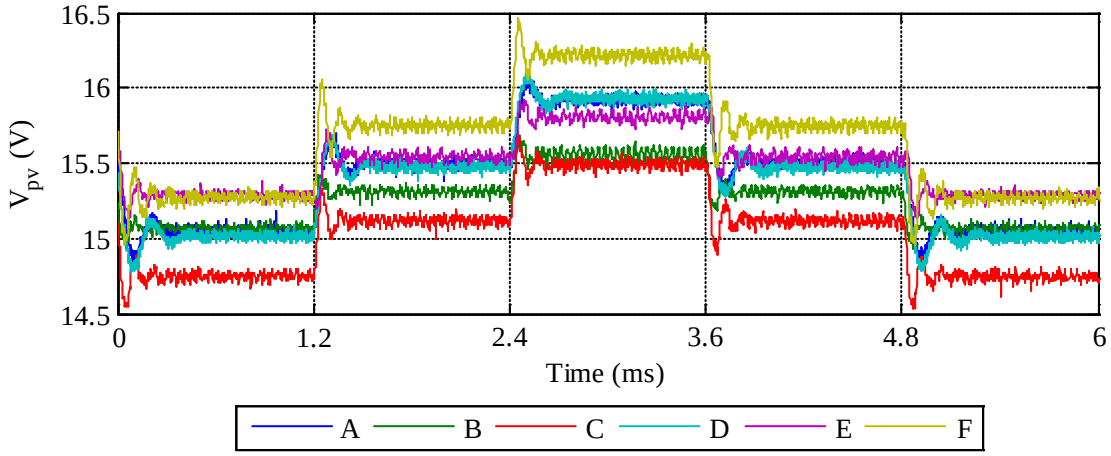


Figure 6.10: MSX 60 voltage waveforms for tests A-F in Table 6.6

To obtain f_s the Fast Fourier Transforms (FFTs) of tests H-J were computed and the results are displayed in Figure 6.11. The peak below 20kHz is likely to be due to ringing

caused by the energy storage components of the SM since switching of power electronics in the audio spectrum is generally avoided.

Test H shows a peak around 26.5kHz with a dominant peak at around 212.5kHz indicating the switches are operated at the higher frequency. However, the results for test I have a dominant peak at around 26.5kHz with no apparent 212.5kHz component. Test J has a noticeable peak at both frequencies, implying the switching of the power electronics uses an unknown modulation technique and f_s may be 26.5kHz or 212.5kHz. Since the simulation model developed in Chapter 7 does not include the switching action of the power electronics, the actual switching pattern is not relevant for this study and no further attempt is made to establish the applied modulation technique.

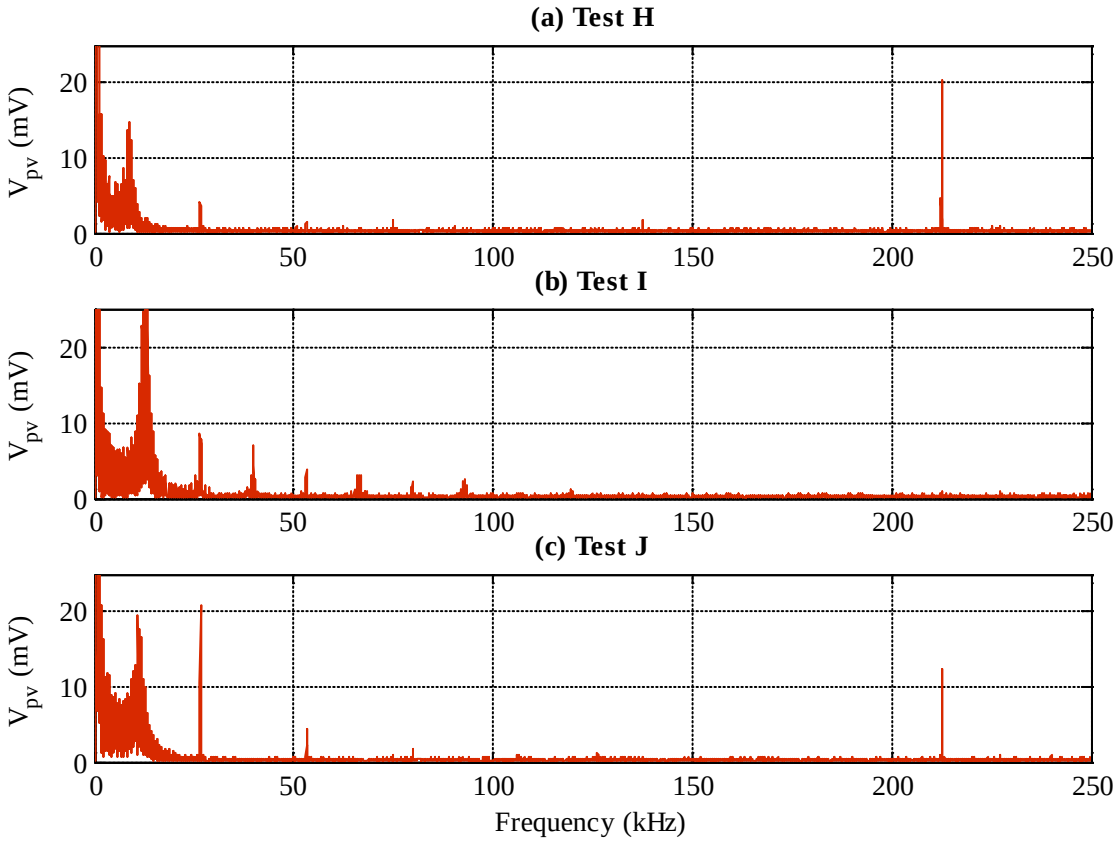


Figure 6.11: FFTs of V_{pv} to show switching frequency

To show the dynamic response of the energy storage components in the SM power electronics, the voltage waveforms are filtered in a similar manner to the results in

Chapter 5. The filtering removes the switching ripple and provides a clearer view of the underlying waveform. The filtered waveforms of test H, given in Figure 6.12, illustrate the ringing in V_{out} (also reflected in V_{in}) and the time constant for the change in $V_{pv.}$

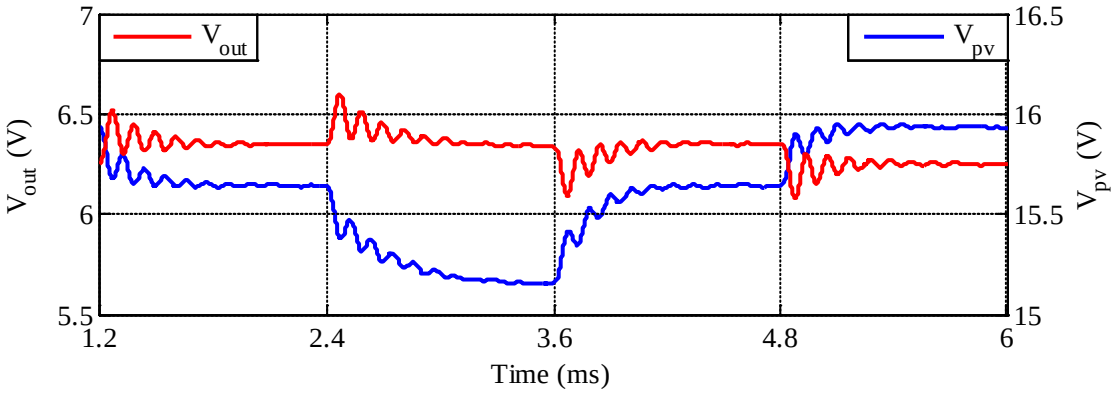


Figure 6.12: Filtered voltage waveforms for test H

Since the dynamic response may have an effect on the MPPT of the SM, the values of the energy storage components in the PSpice model of Chapter 7 are set to obtain the same dynamic response as displayed Figure 6.12. The waveforms show a ringing at approx. 9kHz, validated by the FFT of Figure 6.11 (a), and a first order response with a time constant around 0.3ms.

Test G was run to observe the start-up procedure of the SM; the resulting V_{pv} and P_{pv} waveforms are shown in Figure 6.13. The SM appears to start the MPPT from V_{oc} using a perturb and observe (P&O) algorithm to find the MPP.

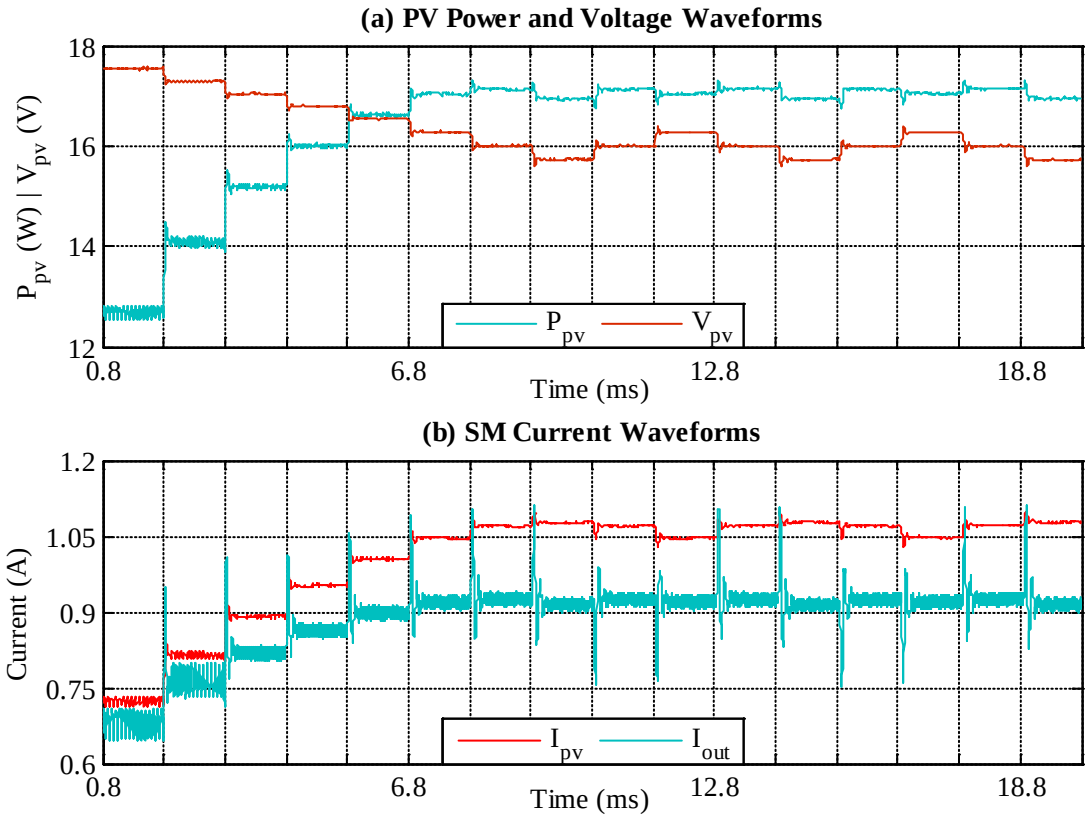


Figure 6.13: Start-up waveforms from test G

To summarise, the SM MPPT update period has been shown to be constant at 1.2ms and a complex switching modulation technique is implemented inside the SM with frequency components of 26.5kHz and 212.5kHz. To allow determination of values for the SM model components the dynamic response of the SM has been observed. The SM start-up procedure has been recorded and analysed for use in the model.

6.1.3 SM Testing using the PV Emulator

The previous subsections described the tests of an SM using a solar emulator to obtain the MPPT period, switching frequency, dynamic response and start-up characteristic for use in the SM model. However, the effects that varying SM operating parameters V_{mpp}, I_{mpp} and V_{out} have on the efficiency η and duty cycle perturbation size ΔD also need to be analysed to determine whether they should be accounted for in the model.

Due to the limited V_{mpp} range of the MSX60 PV module used in the solar emulator, an alternative means of testing is required. Therefore, the PV module emulator (PVME) described in Chapter 5 is used as a controllable PV source and the SM is again connected to a constant voltage load, as illustrated by Figure 6.14.

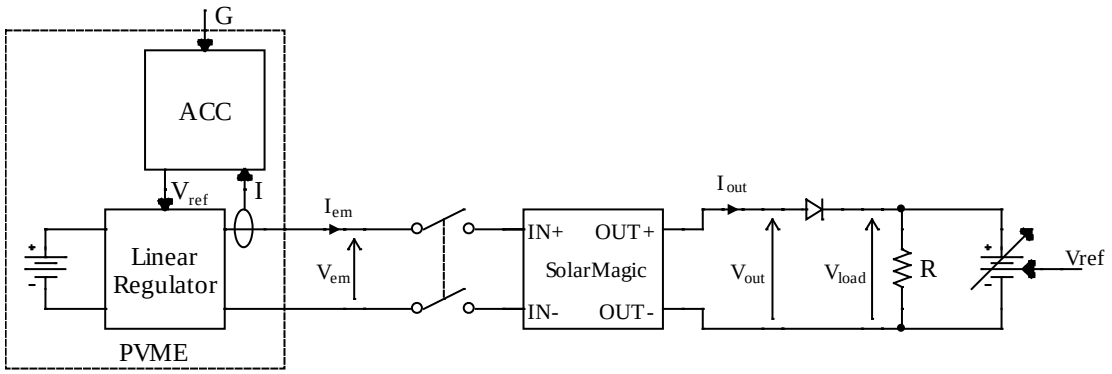


Figure 6.14: Setup for SM testing using a PV emulator

The PVME allows testing of the entire SM V_{mpp} range, although due to the limit of 180W power dissipation in the linear regulator section and the need for the DC supply to be 10V higher than V_{mpp}, the I_{mpp} at the SM maximum V_{mpp} of 40V is limited to 2.6A. Conversely, to achieve the maximum I_{mpp} of 8A for the PVME the V_{mpp} is limited to 15V.

To obtain the η and ΔD characteristics, tests designed to achieve a wide range of operation, whilst remaining within the limitations of the PVME, were carried out at the points summarised in Table 6.7

Test Reference	Constants	Variable	Range	Increment
A	I_{mpp} (3A) V_{out} (30V)	V_{mpp}	15V to 40V	5V
B	V_{mpp} (25V) V_{out} (30V)	I_{mpp}	1A to 6A	1A
C	I_{mpp} (3A) V_{mpp} (25V)	V_{out}	10V to 35V	5V

Table 6.7: Summary of SM tests using a PVME

The waveforms of the PV voltage V_{pv}, output voltage V_{out}, PV current I_{pv} and output current I_{out} were recorded using an oscilloscope and the data is used to determine η and ΔD. The SM efficiency is defined here as:

$$\eta = \frac{V_{out} I_{out}}{V_{pv} I_{pv}} \qquad \textbf{(6.1)}$$

As mentioned in Chapter 2, the SM2130 DCPO utilises a buck-boost topology. As such, the relation between duty cycle D and DC voltage gain of the power electronics was used to obtain D from the recorded data.

$$D = \frac{1}{1 + \frac{V_{pv}}{V_{out}}} \qquad \textbf{(6.2)}$$

6.1.4 Results of Testing with a PV Emulator

The previous subsection describes Tests A to C designed to investigate the dependency of SM efficiency η and duty cycle perturbation ΔD on the SM operating point for use in the modelling of a DMPPT system.

To establish a dependency for η the values calculated using (6.1) have been plotted in a separate graph for each test as shown in Figure 6.15.

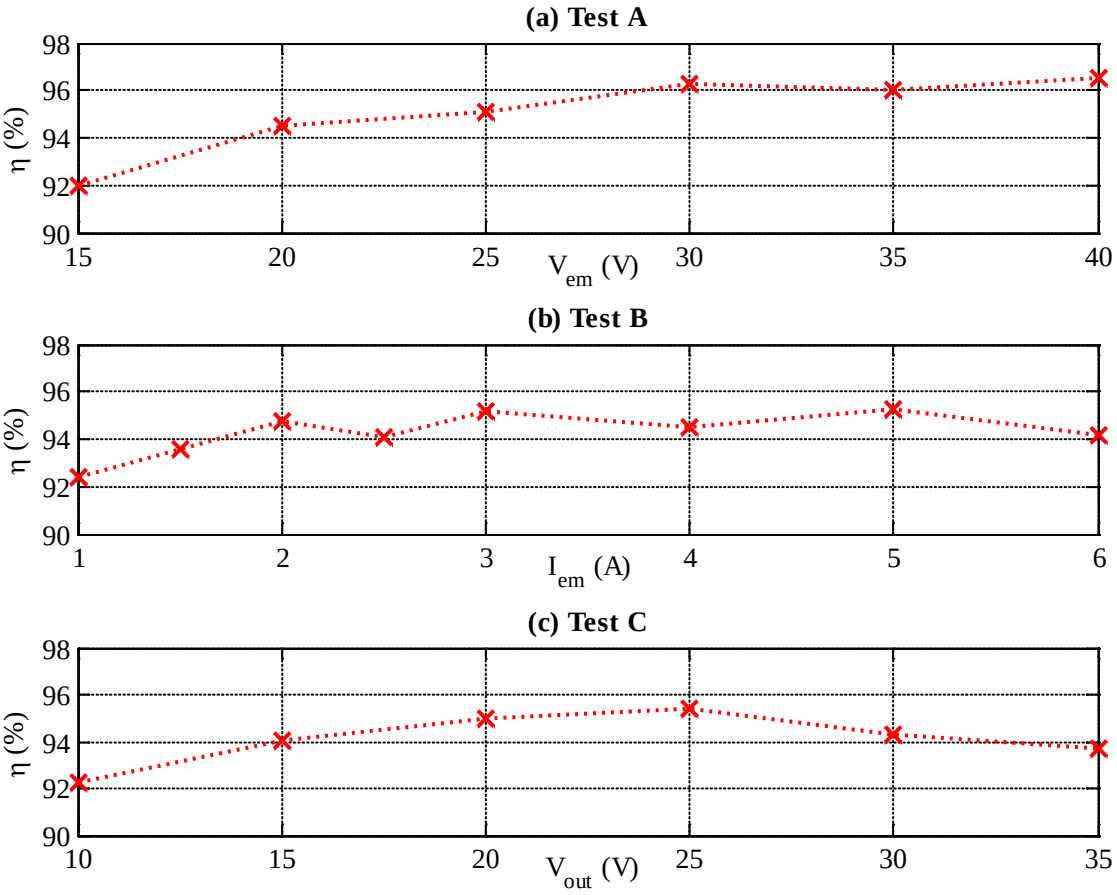


Figure 6.15: Dependency of η

It can be seen that for all test data η lies between 92% and 96% and depends on all three of the SM operating parameters tested. However, for the intended use of the model a constant value of 94% will suffice for η in the SM simulations.

To determine the characteristics of ΔD the duty cycle waveforms were obtained from the measured voltage waveforms (filtered to remove the unwanted switching ripple) using (6.2). The plots of D were evaluated to ascertain the ΔD value as an absolute percentage for each test point by taking the average of ΔD^{+} and ΔD^{-} indicated in Figure 6.16.

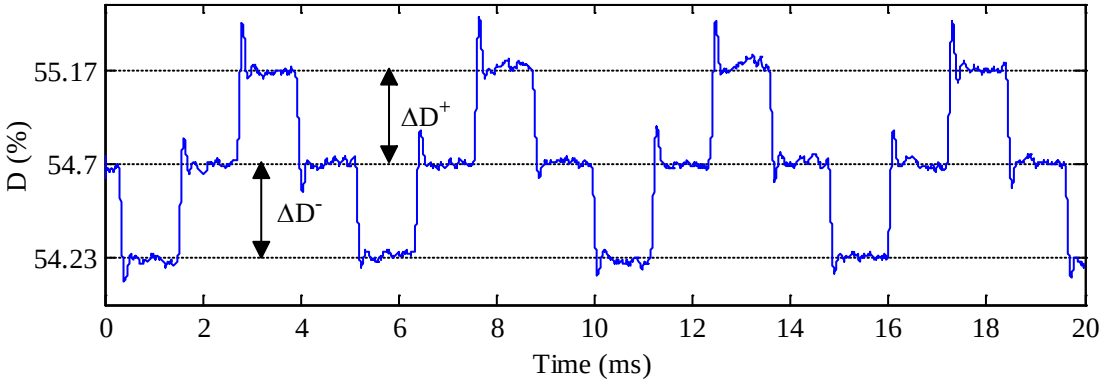


Figure 6.16: D waveform for Test C with V_{out} at 30V

For comparison, the absolute percentage values of ΔD for each test are plotted against D in the graph of Figure 6.17, where D is taken as the intermediate level (54.7% in Figure 6.16). It can be seen that all data points are close to 2 straight lines emanating from 48.7% duty cycle. To implement the variation of ΔD as part of the Simulink MPPT modelling a 3-point lookup table with linear interpolation and extrapolation is used. The extrapolation is limited by the operating range of D which is either restricted to a value of 66.67% (a reasonable value giving a voltage gain of 2 for the buck-boost topology) or by the maximum operating parameters of the SM.

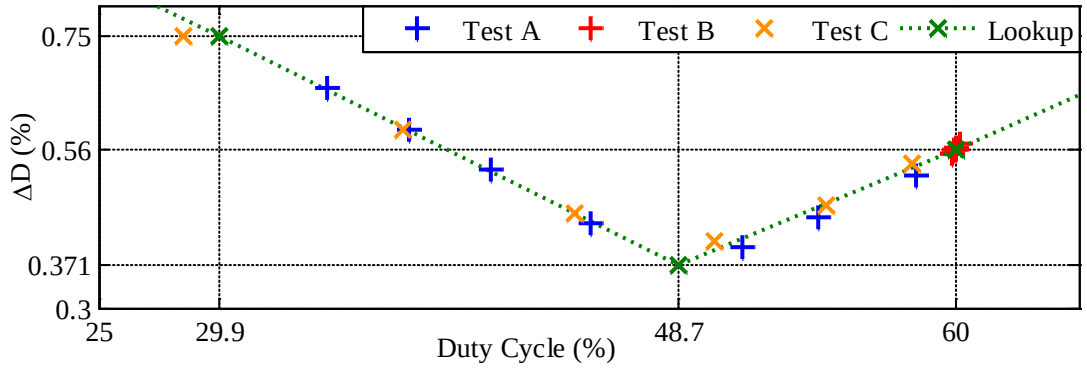


Figure 6.17: Variation of ΔD

In summary, the efficiency of the SM operating point was found to range from 92% to 96%. Since the variation in η is deemed to have a minor effect on the operation of the

SM, a constant value of 94% is used for η in the SM model. The relationship of ΔD to D was shown to be less complex and can be implemented as a piecewise linear lookup table in the model.

6.2 Outdoor Test Rig for Grid-Connected PV System

Experimental data on the operation of the inverter is required to develop a PSpice model. Also, observation of a real DMPPT system is useful to obtain data for comparison with the complete DMPPT system model as well as showing possible causes for negative interactions that require further investigation with the complete model.

An outdoor test rig was developed to acquire these sets of data. The design and testing of the outdoor rig, containing four BP7175S PV modules and an SMA SB700 inverter, are presented in this subsection.

6.2.1 Operation of the SB700

The SMA SB700 is a single-phase full-bridge inverter with an output transformer, as shown in Figure 6.18. The switching section of the inverter draws the current i_d, the sum of i_c and i_{in}, that contains a 2nd harmonic ripple current i_{d2} (where the fundamental is the mains frequency) as described in [91]. With the mains in the UK operated at 50Hz, the frequency of this ripple will be 100Hz.

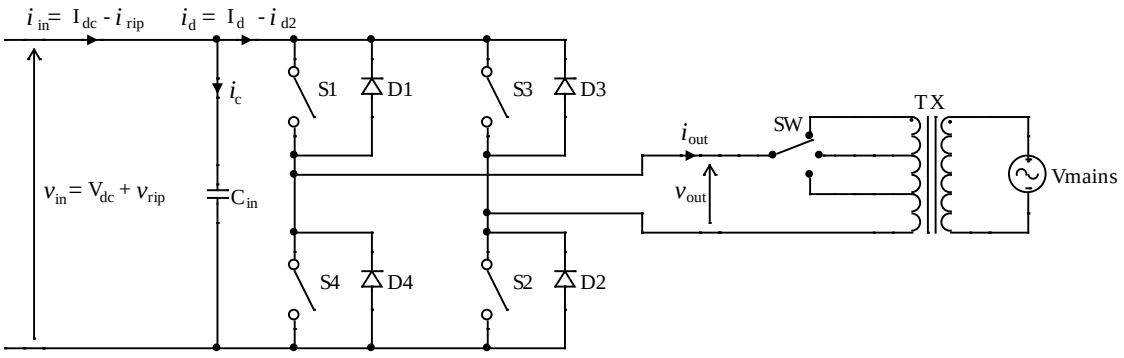


Figure 6.18: SB700 diagram

The amplitude modulation ratio m_a for the inverter pulse width modulation (PWM) technique described in [91] is varied to control the DC input voltage V_{dc}. The relationship between V_{dc} and m_a is given by equation (6.3) where N_t is the turns ratio of the internal transformer TX of the SB700 and V_{mains} the rms grid voltage.

$$V_{dc} = \frac{\sqrt{2}V_{mains}}{N_t m_a} \qquad 0 \leq m_a \leq 1 \qquad \textbf{(6.3)}$$

Since the SB700 is a grid-connected inverter, regulations on the harmonic content of the output are imposed by the utility to maintain the power quality of the mains. To minimise the harmonic content of the SB700 output over-modulation ($m_a > 1$) is avoided and the inverse relation of (6.3) between m_a and V_{dc} holds true.

Since the ripple and presence of the capacitor C_{in} could affect MPPT performance an understanding of the ripple characteristic and determination of the MPPT properties are all required for the SB700 model. For reference, the BP7175S technical data, taken from the datasheets in Appendix B, are given in Table 6.8.

P_{mpp} (W)	V_{mpp} (V)	I_{mpp} (A)	I_{sc} (A)	V_{oc} (V)	kV_{oc} (V/K)
175.0	36.0	4.90	5.200	44.2	-0.16

Table 6.8: Technical data for BP7175S PV modules at STC

The inverter allows selection of the V_{mpp} range by configuring the low-voltage side of transformer TX, as indicated by the switch SW in Figure 6.18. To allow the inverter to operate under mismatched module conditions, where the PV array voltage loses any contribution from bypassed modules, the SB700 has been set to the lowest V_{mpp} range of 73V-150V. The model value for the transformer turns ratio can be derived from this as described in Chapter 7, subsection 7.2.4.

6.2.2 Outdoor Test Rig Design

An 11.5kWp PV demonstration and research system has been established at the University of Leicester as described in [92]. The system uses sixty-four BP7175S PV modules, divided into 7 sub-arrays of various sizes, each with its own SMA inverter. To keep the cost and complexity of the DMPPT test rig down the smallest sub-array, with 4 PV modules and an SB700 PV inverter, was chosen for testing. The original configuration with a centralised maximum power point tracker (CMPPT) is illustrated in Figure 6.19. The electrical input parameters of the SB700 inverter, taken from the datasheets in Appendix B, are given in Table 6.9.

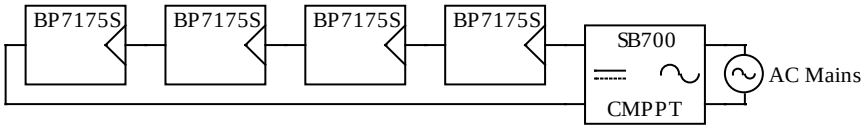


Figure 6.19: PV system with CMPPT

Voltage Range (V)	Maximum Power (W)	Maximum Voltage (V)	Maximum Current (A)
73 – 150	510	250	7

Table 6.9: Input parameters for SMA SB700 inverter

Four SM1230 DCPOs were purchased and installed for testing the DMPPT system displayed in Figure 6.20. The SM manufacturer strongly recommends installing an SM2060 blocking diode to protect the SM1230 DCPOs.

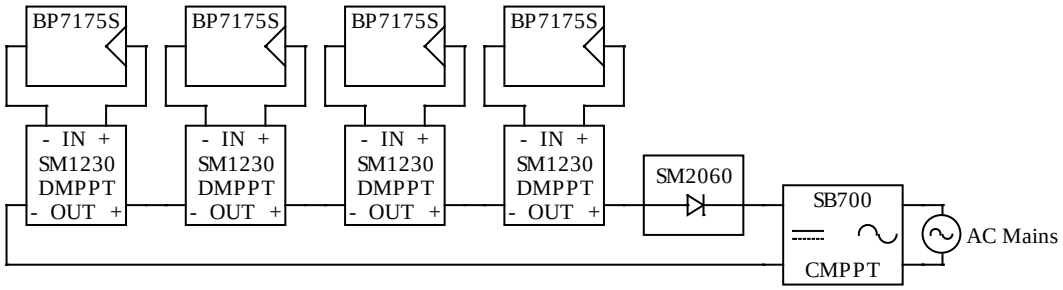


Figure 6.20: PV System with DMPPT

To allow testing of CMPPT and DMPPT on the same array, two ganged multi-pole switches have been added to the setup as shown in Figure 6.21.

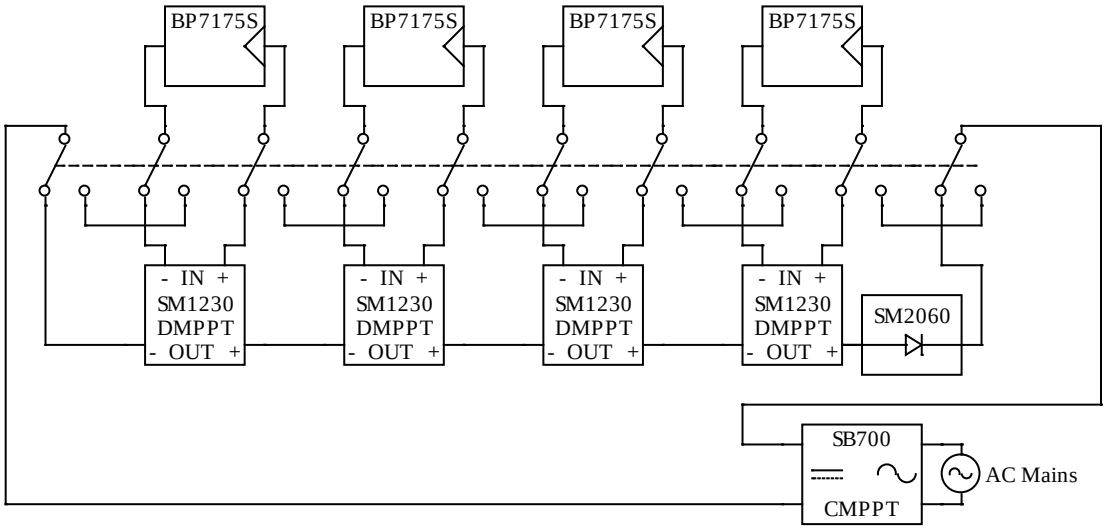


Figure 6.21: Switchover PV system for testing both CMPPT and DMPPT

The switches allow the system to be changed between DMPPT and CMPPT almost instantaneously so that both cases can be tested within a short time span. A single PV system that can be switched over is preferred to two physically separate systems since a comparison between tests on the same PV modules in the same physical position is unaffected by any degradation or soiling. If testing is performed close to solar noon then the change in both irradiance angle and magnitude will be minimized, allowing for a fairer test.

The datalogger included in the test rig is used for measurement of all the system currents and voltages. Isolating transducers are used to scale the measurements to the level required by the datalogger and provide protection from the power circuits.

Situated next to the PV installation there is a tree that casts a shadow onto the array from just before noon. This limits the opportunity for testing of controlled shading patterns to before this time but does allow investigation into a real world problem that may be faced by residential installations.

6.2.3 Controlled Shading Patterns

In order to apply a controlled pattern of shading a semi-translucent material was placed directly onto the PV modules. This method was deemed preferable over the use of an opaque object to cast a shadow on the array since the direct covering of the module's cells improves control of the shaded area which would otherwise be dependent on the angle of the solar beam irradiance when shadowing with an opaque object.

A graph of the ratio of diffuse to global irradiance over a whole sunny day in June is given in [47] for Freiburg, Germany. The graph shows the ratio varying from 100% at sunrise to 10% around noon and back to 100% at sunset. Since shading from nearby objects would leave just the diffuse component, the amount of shaded light could be as low as 10% of the unshaded value. A percentage of around 60% for the shaded irradiance level to the unshaded irradiance level (called the shading percentage from here on) was deemed appropriate for testing.

To obtain a suitable shading material a number of samples were analysed to determine the percentage of transmitted light. The investigation was carried out on the materials in Table 6.10 using the solar emulator described in Section 6.1 with the 10cm x 10cm samples of each material shown in Figure 6.22.

Material Reference	Shading Material
A	2mm Clear Acrylic
B	2mm w/ Car Window Film
C	2mm w/ Silver Reflective Film
D	2mm w/ Bronze Reflective Film
E	3mm Clear Acrylic
F	3mm w/ Car Window Film
G	3mm w/ Silver Reflective Film
H	3mm w/ Bronze Reflective Film

Table 6.10: Shading materials used for analysis

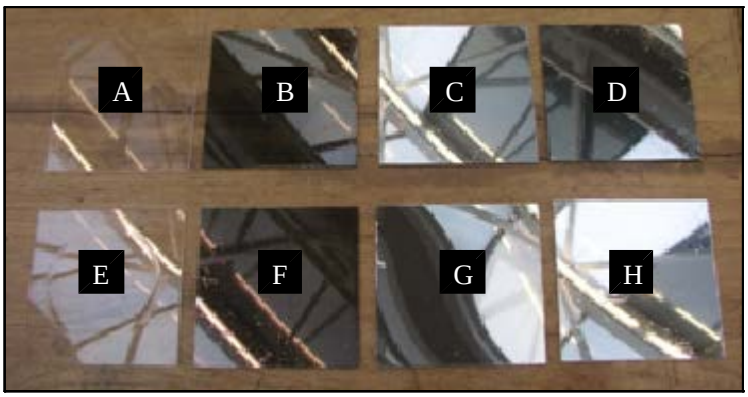


Figure 6.22: Analysis samples of shading materials

To observe the amount of transmitted light an irradiance sensor is required. A photodiode is effectively a small monocrystalline solar cell and has a spectral characteristic close to that of the monocrystalline solar cells of the BP7175S modules in the test rig. Therefore, a BP104S photodiode was selected as the irradiance sensor.

This photodiode has an electrical characteristic similar to a solar cell except that, since it is a low power signal device, the current is much smaller (50μA at 1000lx Appendix B). To explain the operation of the sensor an example characteristic is provided in Figure 6.23 where a positive voltage represents reverse bias of the photodiode.

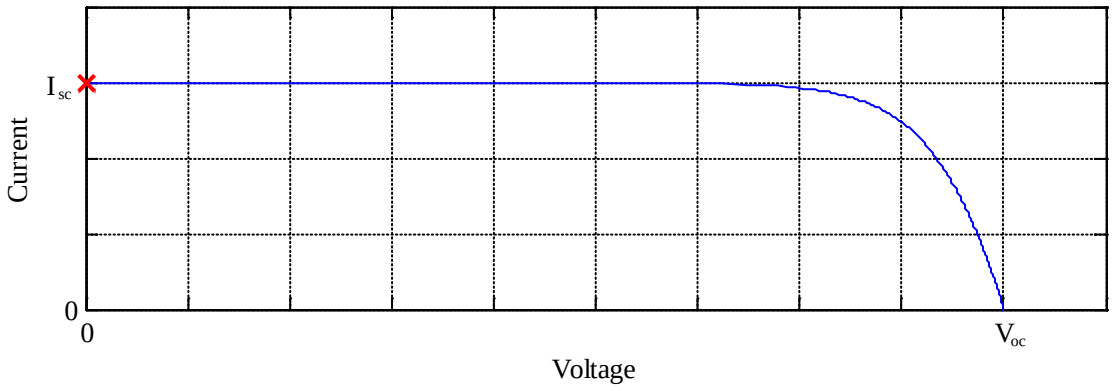


Figure 6.23: Example I-V characteristic of a photodiode

Since the short circuit current I_{sc} is proportional to the incident irradiance on the photodiode it is desirable to operate at this point. This can be achieved using the circuit of Figure 6.24.

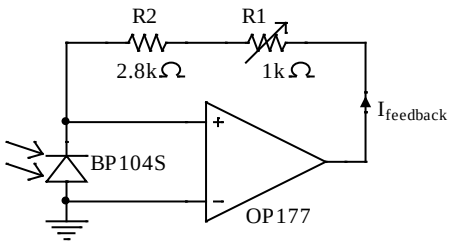


Figure 6.24: Circuit diagram of irradiance sensor

Due to the high gain and high input resistance of the OP177 op-amp the output voltage will rise to a point where the voltage between its inputs, and across the photodiode, is very small and the feedback current is close to I_{sc}. Since this current passes through the feedback resistors the output voltage will be proportional to I_{sc}, and therefore to the irradiance level.

To convert the irradiance readings taken during the tests on the shading materials to a percentage of the unshaded irradiance, the transducer is calibrated to give 10V without shading using the solar emulator. The results of the tests are given in Table 6.11.

Material Reference	Transducer Reading (V)	Shaded Irradiance (%)
A	9.49	94.9
B	6.12	61.2
C	2.79	27.9
D	3.14	31.4
E	9.45	94.5
F	6.26	62.6
G	3	30
H	3.23	32.3

Table 6.11: Results of shading material analysis

To obtain the desired shading percentage of 60%, material B, the 2mm acrylic with car film, was chosen as the shading material. Half-module sheets of the shading material were constructed for use in the outdoor tests as shown on the bottom right module in Figure 6.25. Hooks are attached to the sheets to allow them to be lifted off and dropped

on to the PV module quickly using a specialised tool thus obtaining a fast change in irradiance.

Figure 6.25: Shading material on outdoor test array

6.2.4 Results from Outdoor Test Rig

In order to gain a better understanding of the SB700 MPPT algorithm, data was obtained for a number of tests: start-up after reconnection of the grid, controlled step change in irradiance on a single PV module and natural shading patterns from the nearby tree and during a period of patchy cloud cover. To obtain data for observation of DMPPT system behaviour the tests were also run with the SMs.

First the start-up characteristics of the SB700 were established under different conditions. Figure 6.26 shows the time evolution of the inverter input voltage V_{inv} and illustrates that the same start-up procedure is followed regardless of prevailing conditions. This process appears as a constant slope of decreasing V_{inv} from the open circuit voltage to around 130V at which point the MPPT of the SB700 starts to look for the MPP.

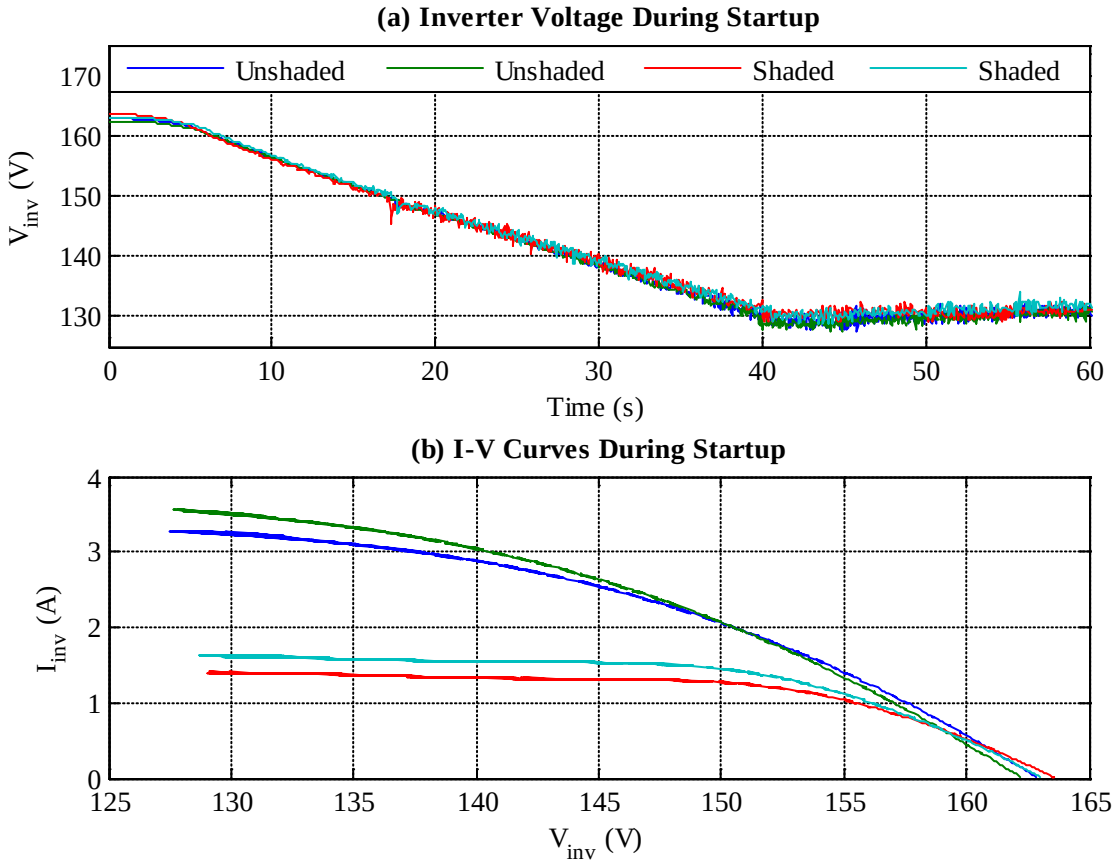


Figure 6.26: Start-up characteristics of SB700

To compare how CMPPT and DMPPT systems react to a change in irradiance on a single PV module an irradiance step change test was performed using the shading procedure described in the previous subsection. The tests are outlined in Table 6.12.

Test Reference	Step in Irradiance	System Configuration
A	Shaded → Unshaded	CMPPT
B	Shaded → Unshaded	CMPPT + DMPPT
C	Unshaded → Shaded	CMPPT
D	Unshaded → Shaded	CMPPT + DMPPT

Table 6.12: Irradiance

The results of Tests A to D are presented in the plots of Figures 6.27 to 6.30 respectively. To obtain a better understanding of the inverter MPPT the time variation of V_{inv} is displayed in plot (a) of each figure. In view of the ripple present on V_{inv} the measured data was filtered to obtain a clearer picture of the underlying waveforms.

To determine the response at module level, plot (b) contains the time evolution of PV module voltages V_{pv} and SM output voltages V_{sm} and plot (c) the corresponding current and power for just CMPPT or currents for DMPPT + CMPPT. Since the three unshaded modules are subjected to similar conditions the response should be the same for each and so only the data of one unshaded module is plotted. To show the relation of the operating point to the PV module characteristics graph (d) displays plots of the PV module power and current trajectories on the P-V and I-V planes respectively.

From observation of plot (a) for each test the MPPT pattern of the inverter (investigated in more detail later) is implied by visible steps every 5s. The V_{inv} time plots also show that the MPPT pattern continues without any significant deviation after the change in irradiance, indicating that the inverter input is voltage controlled.

It can be seen in plot (b) of Figures 6.28 and 6.30 that the change in irradiance causes steps in the SM output voltage since the SMs try to regain the PV module MPPs. The apparent instantaneous steps show that the time the SM takes to respond to a change in irradiance is very quick compared to the inverter. However, the datalogger could not capture the SM response fully due to the sampling time being limited to a minimum of approx. 60ms and the MPPT pattern of the SM having a 1.2ms update period.

It is shown in plots (b) and (d) of Figure 6.27 that before the increase in irradiance the voltage of the shaded PV module (V_{pv} Shaded) is approx. half of the unshaded PV module voltage (V_{pv} Unshaded) indicating that the shaded module was operating with half of its cells bypassed since the shading material only covers half of the PV module. There appears to be 2 maxima in the P-V trajectory before the irradiance change in plot (d) that evidences inverter operation at the MPP of each PV module and also that the I_{mpp} of the shaded module is the same as the unshaded modules.

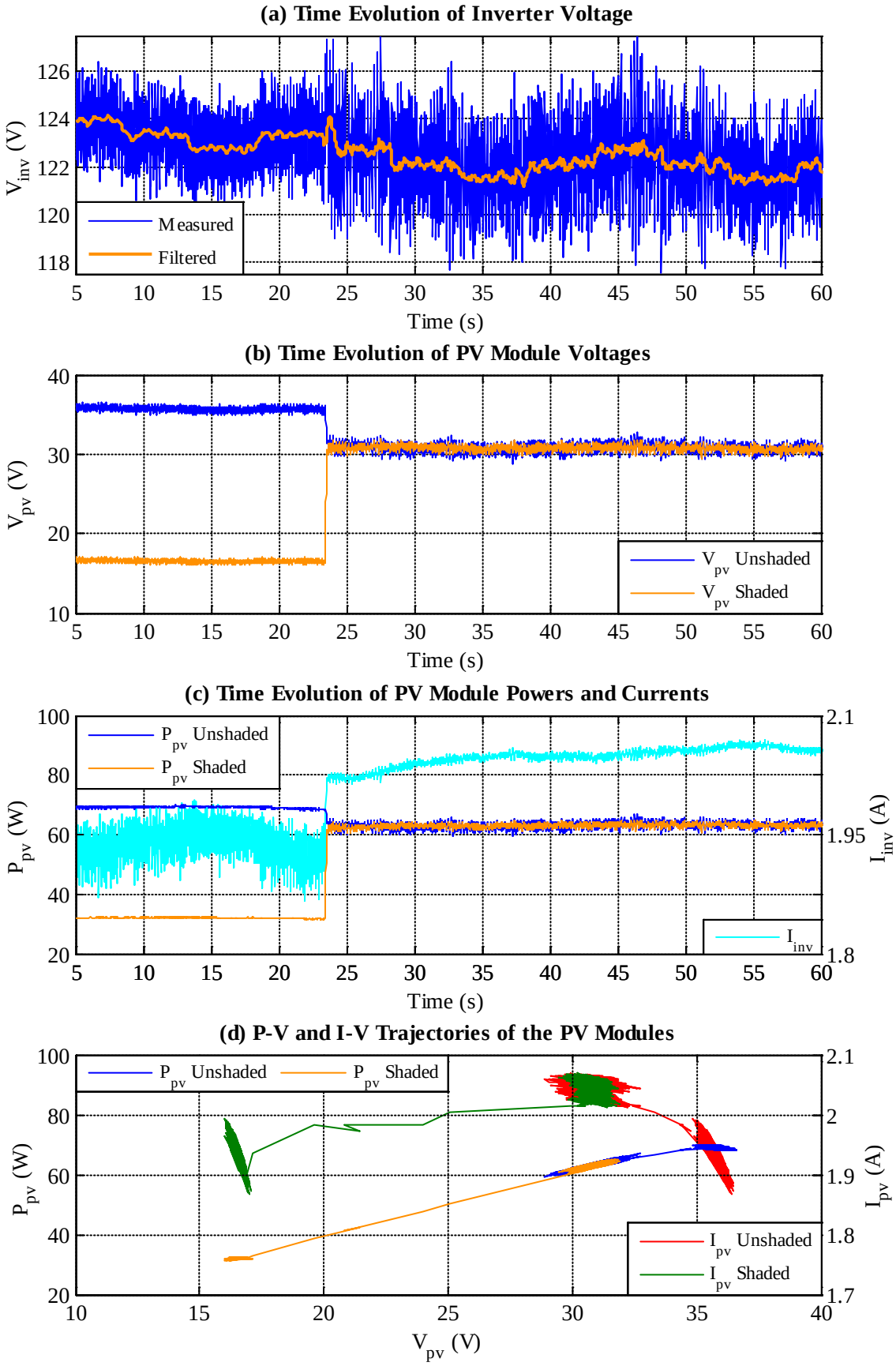


Figure 6.27: Test A - step increase in irradiance without SMs

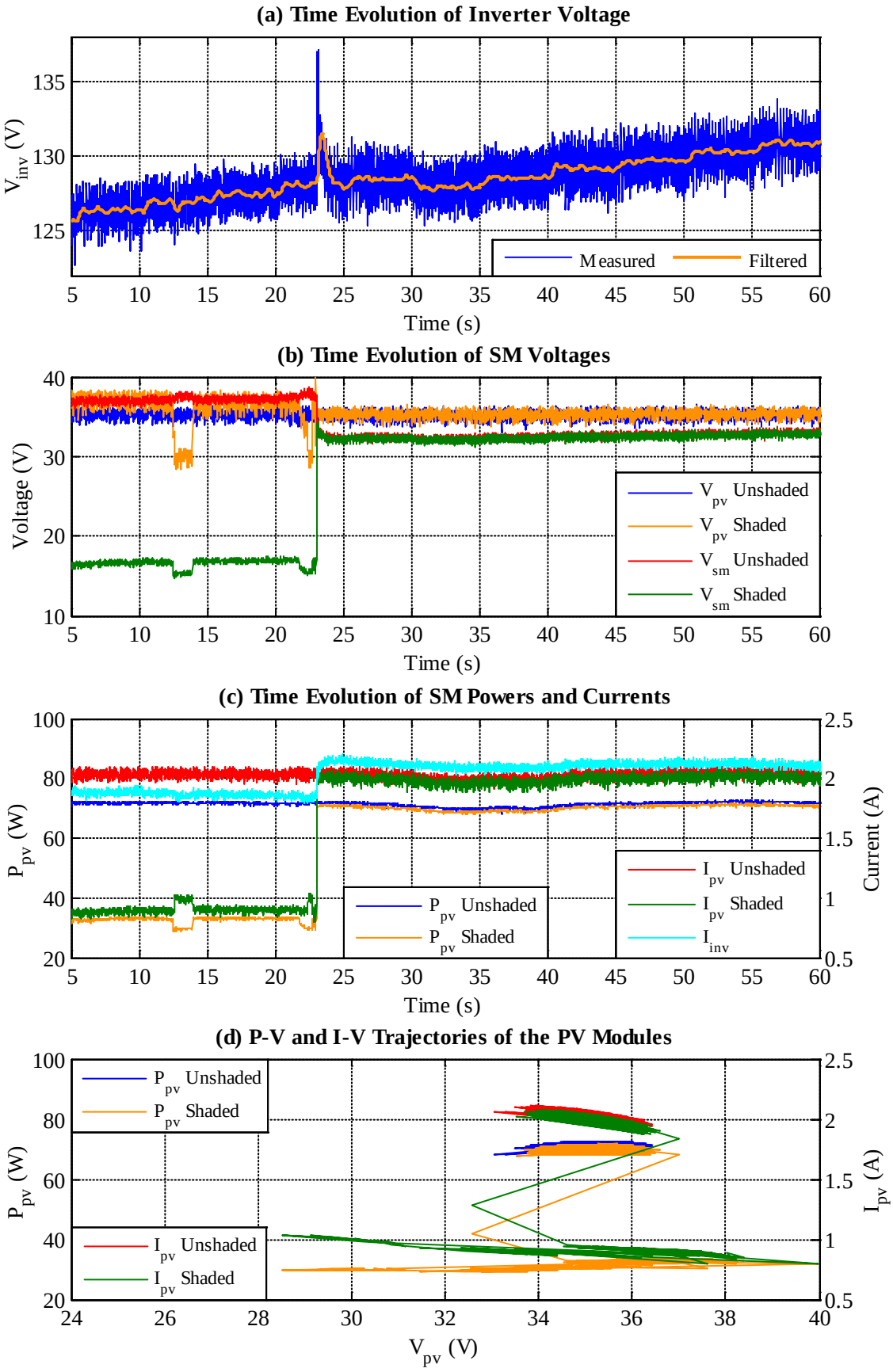


Figure 6.28: Test B - step increase in irradiance with SMs

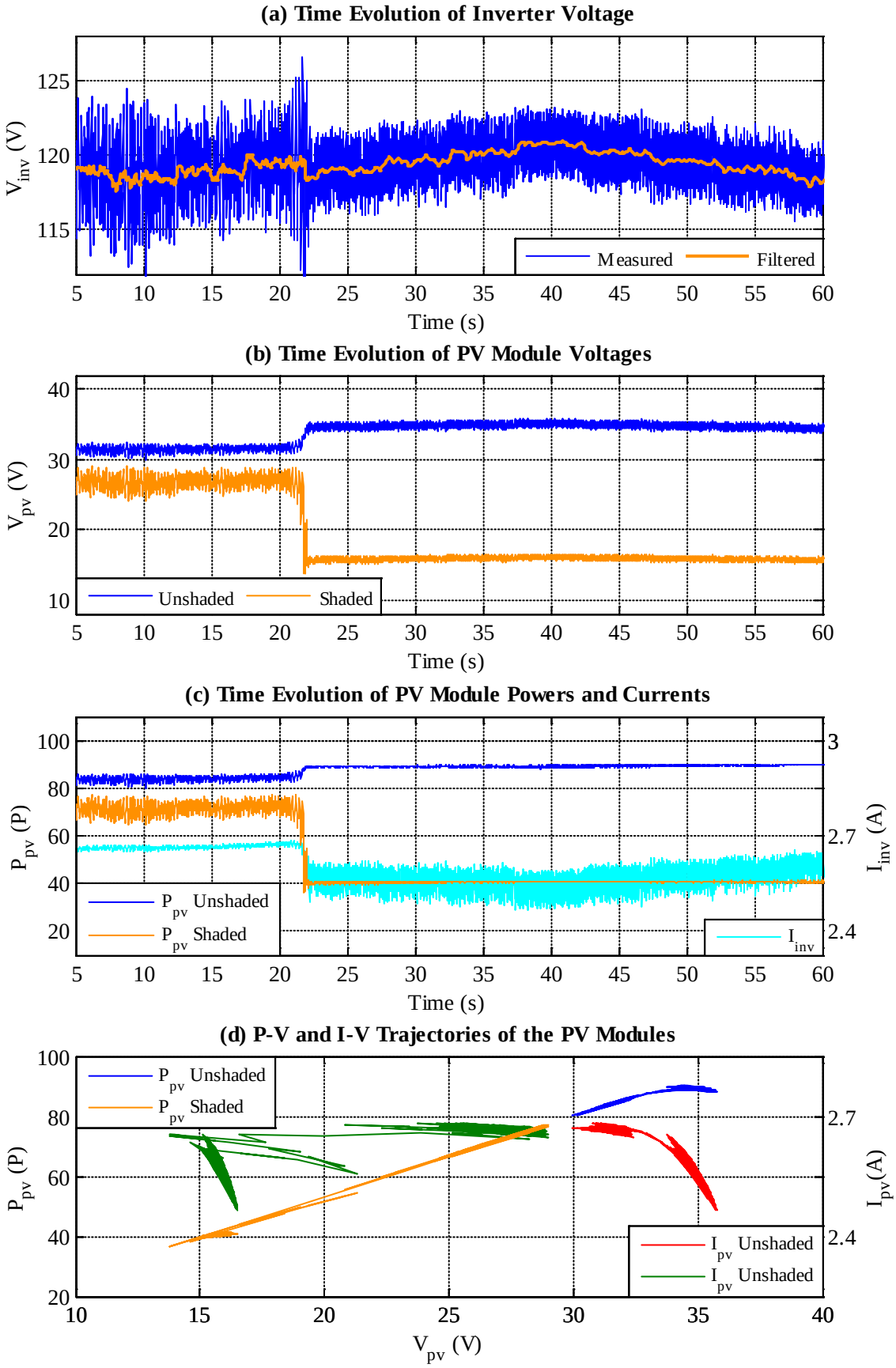


Figure 6.29: Test C - step decrease in irradiance without SMs

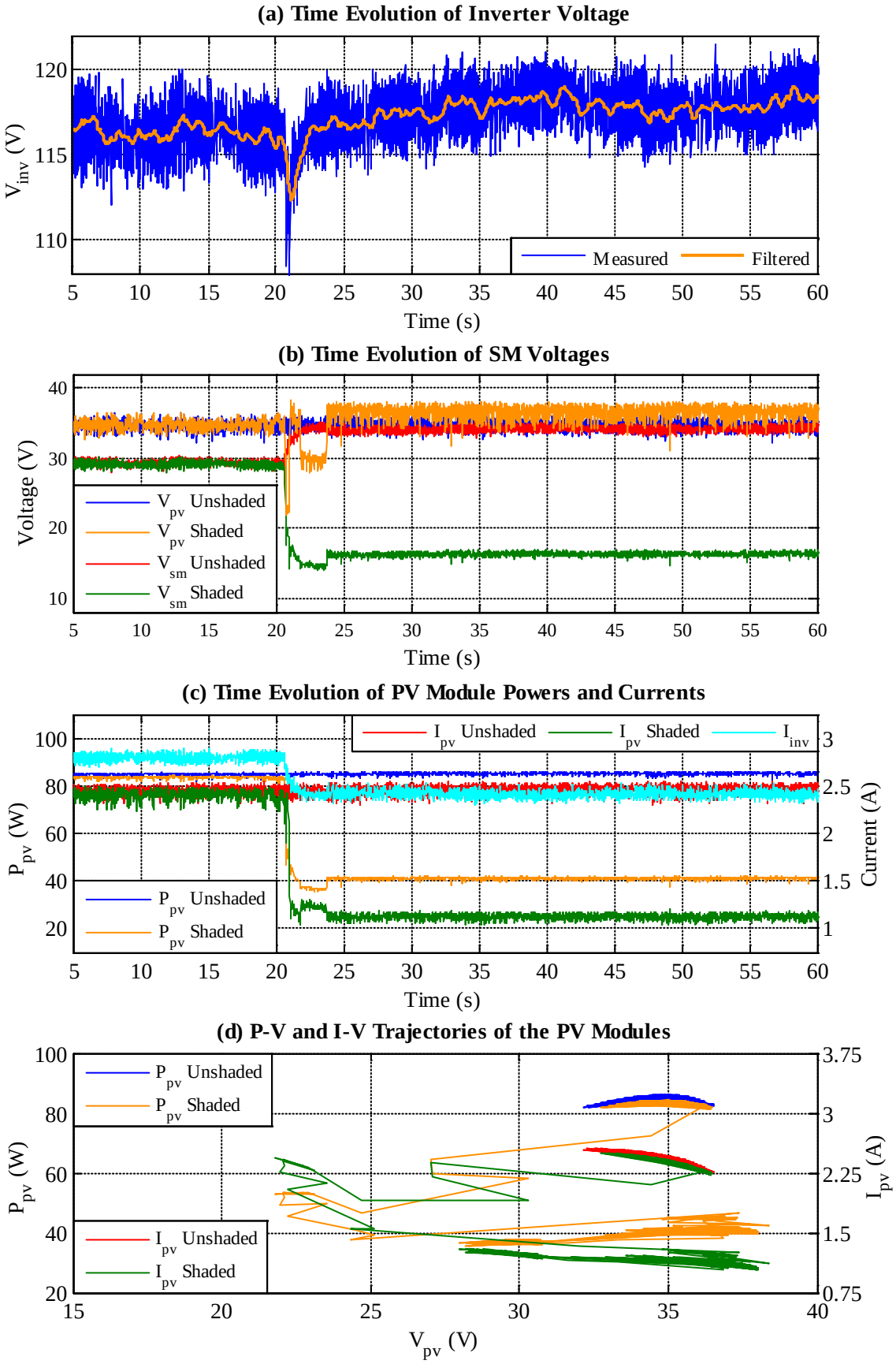


Figure 6.30: Test D - step decrease in irradiance with SMs

In plot (d) of Figure 6.27 the effect on the operating point of the PV modules from maintaining a constant V_{inv} after the irradiance change can be seen. This shows that because half the partially shaded PV module was bypassed, the required V_{mpp} of the inverter is approx. 18V lower than for the case of no shading. Therefore, after the shading is removed the inverter voltage is shared equally between the 4 PV modules resulting in a PV module voltage that is approx. 4.5V lower than the V_{mpp}.

The MPPT pattern of V_{inv} in plot (a) of Figure 6.27 shows a step in V_{inv} of about 0.5V every 5s. The inverter MPPT is therefore very slow and would take almost 3 minutes to obtain the new MPP. This effect makes it challenging to observe both the slow inverter response and the fast SM response.

The PV voltages in plot (b) of Figures 6.28 and 6.30 indicate that the SM maintains the partially shaded PV module at the local maximum in power closest to open circuit where no cells are bypassed. Since this operating point results in a lower I_{mpp}, the SM of the partially shaded module operates in a bucking mode to match the lower module current to the string current.

In Figure 6.28 the unshaded PV module SMs are seen to be boosting their PV module voltage slightly to maintain V_{inv} and compensate for the lower output voltage V_{sm} of the partially shaded SM. This will also have the effect of reducing the string current so that the partially shaded SM bucking action is lessened. It is interesting to note that a slight bucking action is apparent for all of the SMs during the periods without shading indicating that V_{inv} is too low.

To obtain accurate values of the parameters for the MPPT pattern of the SB700, sections of the filtered V_{in} waveforms from the irradiance step tests, both with and without SMs, are examined in Figure 6.31. The MPPT update period can be seen as 5s and the perturbation appears to be a step in voltage of 0.6V. This implies the use of

voltage control in the inverter with the perturbation applied to the reference of the controller.

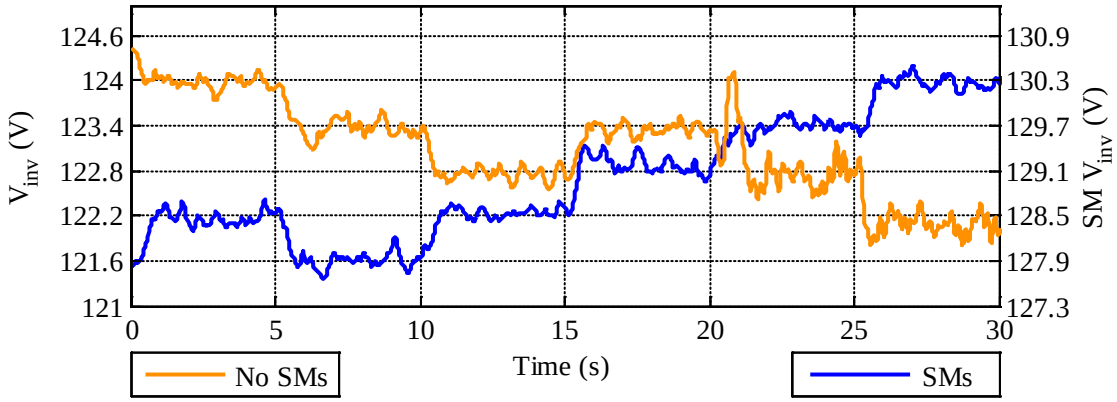


Figure 6.31: SB700 MPPT steps

To analyse the ripple the SB700 is tested during steady state operation using an oscilloscope with the results shown in Figure 6.32.

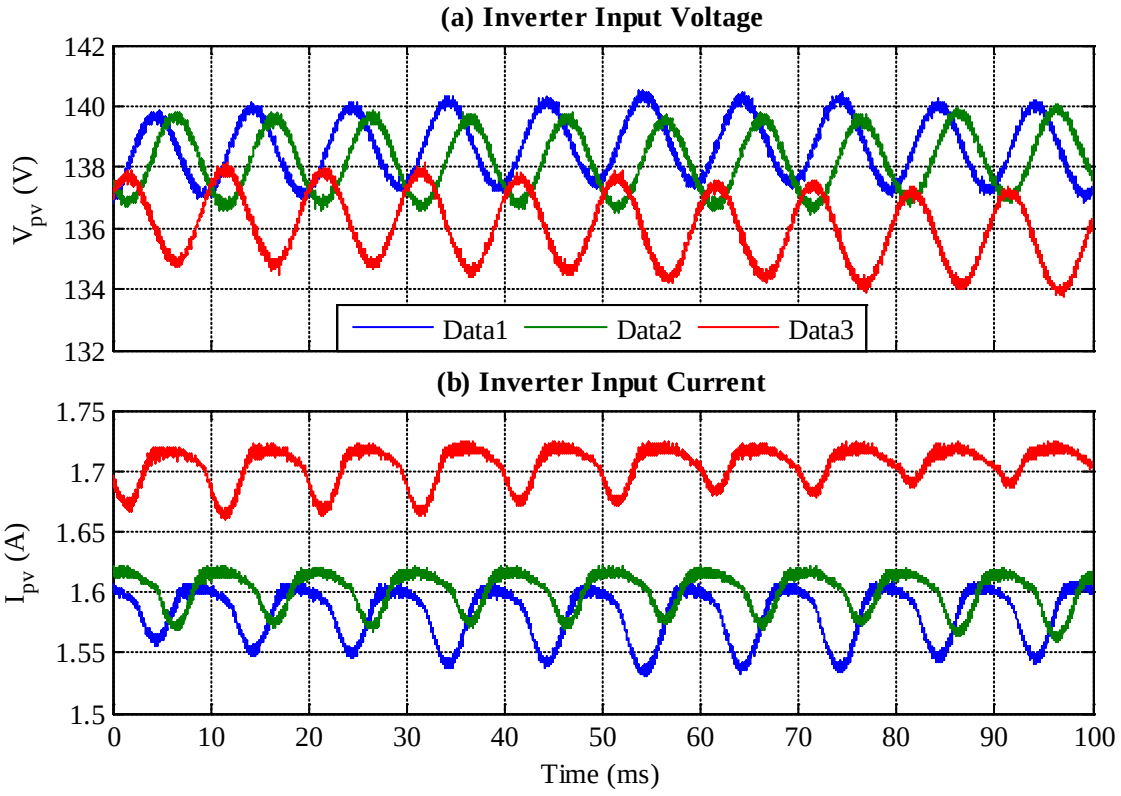


Figure 6.32: Inverter ripple recorded using oscilloscope

The back-propagation of voltage ripple was observed in the 3 sets of data obtained at a sample time of 10µs. The resulting waveforms of inverter input voltage and input current indicate the predicted 100Hz input voltage ripple that has a peak voltage of about 1.5V. The current is non-sinusoidal due to the non-linear nature of the PV source. To gain a better understanding of the ripple a linear Thévenin source can be used to obtain a sinusoidal current, as is explained in the next section.

6.3 Indoor Testing of an SB700

In order to develop the PSpice model of the SB700 three properties need to be defined; the MPPT parameters, the input capacitance C_{in} and the ripple characteristic. Since the inverter efficiency has little effect on the MPPT action of the SB700 it is omitted from the model.

The MPPT parameters are obtained from observation of the outdoor test waveforms described in the previous section. However, a more controlled test of the inverter is required to determine the relationship of the input ripple to the DC input voltage and current whilst also acquiring a value for C_{in}. This section explains the use of an indoor test for this purpose.

6.3.1 SB700 Testing with a Thévenin Source

To obtain the characteristic of the ripple, whilst obtaining a value for the input capacitor, indoor testing of the SB700 is carried out with a Thévenin source using the circuit shown in Figure 6.33. The internal input capacitor C_{in} of the SB700 is shown along with a block to represent the switching section.

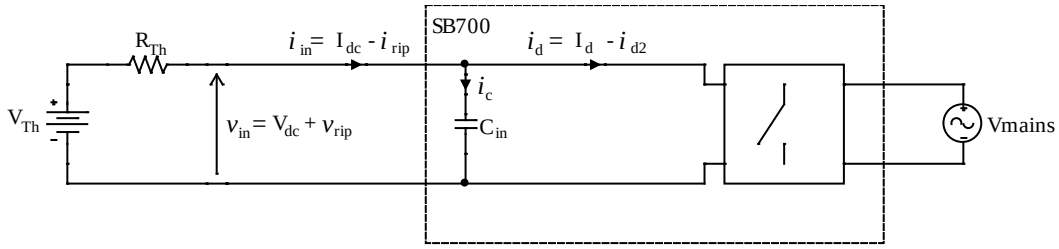


Figure 6.33: Setup for SB700 test with a Thévenin source

The waveforms for i_{in} and v_{in} are measured for a range of input voltages and currents defined in Table 6.13.

Test Reference	Variable	Range	Increment	Constant Value
A	V_{mpp}	75V to 115V	10V	I_{mpp} = 5A
B	I_{mpp}	1A to 5A	1A	V_{mpp} = 75V
C	I_{mpp}	1A to 5A	1A	V_{mpp} = 100V

Table 6.13: Thévenin source tests for SB700

Since the maximum power will be delivered when the inverter input resistance is the same as R_{Th}, the voltage source V_{Th} is set to $2V_{mpp}$ and the value for R_{Th} calculated by dividing V_{mpp} by I_{mpp}. To obtain the experimental ripple characteristic the measured waveforms are plotted and analysed as shown in the example plot of Figure 6.34.

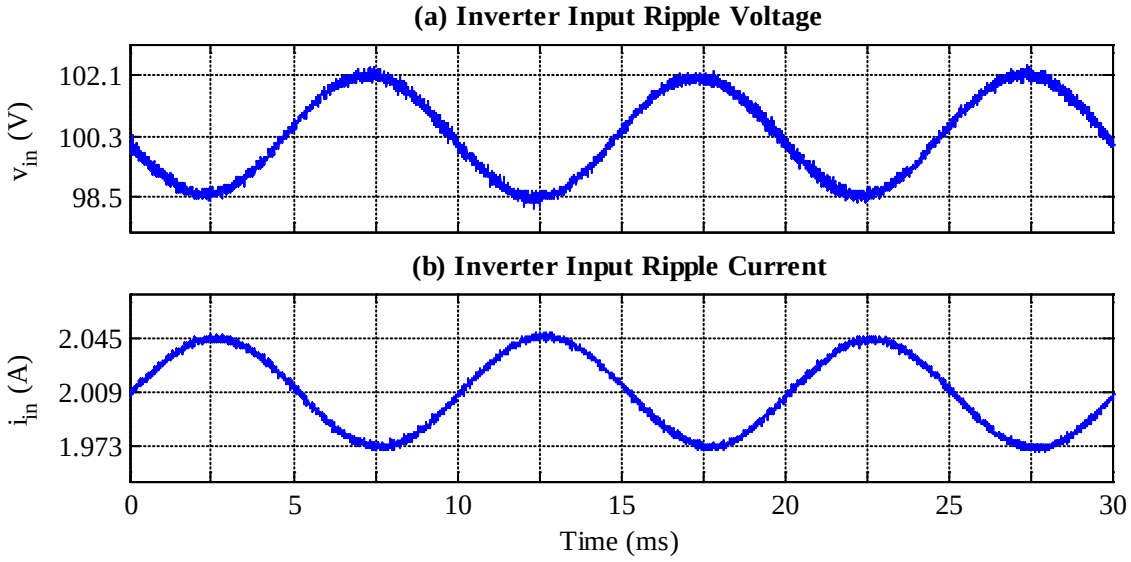


Figure 6.34: Inverter ripple waveforms

The voltage waveform v_{in} shows a DC component V_{dc} of 100.3V with the added 100Hz ripple v_{rip} with a peak value $V_{rip}|_{pk}$ of 0.8V. Similarly, the current waveform gives an I_{dc} of 2.009A and $I_{rip}|_{pk}$ of 36mA.

It can be seen that a near 180° phase shift exists between v_{rip} and i_{rip} implying that the ripple current originates from the inverter; the slight shift from 180 indicates a leading current which is most likely due to the inductance of the rheostat. The observation of a 180° shift is supported by theory from [91].

$$i_{\mathrm{d}} = \mathrm{I_d} - i_{d2} \qquad \textbf{(6.4)}$$

Equation (6.4) shows that the current flowing into the switching section i_d consists of the DC current I_d and a negative 2nd harmonic component i_{d2}. The rms value I_{d2} of the AC current i_{d2} is proportional to the rms values V_{out} and I_{out} (defined in Figure 6.18) and inversely proportional to the DC input voltage V_{dc}.

$$\mathrm{I_{d2}} = \frac{\mathrm{V_{out}I_{out}}}{\sqrt{2}\mathrm{V_{dc}}} \qquad \textbf{(6.5)}$$

Re-arranging (6.5) shows that the product of the DC input voltage V_{dc} and the peak i_{d2} value $I_{d2}|_{pk}$ is equal to the rms output power of the inverter.

$$\sqrt{2}\mathrm{I_{d2}V_{in}} = \mathrm{V_{out}I_{out}} \qquad \textbf{(6.6)}$$

At steady-state the inverter operates at the MPP and so the DC input voltage is V_{mpp}, the DC input current I_{mpp} and input power the product of V_{mpp} and I_{mpp}. Therefore, assuming a power factor of 1, as indicated on the datasheet in Appendix B, and neglecting the inverter losses, equation (6.6) can be re-written to show that $I_{d2}|_{pk}$ is equal to the source I_{mpp}.

$$\hat{\mathrm{I}}_{\mathrm{d2}} = \mathrm{I_{mpp}} \qquad \textbf{(6.7)}$$

To analyse the AC ripple currents, and associated ripple voltage, an AC equivalent circuit of the test using a Thévenin supply has been derived from the observation that the inverter input acts as an AC current source. Therefore, the direction of i_{d2} and i_{rip} are the reverse of i_d and i_{in} respectively and i_{rip} is no longer 180° out of phase with v_{rip}. The equivalent circuit in Figure 6.35 indicates that the ripple is dependent on the source impedance $Z_{s,}$ in this case R_{Th}, and the reactance X_c of C_{in}.

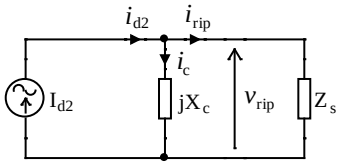


Figure 6.35: AC equivalent circuit of the Thévenin source test

As observed the ripple occurs at twice the mains frequency. The magnitude of the reactance $|X_c|$ can therefore be defined at a frequency of 100Hz.

$$|X_c| = \frac{1}{200\pi C_{in}} \qquad \textbf{(6.8)}$$

The ripple voltage v_{rip} caused by i_{d2} could have an effect on the MPPT controllers in a DMPPT system. The model of the SB700 therefore requires a model relating v_{rip} to the operating point of the inverter. To obtain the desired characteristic the AC equivalent circuit was analysed using the phasor diagram of the peak currents illustrated in Figure 6.36.

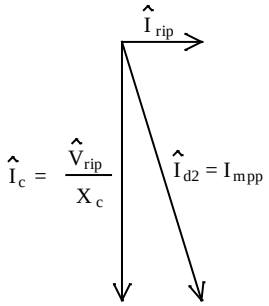


Figure 6.36: Phasor diagram of the Thévenin source tests

The equation for calculating the capacitor reactance from the measured data was derived from the phasor diagram. X_c was found to have a magnitude of 0.888Ω which was used to obtain a value of approx. 1800µF for C_{in} using (6.8).

$$X_c = \frac{\hat{V}_{rip}}{\sqrt{I_{mpp}^2 - \hat{I}_{rip}^2}} \qquad \textbf{(6.9)}$$

The relation of R_{Th} to the peak ripple values $V_{rip}|_{pk}$ and $I_{rip}|_{pk}$ can be derived from inspection of the AC equivalent circuit.

$$R_{Th} = \frac{\hat{V}_{rip}}{\hat{I}_{rip}} \qquad \textbf{(6.10)}$$

Since the inverter operates at MPP during steady state the DC voltage dropped across R_{Th} due to I_{mpp} will be equal to V_{mpp}.

$$R_{Th} = \frac{V_{mpp}}{I_{mpp}} \qquad \textbf{(6.11)}$$

Equations (6.10) and (6.11) can be equated to derive a relation between the peak ripple values and the MPP values.

$$\frac{V_{mpp}}{I_{mpp}} = \frac{\hat{V}_{rip}}{\hat{I}_{rip}} \qquad \textbf{(6.12)}$$

A second equation relating I_{mpp} to the peak ripple values is derived from the phasor diagram.

$$I_{mpp}^2 = \hat{I}_{rip}^2 + \frac{\hat{V}_{rip}^2}{X_c^2} \qquad \textbf{(6.13)}$$

To obtain equations describing $I_{rip}|_{pk}$ and $V_{rip}|_{pk}$ in terms of the inverter operating point equation (6.12) is re-arranged and substituted into (6.13) to eliminate $V_{rip}|_{pk}$ and $I_{rip}|_{pk}$ respectively.

$$\hat{I}_{rip} = \frac{X_c I_{mpp}^2}{\sqrt{X_c^2 I_{mpp}^2 + V_{mpp}^2}} \quad \textbf{(6.14)}$$

$$\hat{V}_{rip} = \frac{X_c I_{mpp} V_{mpp}}{\sqrt{X_c^2 I_{mpp}^2 + V_{mpp}^2}} \quad \textbf{(6.15)}$$

Since for the SB700 X_c is less than 1Ω, the maximum I_{mpp} is 7A and the V_{mpp} range is 75V to 150V, it follows that:

$$V_{mpp}^2 \gg X_c^2 I_{mpp}^2 \quad \textbf{(6.16)}$$

Equations (6.14) and (6.15) can therefore be reduced to (6.17) and (6.18) respectively. Approximate relationships can be seen in these equations; the ripple current varies with the square of I_{mpp} and is inversely proportional to V_{mpp} whereas the ripple voltage varies linearly with I_{mpp} but doesn't vary with V_{mpp}.

$$\hat{I}_{rip} \approx \frac{X_c I_{mpp}^2}{V_{mpp}} \quad \textbf{(6.17)}$$

$$\hat{V}_{rip} \approx X_c I_{mpp} \quad \textbf{(6.18)}$$

To verify the derived equations for the peak ripple values the characteristics are plotted with the experimental data in Figure 6.37. The plots show that the equations give a good representation of the measured data except for a few minor differences: it can be seen that in plots (a) and (c) the measured ripple current is slightly lower than expected for the measurement at 75V and 5A, plot (b) also shows the measured ripple voltage at 75V, 1A is also a bit lower than predicted, and plot (c) has a small offset in the ripple current – DC voltage characteristic. However, these differences are negligible in terms of modelling the SB700 behaviour and the derived equations are used.

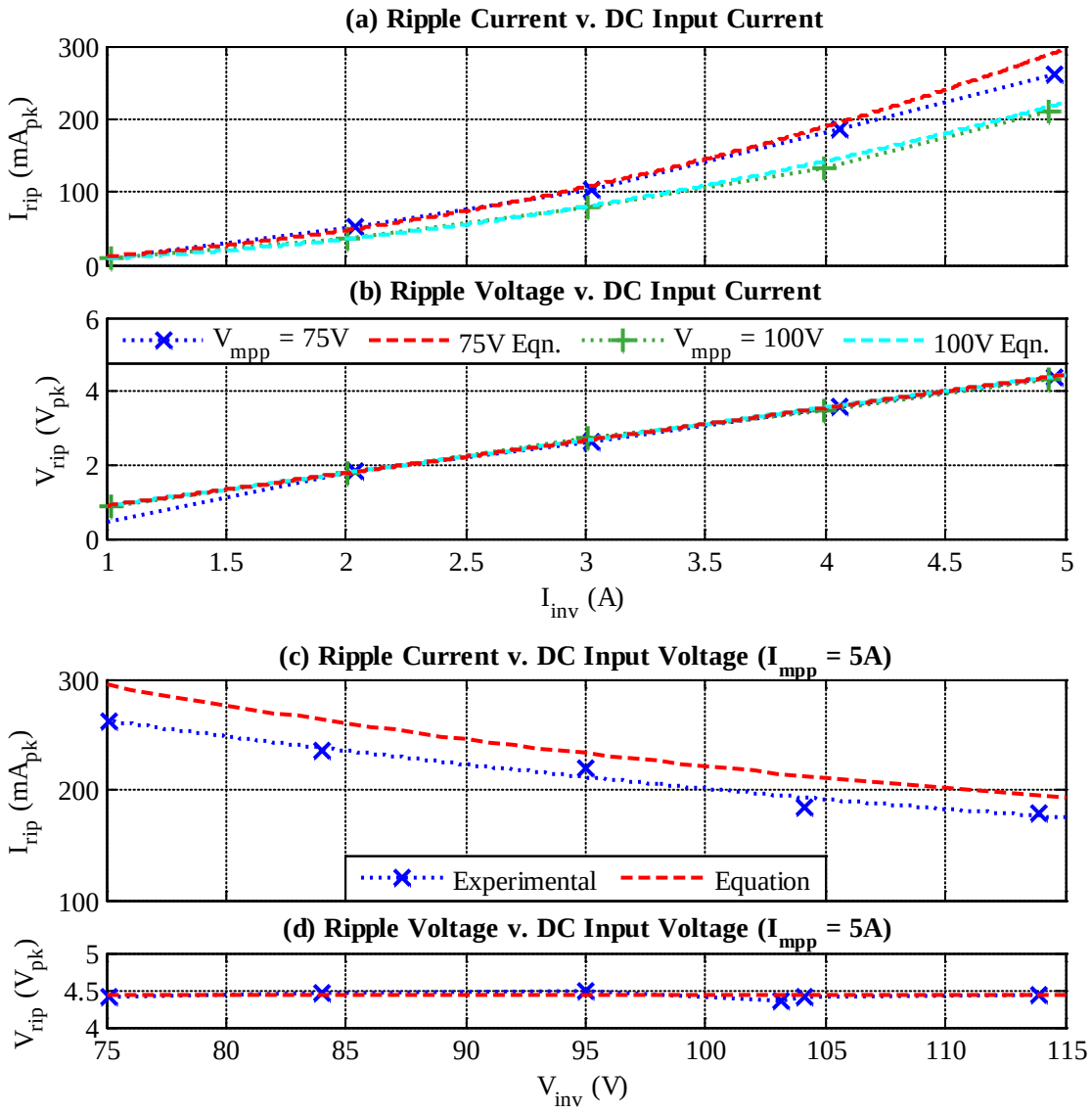


Figure 6.37: Ripple characteristics for the SB700

6.4 Summary of PCD Testing

This chapter has presented analyses of tests undertaken on power conditioning devices (PCDs) to obtain the required parameters for the modelling in Chapter 7. The test methods have been described and relevant results displayed and discussed. The PCDs considered were the SolarMagic (SM) DC power optimiser (DCPO) and the SMA SB700 PV inverter.

The first section provides details of indoor tests carried out on the SM. Tests carried out using a solar emulator with MSX60 PV module were described. In the time plots of

voltage and power a constant MPPT period of 1.2ms was observed. FFTs of the voltage revealed that a switching modulation technique involving two frequencies, 26.5kHz and 212.5kHz, is used inside the SM. To allow values of the SM energy storage components to be obtained the voltage-time plots were also observed on a smaller time scale to see the dynamic response. Furthermore, for verifying the SM MPPT model in Chapter 7 the SM start-up routine was examined.

The dependencies of the efficiency η and the duty cycle perturbation ΔD on the operating point of the SM were also investigated. Since the V_{mpp} range of the MSX60 was limited in the solar emulator, the PV module emulator (PVME) developed in Chapter 5 was used for extending the SM test range. The results were analysed and it was concluded that η can be modelled as a constant value of 94%, whereas ΔD displayed a piecewise linear type characteristic against the duty cycle D that will be applied as a lookup table in the MPPT model.

The second section describes the outdoor PV test facility at the University of Leicester and the modifications made to enable testing of a distributed maximum power point tracker (DMPPT) system. Details are given on the development of a means of applying controlled shading to the test array using sheets of translucent shading material.

A comparison of the response to a step change in irradiance on a single PV module was made between the system with and without DMPPT. The system without DMPPT was shown to have a slow but steady response to the irradiance change. However, the SMs in the DMPPT system appear to have a procedure for relocating the MPPs, indicated by a step change in the time plots of the module voltages. This behaviour is investigated further in Chapter 7.

The outdoor test results were also used to determine the operation of the SB700 MPPT which was found to have a constant period of 5s and a constant voltage perturbation of

0.6V. A 2nd harmonic 100Hz ripple at the inverter input was observed using an oscilloscope which showed a sinusoidal voltage ripple with a distorted current ripple.

The third section presents indoor tests to further investigate the ripple of the inverter using a Thévenin source. Equations for describing the ripple in terms of the inverter operating point are derived and were plotted with the experimental data for comparison. These plots have demonstrated a close match and the equations are therefore deemed accurate enough for use in the inverter model. The measured data was also used to obtain the value of 1800μF for the input capacitor C_{in}

Chapter 7 Computer Simulation of PV Systems with DMPPTs

In Chapter 6 a real-world photovoltaic (PV) system and its power conditioning devices (PCDs) were tested to analyse the behaviour of the maximum power point trackers (MPPTs). However, a full analysis of MPPT interactions was difficult to achieve as the tests were limited in terms of the PCDs and testing systems available.

Therefore computer simulations of PV system PCDs have been developed from the data obtained in Chapter 6. These models allow a more detailed investigation into interactions between PCD MPPTs. The development of the simulation models is described in this chapter.

7.1 Simulation of a PV Array

Combined models of a PV array and the associated PCDs are required for analysis of the dynamic interactive behaviour of MPPTs. To simulate distributed MPPT (DMPPT) systems a collection of PV module models with independent parameter control is required. The individual PV module models are necessary for combining with per-module PCD models.

In Chapter 4 the MATLAB based computer simulation of a PV array, PVArraySim, was presented. PVArraySim was designed to produce a single accurate lookup table of a PV array's I-V characteristic for use in a hardware PV emulator. PVArraySim allows individual control of the PV module parameters permitting simulation of partial shading conditions.

The speed of the simulation was not the main criteria for PVArraySim as it was designed to generate an instantaneous static characteristic using iterative algorithms. PVArraySim was also designed to generate a single characteristic for the entire PV

array. Therefore PVArraySim is not suitable for use in a dynamic simulation of a DMPPT system.

A new PV model was required to simulate a DMPPT system where dynamic simulation of a number of separate PV modules is important. The required PV model was produced in PSpice as this facilitates the combination of a dynamic electrical model with a model of the PCDs. The development of the PV cell model, and the subsequent expansion into PV module and array models, are described in this section.

7.1.1 PV Cell Model

It is possible to construct a direct representation of the single diode model introduced in Chapter 2 in PSpice as shown in Figure 7.1. However this would mean that only the current source I_{ph} could be updated during a simulation. For simulating time varying environmental conditions a more flexible programmable model with the ability to change the parameters of the diode junction and the resistances during a simulation is desired.

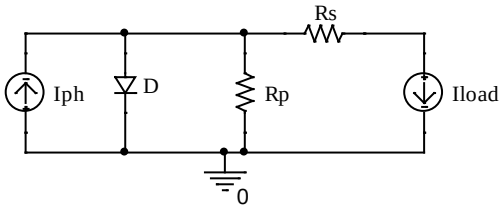


Figure 7.1: PSpice single diode model representation of a PV cell

PSpice offers a range of analogue behavioural model (ABM) blocks that are either pre-programmed for a specific function or allow the user to enter an expression for the output. A PV cell model was developed based on these blocks. A list of the important blocks used and a brief description of their functionality is given in Table 7.1. Appendix E contains the full list of blocks used.

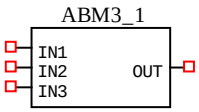
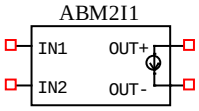
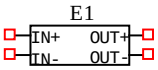
Block Name	Diagram	Description
ABMn_		ABMn_ has n single ended voltage inputs and a single ended voltage output that are referenced to the circuit ground. The output is programmed by a user set expression dependent on the inputs. A differential voltage input can be created by subtracting one input from another.
ABMnI		ABMnI has the same functionality as ABMn_ except that the output is a 2 terminal floating current source. This is useful for simulating the current drawn by a variable parallel resistance.
EVALUE		EVALUE has a 2 terminal floating voltage source output programmed by a user set expression dependent on a 2 terminal differential voltage input. The expression can be rewritten to use single ended inputs. This is useful as part of simulating the voltage dropped across variable series resistance.

Table 7.1: Description of PSpice ABM blocks

The programmable PSpice ABM model of a PV cell model is shown in Figure 7.2. The assignment of the PV model parameters using the CONST blocks and the DC current source I_{ph} permits control of the parameters by an SLPS linked Simulink simulation.

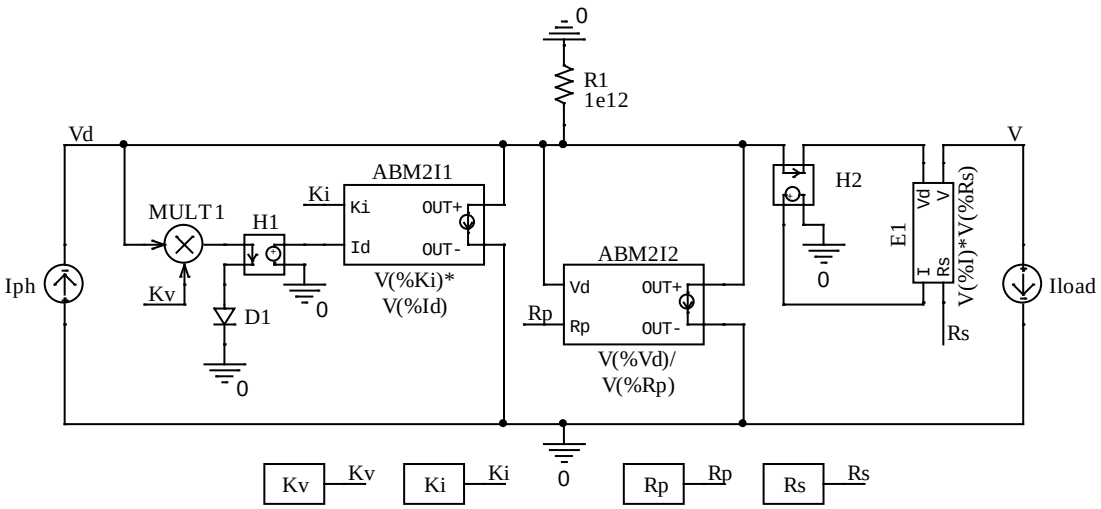


Figure 7.2: PSpice analogue behavioural model of a PV cell

The PSpice diode model D1 is combined with MULT1, H1 and ABM2I1 to allow allocation of the diode junction parameters. The model of D1 applies the Shockley

equation (7.1) with a default ideality factor $\gamma_{default}$ of 1, default absolute temperature $T_{default}$ of 300K and dark saturation current $I_o|_{D1}$ of 10^{-10}A. $I_o|_{D1}$ has been set to this value as the dark saturation current of a PV cell junction is generally of this magnitude around 25°C although it varies significantly with temperature T.

$$I_{D1} = I_o|_{D1}\left(e^{\left(\frac{qV_{D1}}{k\gamma_{default}T_{default}}\right)} - 1\right) \quad \textbf{(7.1)}$$

In the ABM PV cell model I_{D1} is converted to a voltage by H1 so that ABM2I1 can multiply I_{D1} by the factor K_i. This allows manipulation of $I_o|_{D1}$ as demonstrated in equation (7.2) derived from multiplying (7.1) by K_i. The output of ABM2I1 draws the resulting current I_d away from I_{ph}.

$$I_d = K_i I_o|_{D1}\left(e^{\left(\frac{qV_{D1}}{k\gamma_{default}T_{default}}\right)} - 1\right) \quad \textbf{(7.2)}$$

The desired PV cell saturation current I_o can therefore be programmed using the parameter K_i which is pre-calculated using (7.3).

$$K_i = \frac{I_o}{I_o|_{D1}} \quad \textbf{(7.3)}$$

Equation (7.1) is re-written in (7.4) to make V_{D1} the subject so that the strategy for modifying the junction parameters γ and T can be explained.

$$V_{D1} = \frac{k}{q}\gamma_{default}T_{default}\ln\left(\frac{I_{D1}}{I_o} + 1\right) \quad \textbf{(7.4)}$$

The PV cell junction voltage V_d for the desired values γ_{new} and T_{new} can be calculated with equation (7.5) that has been derived from (7.4).

$$V_d = \frac{\gamma_{new}T_{new}}{\gamma_{default}T_{default}}V_{D1} \quad \textbf{(7.5)}$$

In the model of Figure 7.2 the block MULT1 achieves the variability in T and γ by multiplying V_d by a factor K_v to give the required V_{D1}. The factor K_v is pre-calculated using (7.6) obtained from (7.5).

$$K_v = \frac{T_{default}\gamma_{default}}{\gamma_{new}T_{new}} \qquad \textbf{(7.6)}$$

The block ABM2I2 represents the parallel resistance in the single diode model and is set using the parameter R_p. The output of ABM2I2 draws I_p away from I_{ph}.

The EVALUE block E1 acts as the series resistance of the single diode model using single ended voltage inputs. CCVS block H2 converts the PV cell output current I to a voltage. E1 multiplies this voltage by the series resistance R_s to obtain the voltage drop IR_s. The differential voltage output of E1 subtracts IR_s from V_d to give the PV cell output voltage V.

The DC current source I_{load} was increased from 0A to short circuit in steps of 0.1mA to obtain the I-V characteristic of the model. However, the only connections from the nodes V_d and V to ground are through the current sources I_{ph} and I_{load} which are treated as open circuit in PSpice. The nodes V_d and V would therefore be considered as floating and prevent PSpice from running the simulation. The resistor R1 is introduced to connect V_d and V to ground. R1 is set to the maximum permissible resistance to minimise the effect it has on the simulation.

The PV cell model was used to simulate a cell from the BP7175S PV module. To convert to module level the cell voltage is multiplied by the number of series connected cells in the module, which is 72. The resulting data is plotted in Figure 7.3 along with the characteristic taken from the datasheet in Appendix B. Figure 7.3 demonstrates that the PSpice model is an acceptably accurate representation of the actual PV module.

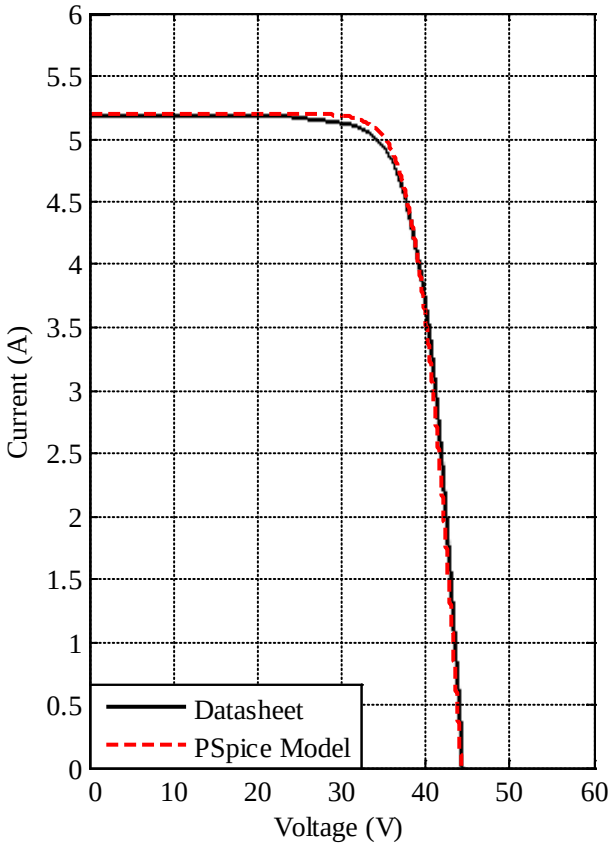


Figure 7.3: I-V characteristic of BP7175S PV module

7.1.2 PV Module Model

A PV cell model with programmable parameters has been described in the previous subsection. However, it would not be practical to set the parameters for each individual PV cell when simulating a PV array consisting of multiple PV modules as there would be hundreds or possibly thousands of cells. Therefore scaling of the PV cell model to the level of a PV module was necessary. Chapter 1 outlines how the parameters of the single diode model are converted.

The ability to simulate PV arrays of various sizes and configurations is desired for analysing DMPPT systems. A PV module model that minimises the complexity of creating a PV array simulation is therefore required.

Simulation of PV arrays subjected to mismatch conditions, especially partial shading, is essential. The PV module model must therefore include the bypass diodes that protect

the underperforming modules and allow the others to maintain operation close to their MPPs. To reduce the complexity of the PV module model all of the cells within a module, and all of the bypass diodes, are assumed to be identical and subjected to uniform environmental conditions.

The number of bypass diodes per module (N_d) is the parameter input on the left of the PV module block. Since N_d only depends on the type of PV module it is only specified once per array. However the parameters at the bottom of the block vary with the environmental conditions of irradiance and temperature and hence are set on a per-module basis. All of the parameters can either be controlled by a Simulink model or set directly in PSpice.

The required scaling of the PV cell model parameters with respect to the number of series connected cells N_s and parallel connected cells N_p in a PV module is outlined in Chapter 2. The equations (7.7) to (7.11) are applied to the ABM model. These equations assume that all of the cells within the module are identical and operate at the same environmental conditions.

$$I_{ph}|_{module} = N_p I_{ph}|_{cell} \quad \textbf{(7.7)}$$

$$R_s|_{module} = \frac{N_s}{N_p} R_s|_{cell} \quad \textbf{(7.8)}$$

$$R_p|_{module} = \frac{N_s}{N_p} R_p|_{cell} \quad \textbf{(7.9)}$$

$$I_d|_{module} = N_p I_d|_{cell} \quad \textbf{(7.10)}$$

$$V_d|_{module} = N_s V_d|_{cell} \quad \textbf{(7.11)}$$

The relationship between $K_i|_{module}$ and $K_i|_{cell}$ has been derived from (7.3) and (7.10) since $K_i|_{cell}$ acts on I_o.

$$K_i|_{module} = N_p K_i|_{cell} \quad \textbf{(7.12)}$$

Similarly, the relationship between $K_v|_{module}$ and $K_v|_{cell}$ comes from (7.11) since K_v acts on the voltage V_d to give V_{D1}. The scaling of V_d is therefore incorporated into the factor $K_v|_{module}$.

$$K_v|_{module} = \frac{1}{N_s} K_v|_{cell} \quad \textbf{(7.13)}$$

To permit the series connection of PV module models to form an array the blocks E2 and Bypass are added to the cell model of Figure 7.2 to produce the PV module model displayed in Figure 7.4. Apart from the addition of these blocks the models are essentially the same since it is assumed that the module parameters I_{ph}, K_i, K_v, R_p and R_s, are pre-scaled from cell level or are original module level values taken from a database.

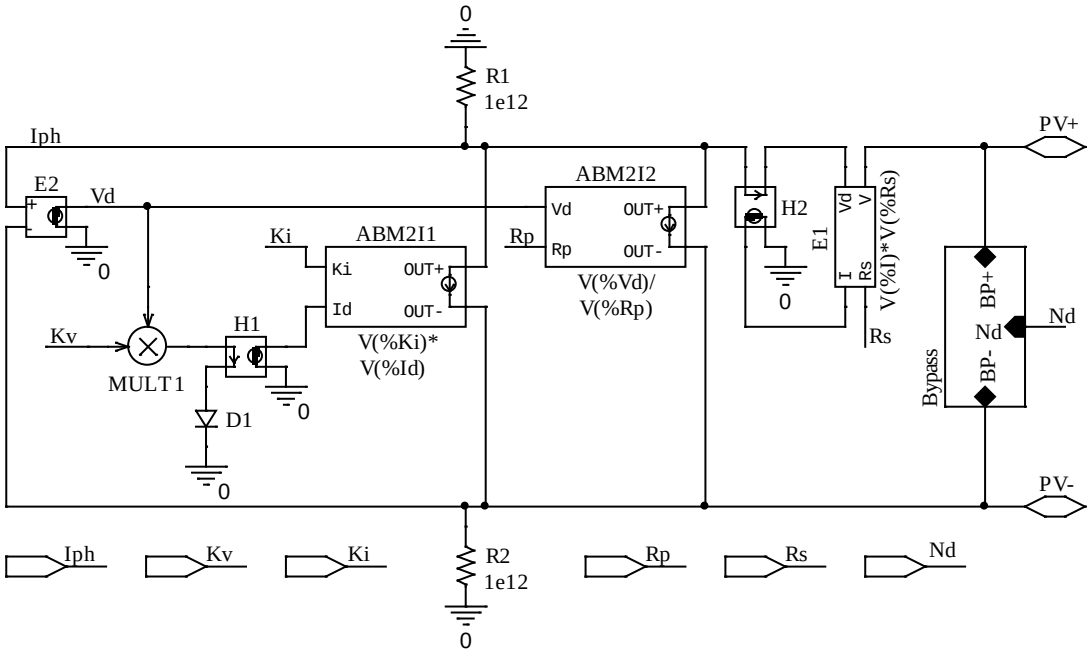


Figure 7.4: PSpice ABM model of a PV module

The ability to connect PV modules in series necessitates the removal of any direct connections to ground from the circuit achieved through the addition of the large

resistances R1 and R2. However, as mentioned previously, the ABM inputs are single ended with reference to ground and so E2 is required for isolation of V_d.

The Bypass block containing the bypass diode model is required to complete the PV module. Control over the number of bypass diodes N_d in the model is desirable since this can vary between PV module models. The bypass diodes are connected across the output so that they are reverse-biased during normal operation. The equation for scaling the PV module output voltage V by the number of bypass diodes N_d is given in (7.14).

$$V_{bypass} = \frac{V}{N_d} \qquad \textbf{(7.14)}$$

The developed bypass diode section is displayed in Figure 7.5, where the generic PSpice diode model D2 is used to represent a single bypass diode. ABM3_2 uses 2 of its single ended inputs to obtain V as a differential voltage which is then divided by the 3rd input N_d. The resulting V_{bypass} is dropped across D2. The CCCS block F1 draws the bypass current from the PV module output whilst isolating the ground connected D2.

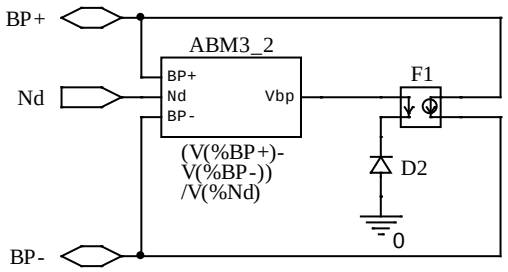


Figure 7.5: Bypass diode section of PV module ABM model

To reduce the visual complexity, a PV array model can be constructed as a PSpice hierarchical design. This approach is demonstrated in Figure 7.6 with a PV array of 2 series connected PV modules. It has the additional benefit of only requiring construction of a single PV module model schematic that can have numerous references from the

array schematic as hierarchical blocks. This 'black box' method provides the required flexibility in the size and configuration of the model.

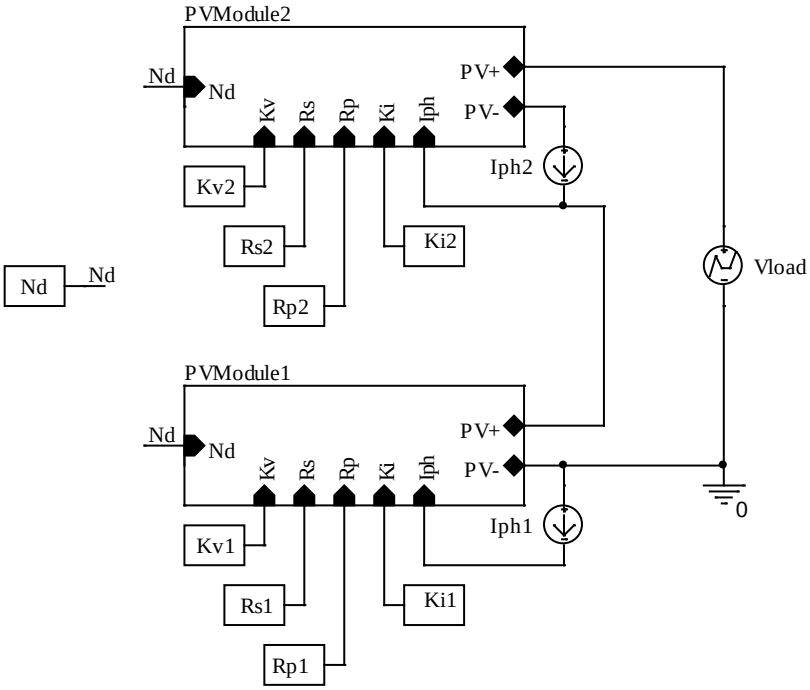


Figure 7.6: PSpice hierarchical design for a PV array

Each PV module block accepts controllable model parameters and gives a 'floating' electrical output to allow series connection. The output is not strictly floating since both the output rails have been tied to ground through large value resistances to allow the PSpice simulation to run.

The hierarchical PV array model in Figure 7.6 was used to simulate 2 series connected BP7175S PV modules. The PV module 1 parameters were set to standard test conditions (STCs) whereas the PV module 2 parameters were set to half the irradiance of PV module 1. The load voltage was varied from 0V to V_{oc} to obtain the PV array I-V characteristic. The results of the simulation are displayed in Figure 7.7. The results indicate that the bypass diode model functions correctly as bypass diode 2 starts to conduct when I exceeds I_{sc} of PV module 2.

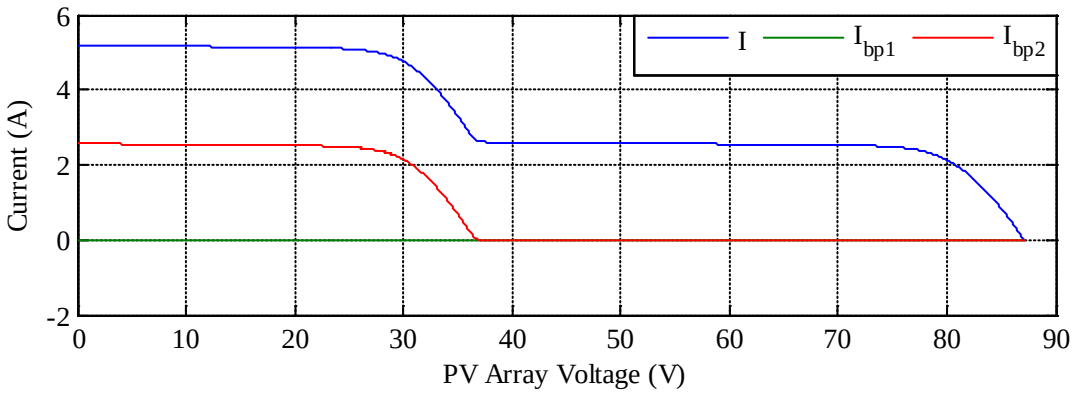


Figure 7.7: Simulation results of PV array model with $G_2 = 0.5G_1$

7.2 Simulation of PCDs

To enable simulation of a DMPPT PV system, PCD models are required in addition to the PV models presented in Section 7.1. PSpice is used again for the simulation as this allows generation of an electrical representation that can be combined with the developed PV models. A PSpice model also provides the option to link through SLPS to a Simulink simulation of the MPPT algorithms. This is beneficial as Simulink is more suited to simulating an MPPT controller than PSpice.

This section presents the development of a PSpice SolarMagic (SM) model and a Simulink MPPT model. The models are combined using SLPS to obtain simulation results that can be compared with the experimental results in Chapter 6. The development of a PSpice model for an SB700 inverter is described and the results from co-simulating with the Simulink MPPT model, modified for the SB700, are displayed. These models provide the 'building blocks' to form simulations of DMPPT systems and investigate MPPT controller interactions.

7.2.1 SM ‘Switching Model’

In Chapter 6 experimental data for the SM DC power optimiser is presented along with a derived specification for the operational parameters. In [47] the SM power electronics circuit is shown as a buck-boost converter based on 4 switches as displayed in Figure 7.8.

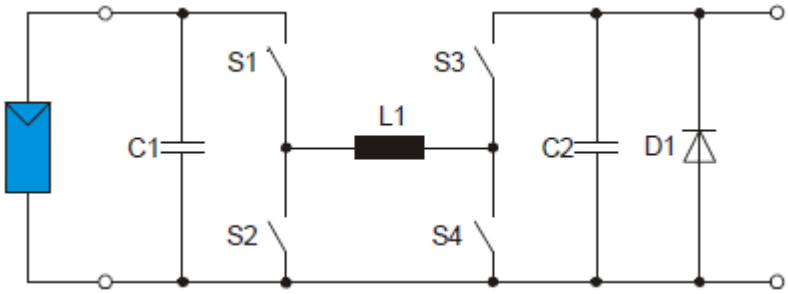


Figure 7.8: Power electronics circuit for the SM SM1230 [47]

A PSpice switching model based on this circuit of an SM was initially developed to replicate the results in Chapter 6. However, a switching model is limited due to the maximum simulation time-step of the model for accurately replicating the switching frequency. Such a small time-step produces far more samples than are needed to reproduce the overall dynamics of the MPPT system. The excessive amount of samples would also result in a longer real-time simulation duration which would make the model cumbersome when investigating the interactions in a DMPPT system.

7.2.2 SolarMagic ‘Block Model’

The purpose of developing the DMPPT system model is to investigate interactions between MPPT controllers. It is assumed that the SM would use a filter for rejection of noise and to remove the high frequency ripple before applying the MPPT. The switching of the power electronics has therefore been neglected and the ‘block model’ presented in Figure 7.9 was constructed based on the modelling described in [41].

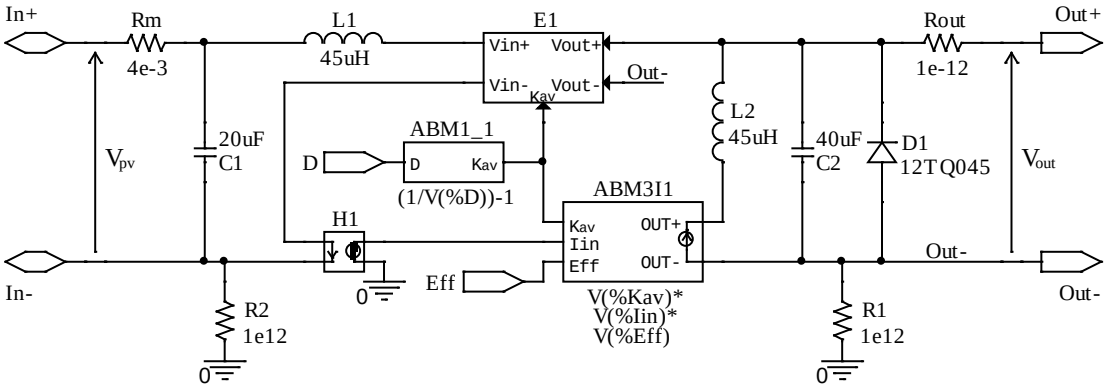


Figure 7.9: SM block model

The block model approach applies the averaged equation for the voltage gain (K_{av}) of the converter as given in (7.15) through the PSpice ABM block ABM1_1.

$$K_{av} = \frac{1}{D} - 1 \qquad \textbf{(7.15)}$$

The block E1 multiplies the output voltage (V_{out}) by K_{av} to obtain the PV voltage (V_{pv}) at the input. The gain K_{av} is applied directly to the voltage conversion to simplify the determination of the duty cycle (D). The efficiency (Eff) of the circuit is included as a factor applied to the current conversion by ABM3I1. This block multiplies the input current (I_{in}) by K_{av} and Eff to obtain the appropriate output current (I_{out}).

Although the switching has been removed the energy storage components of the circuit are maintained, along with the bypass diode, as they may have an effect on the MPPT algorithm. The buck-boost circuit in Figure 7.8 can be considered as 2 circuits, one that charges the inductor from the PV input when S1 and S4 are on, and another that discharges the inductor into the output when S2 and S3 are on. The inductor therefore operates in both the input and output circuits. Since the ABM blocks used in the block model electrically isolate the input and output of the circuit an inductor has been included on both sides. The isolation between input and output also allows a direct connection to ground on the input side.

The resistor R_m was observed in the physical circuit and is assumed to be the current sensing resistor for the SM control circuits whereas the resistor R_{out} has been added to allow a value for I_{out} to be obtained from the PSpice simulation. The hierarchical block models for the PV module and SM were combined to simulate the SM tests using a solar emulator. The model displayed in Figure 7.10 was used to simulate the test case of I_{sc} = 1A, R_{load} = 4.1Ω and includes a blocking diode (D1) as recommended by the SM manufacturer. Using a component analyser the inductance of the wound load resistor was found to be around 10µH.

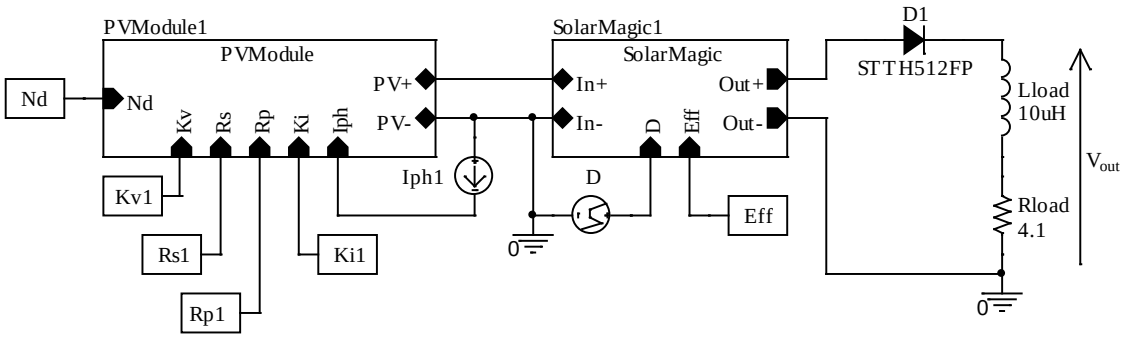


Figure 7.10: PSpice simulation of SM test using a solar emulator

In the model of Figure 7.10 Eff is supplied by a CONST block the value of which was set to 0.94 as described in Chapter 6. An initial run of the PSpice model was performed using the values for D presented in the experimental results of Chapter 6. The resulting SM voltages are compared to the filtered test data in Figure 7.11.

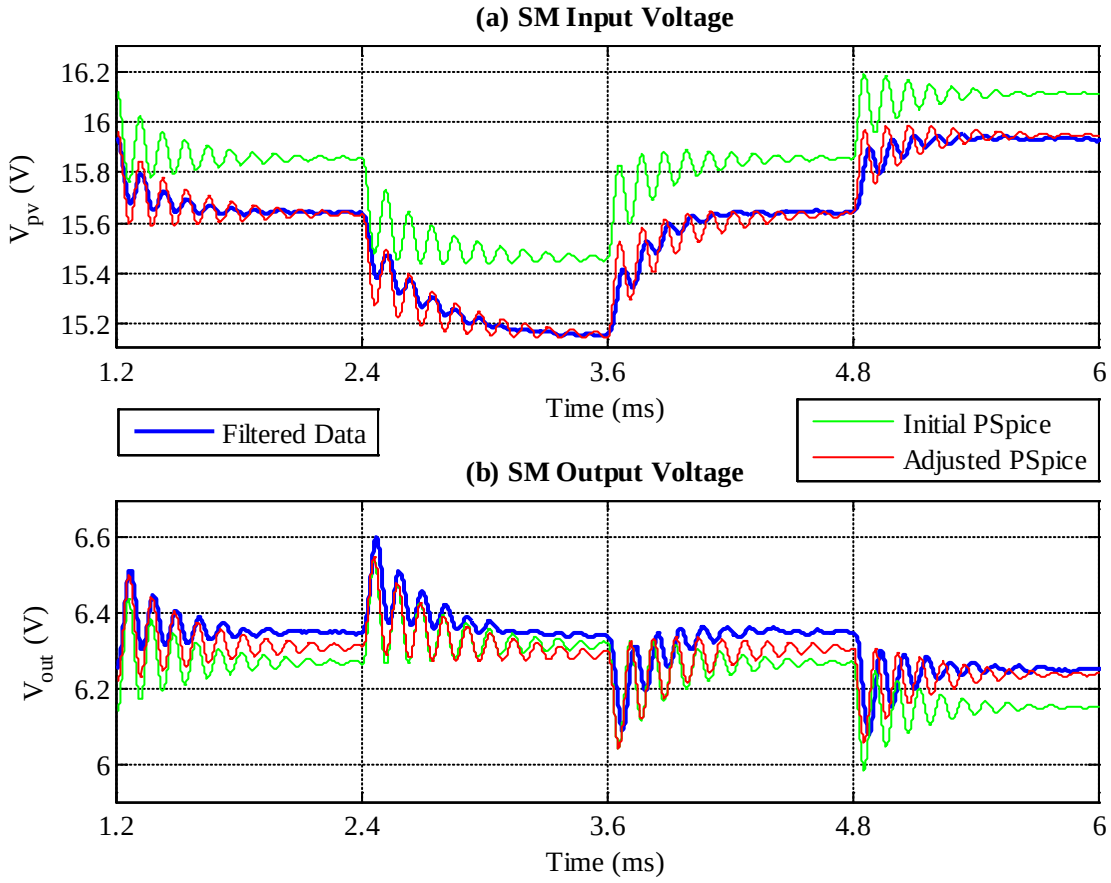


Figure 7.11: Comparison of SM voltage waveforms

It can be seen that the SM V_{out} waveform of the initial PSpice simulation is close to the real data. However, the simulated V_{pv} is too high. The values of D are adjusted to those in Table 7.2 to give a closer match for both V_{pv} and V_{out}.

Period (ms)	D (%)
2.4 – 3.6	34.48
3.6 – 4.8	33.83
4.8 – 6	33.18

Table 7.2: Adjusted values of D

The corresponding current waveforms of the SM from the adjusted simulation are plotted with the measured data in Figure 7.12. Graph (a) shows an inaccuracy of the PV model used in the simulation since I_{pv} is too high whereas V_{pv} in graph (a) of Figure 7.11 has been matched closely. However, the PV model parameters were

extracted from the fitting of the I-V curve where the switching ripple and dynamic ringing of the SM make it challenging to see the true PV operating points.

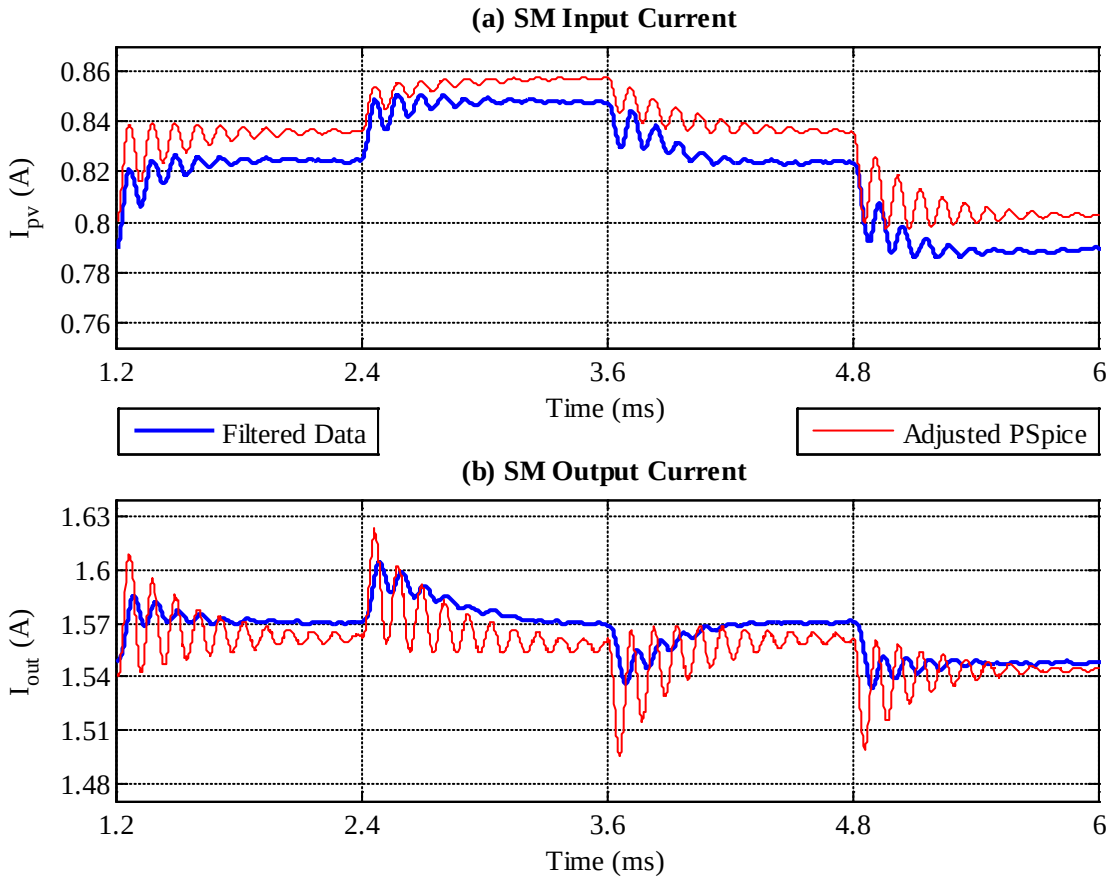


Figure 7.12: Comparison of SM current waveforms

As mentioned, it is the purpose of developing the DMPPT system model to investigate interactions between the MPPT controllers. Although there remain slight inaccuracies in the block model representation of the PV module and SM, the overall performance has shown an adequate reproduction for this purpose.

7.2.3 Simulink Model of an MPPT

The previous subsection described the development of a PSpice block model representation of the SM power electronics for use in simulating a DMPPT system consisting of a number of DCPOs. Each DCPO attempts to keep its corresponding PV module at the MPP, even if the PV array is subjected to mismatch conditions.

This subsection provides details of a Simulink model of an MPPT that can be combined with the PSpice SM block model using the co-simulation software SLPS from Cadence. A Simulink MPPT model is used as it is better suited for simulation of controllers than PSpice. It also enables variables created in MATLAB programmes, such as the extracted PV parameters, to be passed to the simulation directly from the MATLAB workspace and vice-versa.

To avoid numerous signal lines, extensive use is made of the signal multiplexing and de-multiplexing facilities in Simulink, shown as bars with multiple signals on one side and a single signal on the other. When co-simulating Simulink and PSpice it is only possible to include one SLPS block that accepts a single input and returns a single output signal, both of which can be multiplexed, as shown in Figure 7.13.

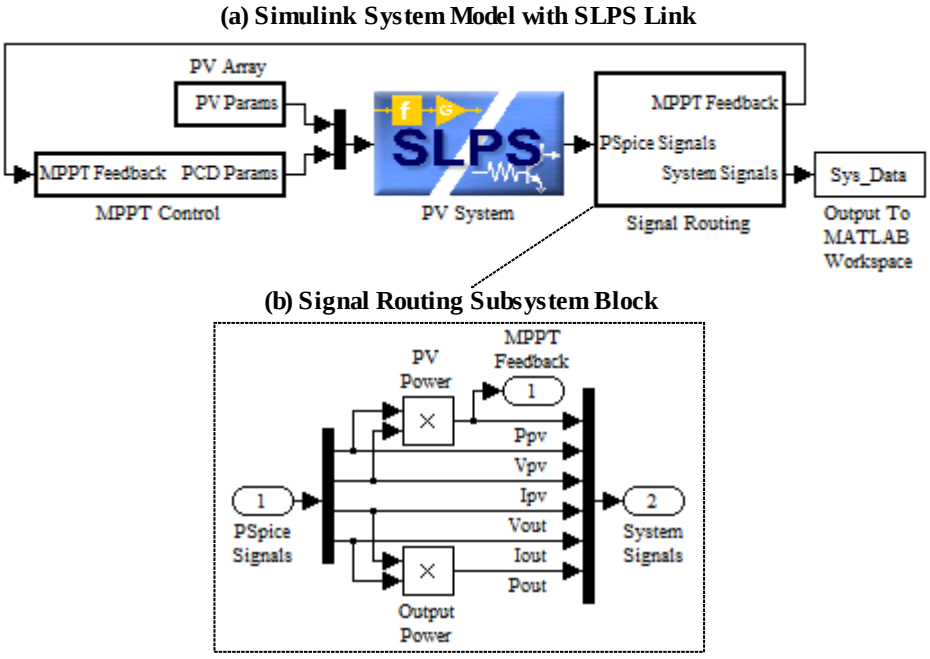


Figure 7.13: Simulink system model for SM test

The PV array model parameters and PCD model parameters are multiplexed for passing to PSpice through the SLPS block ‘PV System’ whilst the signal returned by PV System requires de-multiplexing into the individual signals by the ‘Signal Routing’ subsystem

displayed in (b). Any derived signals are also calculated in this subsystem before the appropriate signals are stored in the MATLAB workspace and, if required by the MPPT algorithm, fed back to the block 'MPPT Control' as indicated by (a).

The MPPT algorithm used in the model is the perturb and observe (P&O) routine as outlined in Table 7.3, shown earlier in Chapter 2. A perturbation of the duty cycle D is implemented and the consequential change in PV power is observed to determine the next perturbation required to track the MPP.

Perturbation	Change in Power	Next Perturbation
Positive	Positive	Positive
Positive	Negative	Negative
Negative	Positive	Negative
Negative	Negative	Positive

Table 7.3: Summary of hill-climbing and P&O algorithm

To utilise the PV power (P_{pv}) in the MPPT algorithm it is passed from Signal Routing to the 'MPPT Control' subsystem as the 'MPPT Feedback' signal shown in Figure 7.14 (a). To execute the P&O algorithm, MPPT Control first determines the change in power using the 'Sign(dP) Calculation' subsystem of (b).

To reduce the effect of the SM dynamics from the PSpice model P_{pv}, the sampled signal P_s is passed through a digital low-pass filter. To obtain the change in power, the filtered signal is measured giving P1 and the difference with a previously stored value P2 is calculated. Since only the direction of P_{pv} is required the magnitude of the difference is set to 1 by the 'Sign' block.

Once the direction of the power has been observed, MPPT control calculates the next perturbation in the duty cycle ΔD and applies it to the duty cycle D using the 'D Calculation' subsystem of (c).

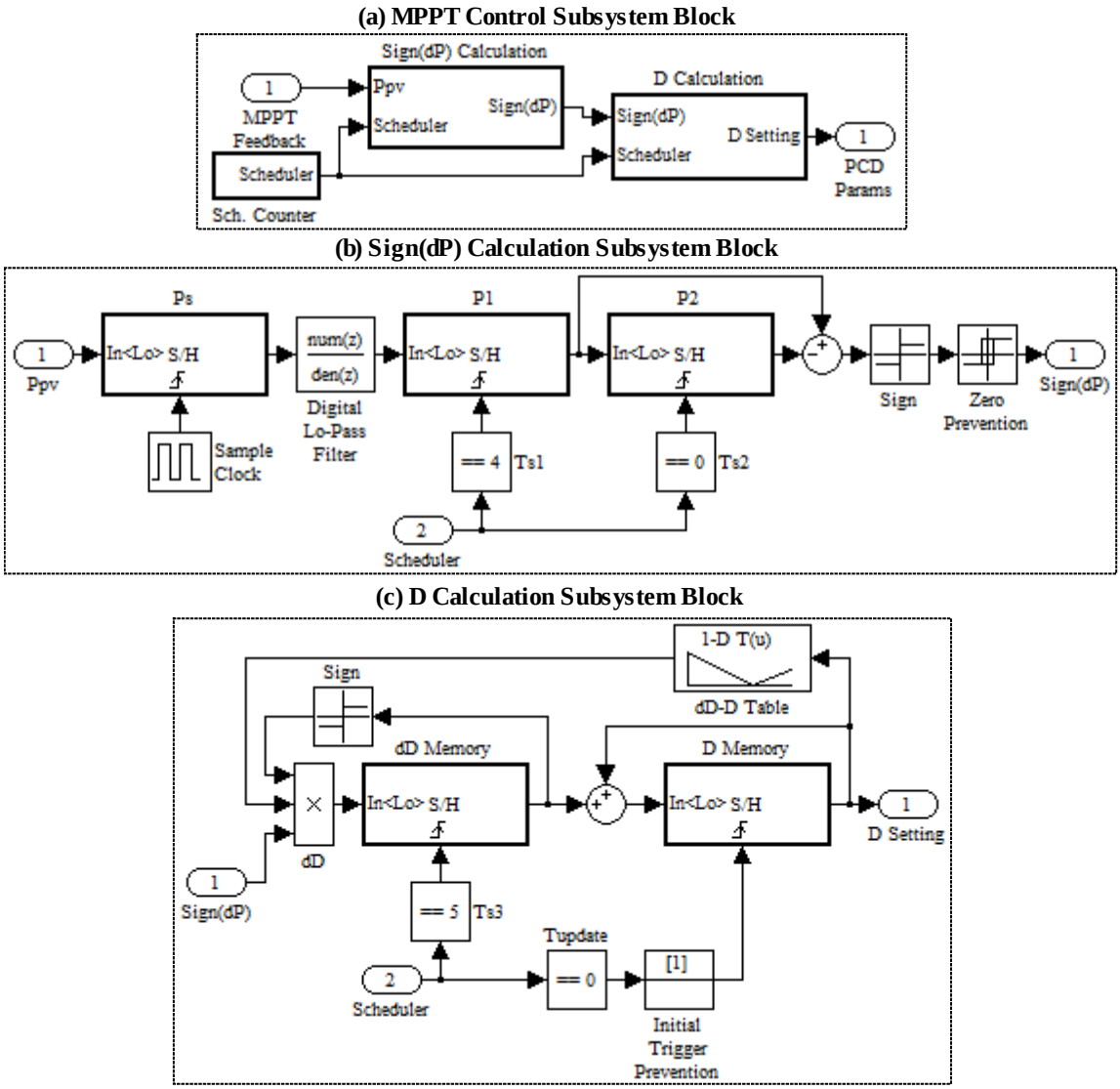


Figure 7.14: Simulink MPPT model for SM test

To find the next ΔD value, the sign of the previous ΔD, stored in 'dD memory', is multiplied by the sign of the power change Sign(dP) and the required magnitude of ΔD. To avoid getting stuck at a point where the power change is zero, the relay action 'Zero Prevention' is employed in Sign(dP) Calculation to ensure that a non-zero value of ΔD is generated.

A distinct relation between the value of D and the magnitude of ΔD is described in Chapter 6 and applied in the model using the lookup table 'dD-D Table'. To realise the

next perturbation and update the value of D, the present value stored in ‘D Memory’ is summed with ΔD.

Due to the necessity of accurate timing for the P&O sequence the MPPT processes are controlled by the block ‘Schedule Counter’. To produce the timing diagrams of Figure 7.15 the timing sequence described in Table 7.4 is applied on the transition edges of Schedule Counter. No action is taken on the first 3 transitions ensuring the filtered power signal P_{filt} settles before the measurement P1 is taken on the 4th transition.

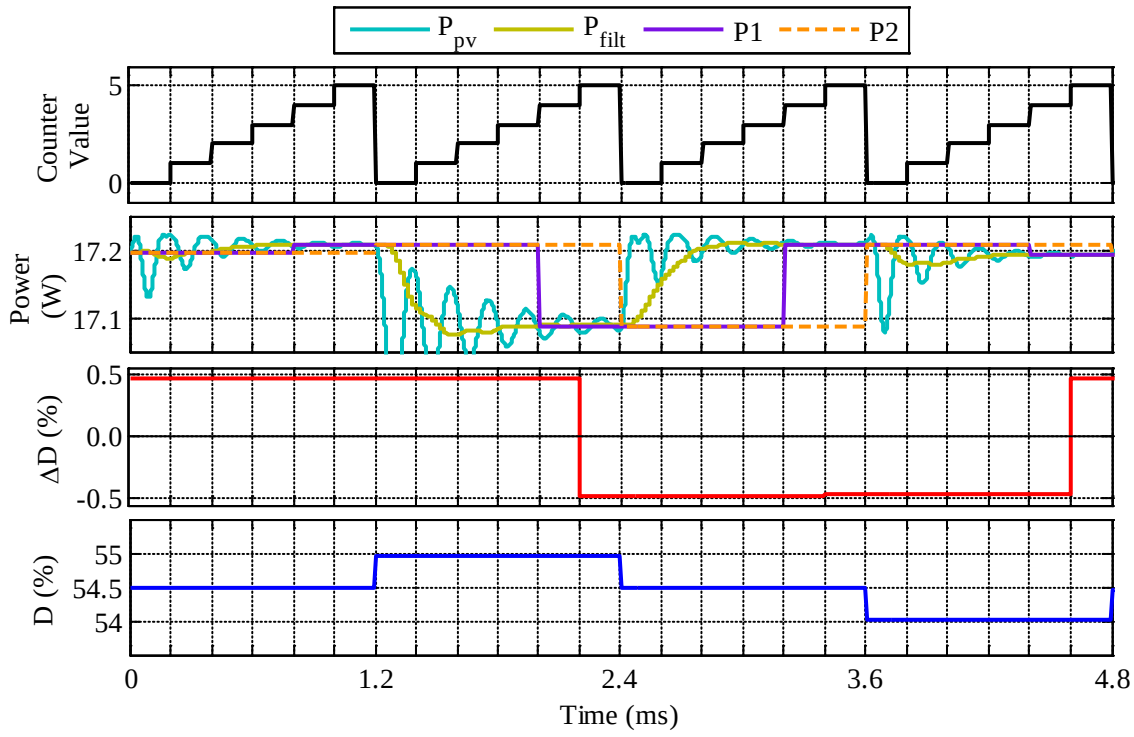


Figure 7.15: Timing of SM MPPT scheduler

Counter Transition	MPPT Actions
5 → 0	Update and store D Store previous power (P2)
0 → 3	Wait
3 → 4	Sample instantaneous power (P1)
4 → 5	Calculate and store ΔD

Table 7.4: SM MPPT timing sequence

Since the MPPT model was used for simulating the SM start-up test, constant values were used for the PV parameters. To investigate DMPPT systems the model can be

expanded to account for the environmental dependencies of the PV module parameters described in Chapter 2.

The developed Simulink MPPT model was co-simulated with the PSpice model of the practical SM MPPT test displayed in Figure 7.16. For verification of the co-simulated model the simulation results are plotted with the results of the experimental setup of Figure 7.16 (b) in Figure 7.17.

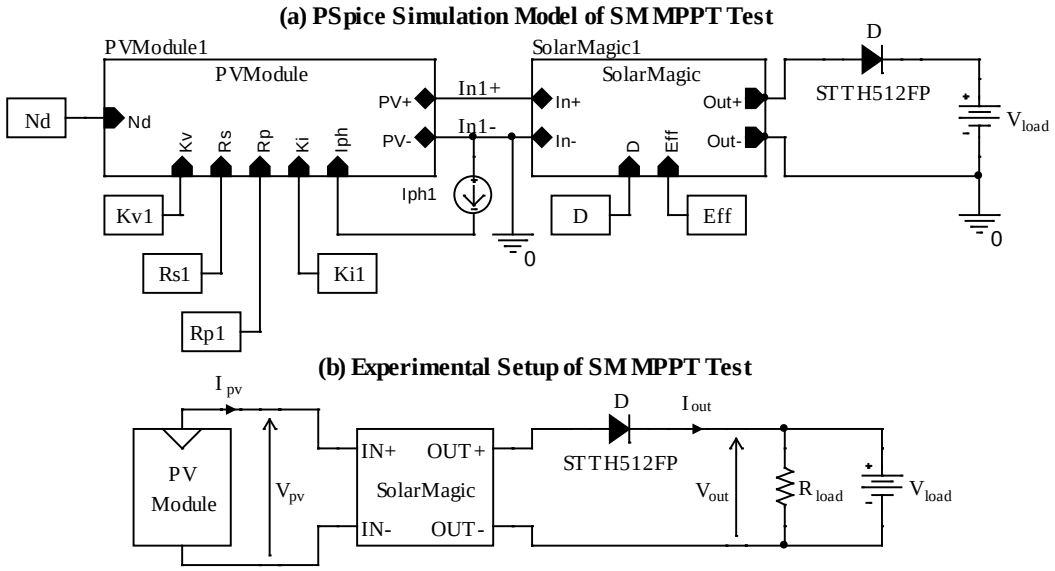


Figure 7.16: System for SM MPPT test

The waveforms in Figure 7.17 demonstrate that the model response is very close to the real system. A stable MPPT algorithm is indicated by an MPPT pattern in which P_{pv} changes direction at twice the frequency of the V_{pv}, as seen in both the experimental and simulation results. Since it is difficult to see the change in P_{pv} for the simulation results during the steady state operation (>8.4ms), the magnified plots of V_{pv} and P_{pv} are displayed in Figure 7.18 with the stable MPPT operation clearly indicated.

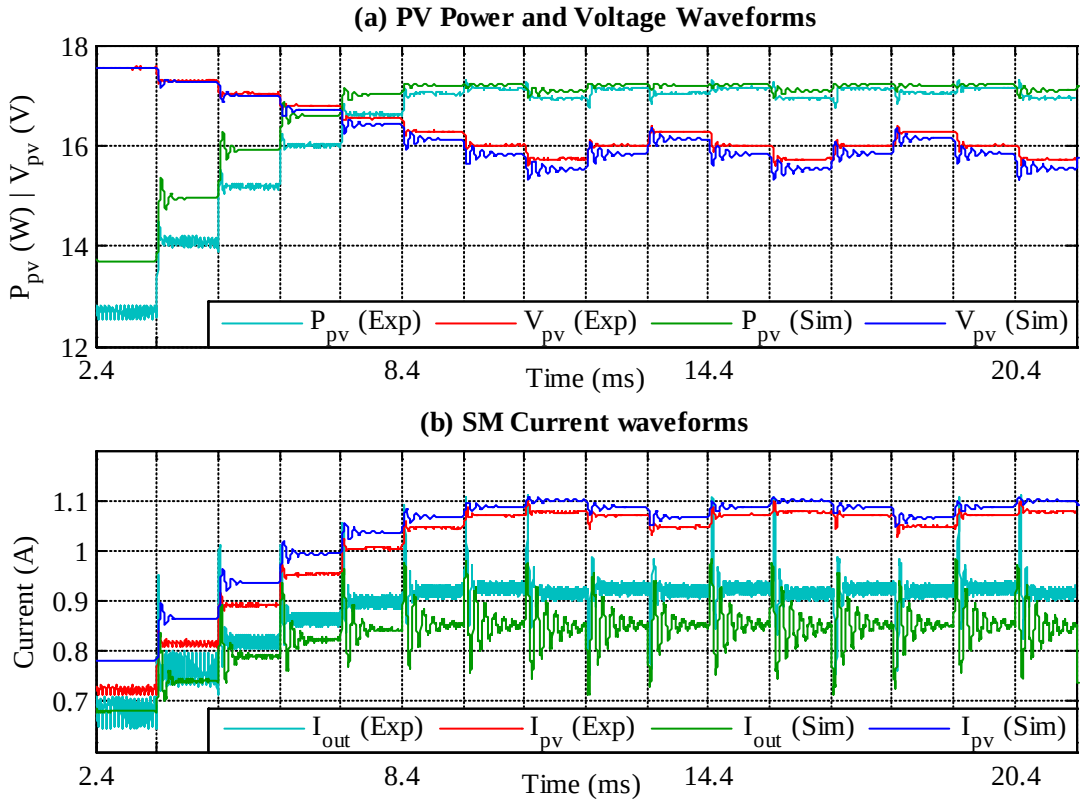


Figure 7.17: Results for SM MPPT test

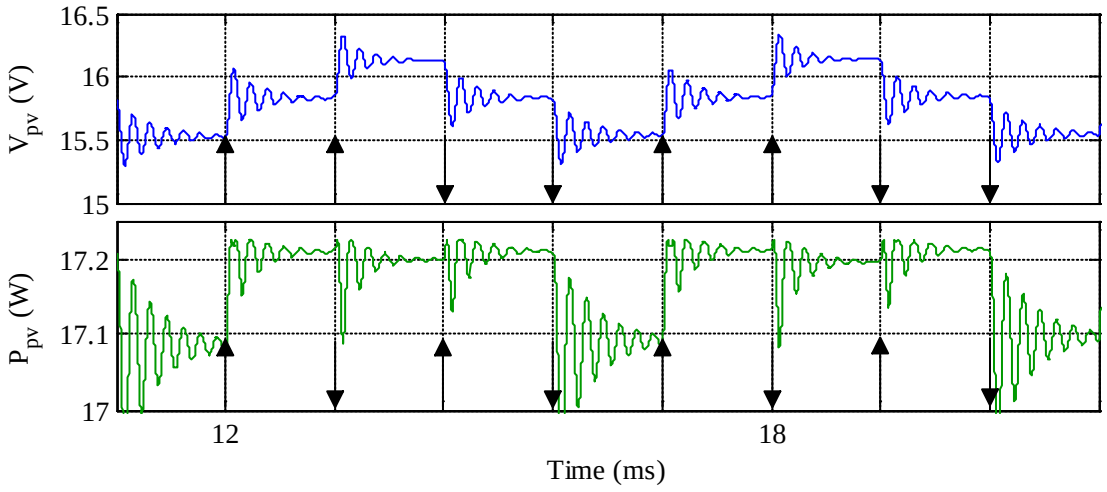


Figure 7.18: MPPT patterns in PV voltage and PV power

The trajectory of a stable MPPT about the MPP on the P-V characteristic is illustrated in Figure 7.19. Starting at the operating point of lowest V_{pv}, a positive ΔD is applied causing an increase in V_{pv} and P_{pv}, as indicated by the solid arrows. Since a rise in P_{pv}

was observed after the first positive perturbation a second positive ΔD was applied. This time P_{pv} decreases as V_{pv} increases since the operating point has passed the MPP.

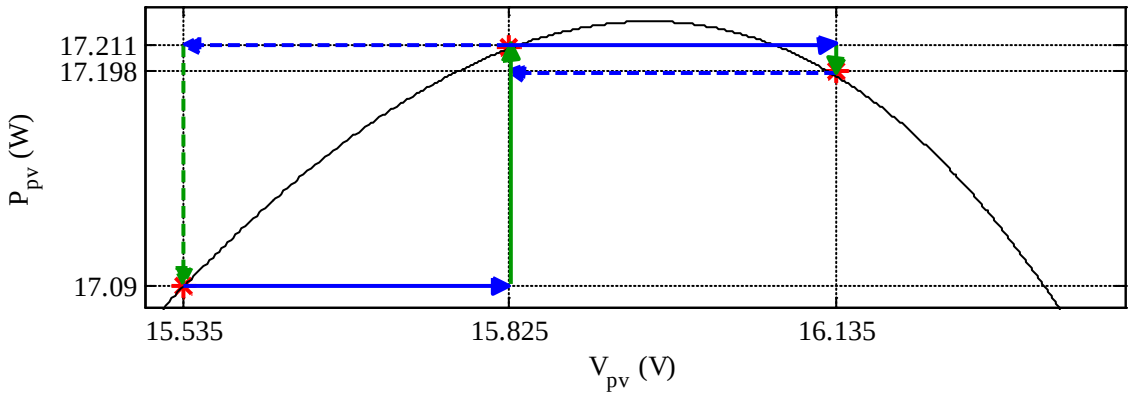


Figure 7.19: P-V characteristic of start-up simulation showing MPPT trajectories

The following ΔD therefore becomes negative and the MPPT returns to the previous operating point of higher P_{pv} as indicated by the dashed arrows. Since there was a rise in P_{pv} a continuing negative ΔD returns the MPPT to the original operating point. The fall in P_{pv} reverses the direction of D and the cycle starts again. Thus the direction of P_{pv} changes at twice the rate of V_{pv}.

Some minor differences can be observed between the simulated waveforms and experimental waveforms in Figure 7.17. These are largely due to small inaccuracies in the models described in the previous subsections as well as some approximations used in the MPPT model as described in Chapter 6. However, the results have demonstrated that when combined, the Simulink MPPT model, PSpice PV model and PSpice SM model represent a stable and realistic model that is adequate for use in investigating DMPPT systems.

7.2.4 SB700 Model

To complete the DMPPT system a model of a PV inverter is required. A description of a PSpice representation of an SB700 PV inverter and the required modifications to the

Simulink MPPT model established in the previous subsection are given in this subsection.

An initial model was created based on the testing presented in Chapter 6. A system diagram of the test setup of 4 series connected PV modules (BP7175S) and the SB700 inverter is displayed in Figure 7.20. The output of the inverter was connected directly to the AC mains grid.

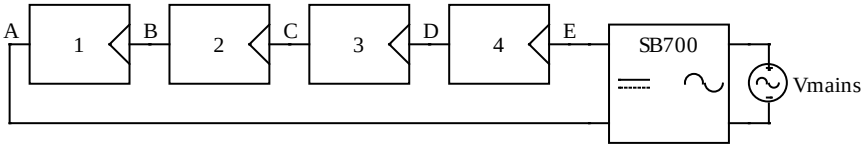


Figure 7.20: System diagram of SB700 test

The developed PSpice reproduction of the system is illustrated in Figure 7.21. The model contains 4 of the PV module hierarchical blocks described at the start of this chapter. These are connected in series using the node alias technique where each node with the same name will be connected in the simulation, e.g. node E on PVModule4 will be connected to node E on SB700.

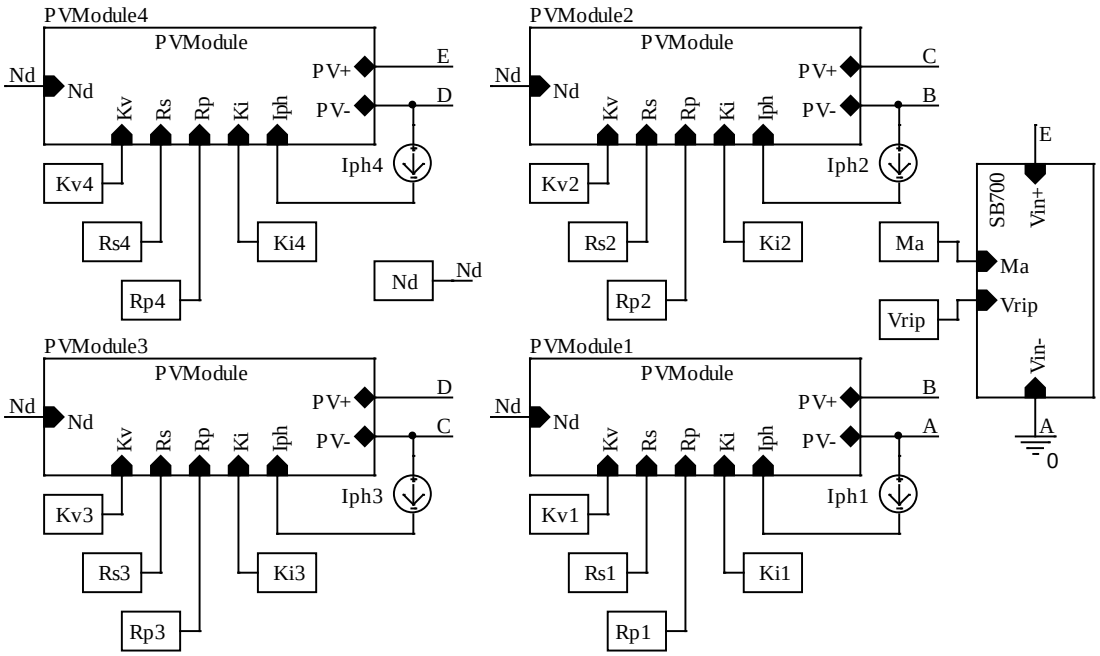


Figure 7.21: PSpice system model of SB700 test

As a reminder, the diagram of the SB700 from Chapter 6 is shown again here in Figure 7.22.

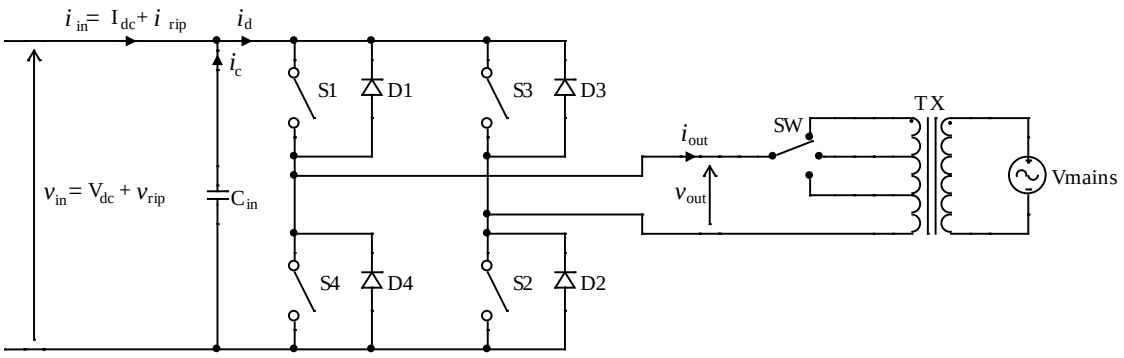


Figure 7.22: SB700 diagram

The relationship between the DC input voltage V_{dc} and the amplitude modulation ratio m_a for the inverter was described in Chapter 6.

$$V_{dc} = \frac{\sqrt{2}V_{mains}}{N_t m_a} \qquad 0 \leq m_a \leq 1 \qquad \textbf{(7.16)}$$

A suitable value for N_t can be calculated from (7.17) using the inverter datasheet values for the maximum rms mains voltage $V_{mains}|_{max}$ and minimum DC input voltage $V_{dc}|_{min}$ at the maximum m_a value of 1.

$$N_t = \frac{\sqrt{2}V_{mains}|_{max}}{V_{dc}|_{min}} \qquad \textbf{(7.17)}$$

To minimise and simplify the equation for V_{dc} the inverter is assumed to operate at $V_{mains}|_{max}$; expression (7.17) for N_t is substituted into (6.3) and a new term M_a is defined as the inverse of m_a which then yields (7.18). The MPPT model for the SB700 applies a perturbation to the new term M_a. To obtain the V_{mpp} operating range of 75V to 150V M_a is varied from 1 to 2.

$$V_{dc} = M_a V_{dc}|_{min} \qquad \textbf{(7.18)}$$

The SB700 hierarchical block in the PSpice system model contains the circuit shown in Figure 7.23. Since the model is to be used for investigating interactions between MPPT controllers on the DC side of the inverter the AC mains is not considered. The block E1 applies equation (7.19) to give V_{dc} across the V_{inv} terminals. A current measurement for the MPPT is provided by the resistor I_{in}.

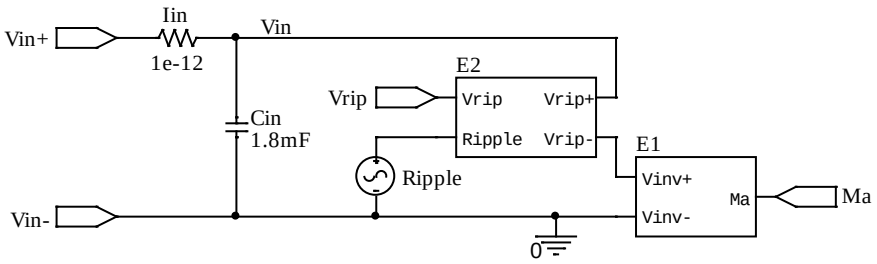


Figure 7.23: PSpice model of an SB700 PV inverter

The 2nd harmonic current ripple drawn by the switching section of the SB700 causes a voltage ripple across the capacitor as described in Chapter 6. This voltage ripple is applied by placing the output of block E2 in series with E1 to produce the sum of the DC inverter input voltage and the 100Hz AC ripple voltage across C_{in}.

To vary the magnitude of the ripple voltage E2 multiplies the 100Hz $1V_{pk}$ AC voltage of the source Ripple by the scaling factor V_{rip}. The approximated dependence of the ripple on the reactance X_c of C_{in}, and the inverter DC input current I_{dc}, as observed in Chapter 6, is maintained in the simulation using equation (7.19), applied through the Simulink MPPT model.

$$V_{rip} = X_c I_{dc} \qquad \textbf{(7.19)}$$

To confirm that the method used for modelling the ripple produces an accurate reproduction, a simulation of the oscilloscope measurements shown in Chapter 6 was run. The PV model parameters were fitted to the measured I-V curves and the ripple

voltage set up to replicate the measured waveform with the results of the corresponding simulation plotted, along with the oscilloscope waveforms, in Figure 7.24.

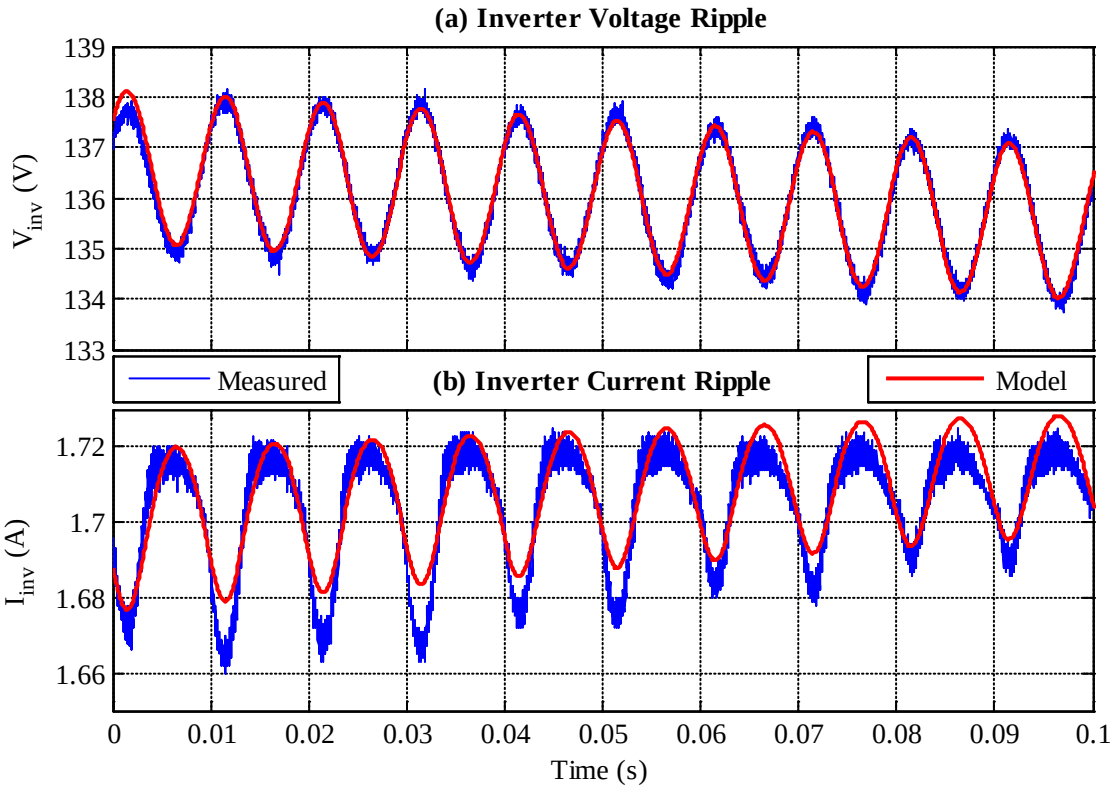


Figure 7.24: Comparison of oscilloscope waveform and PSpice model data for inverter input ripple

The resulting current waveform of the model exhibits a similar pattern to the measured data except with two slight differences: the measured data appears to saturate at 1.72A and has a trough that is lower than the model. The differences arise due to the approximation of the fitted I-V curve (used to extract the model parameters) to the measured data, as indicated in Figure 7.25. The real data has a sharper knee with an almost flat characteristic below V_{mpp}, the saturated part of the waveform, and a steeper characteristic above V_{mpp} that produces the lower troughs.

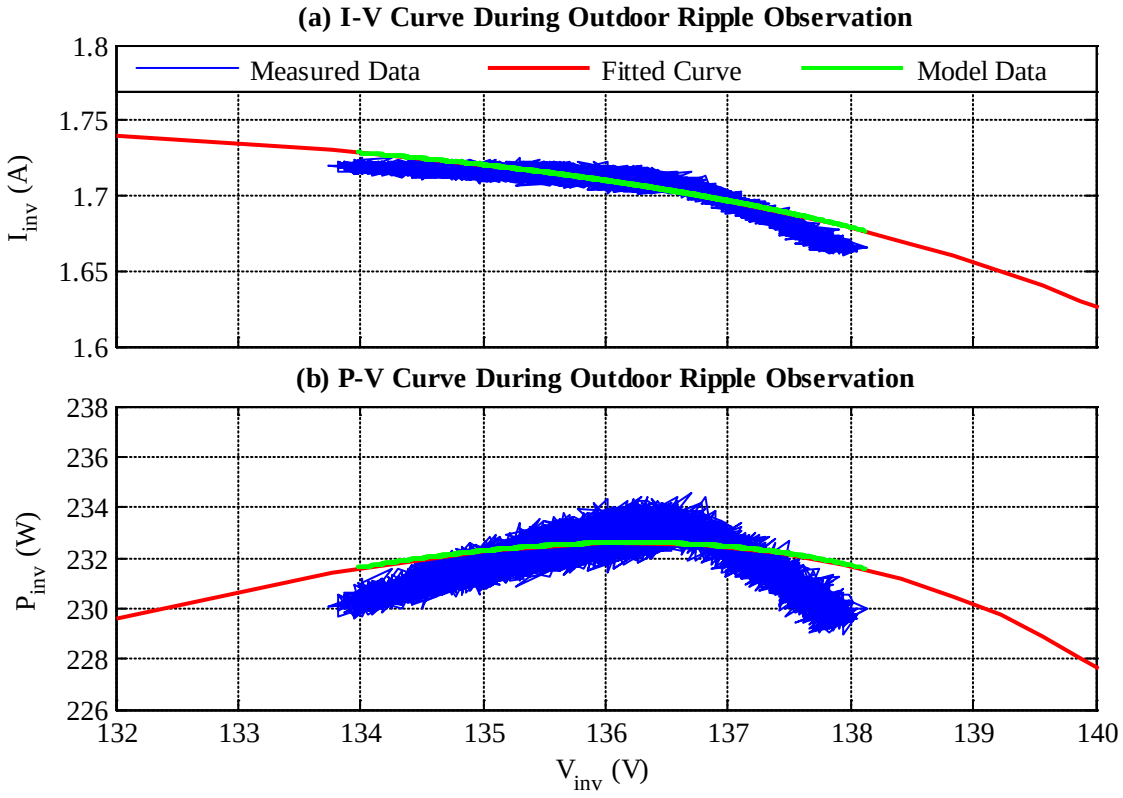
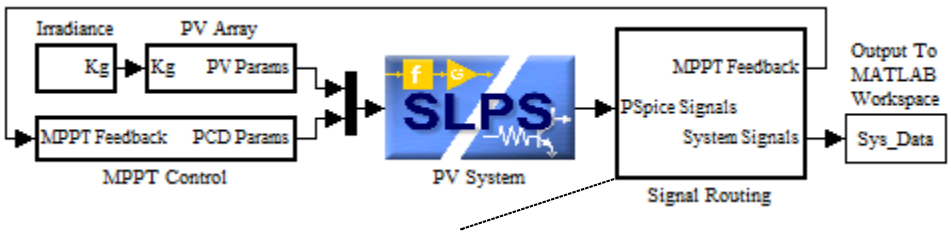


Figure 7.25: PV characteristics for inverter ripple test

To obtain the sharpness required in the knee a 2-diode representation of the PV modules can be used at the cost of extra complexity as described in Chapter 2. However, since the model is used for investigating the interactions between controllers in DMPPT systems the extra accuracy is deemed unnecessary and the combination of the developed inverter and PV models produce a simulation that is accurate enough.

The Simulink model of the MPPT for the SM was adapted for use with the inverter PSpice model. The system model and signal routing are similar except that the PV System SLPS block only returns signals for the inverter input voltage V_{pv} and input current I_{pv} as shown in Figure 7.26. These signals are used to calculate the PV power P_{pv} which is fed back for use in the MPPT algorithm. To calculate V_{rip} the I_{pv} signal is also passed back to the MPPT Control block.

(a) Simulink System Model with SLPS Link



(b) Signal Routing Subsystem Block

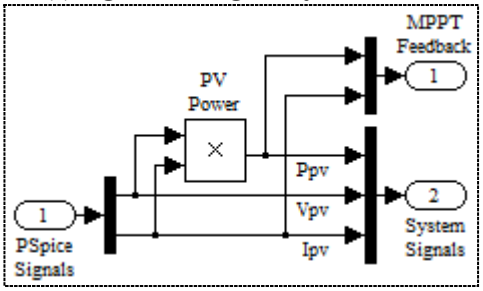


Figure 7.26: Simulink system model for SB700 test

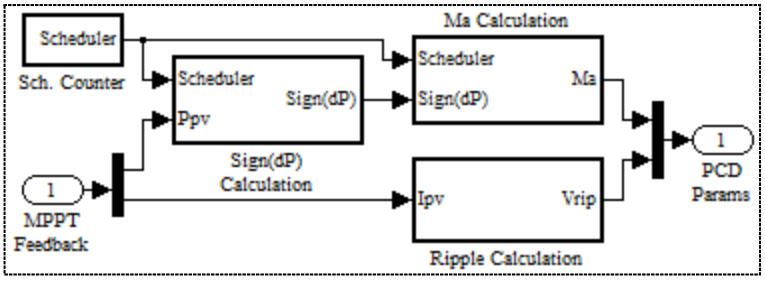
To allow simulation of time varying irradiance, such as the tests of irradiance step in Chapter 6, the PV Array block now accepts an irradiance signal K_g. To minimise the complexity the variation in irradiance is applied directly to the photo-generated current I_{ph} as described by equation (7.20), where K_g is the ratio of the desired irradiance G to the initial reference value G_{ref}.

$$I_{ph} = K_g I_{ph}|_{ref} \qquad \textbf{(7.20)}$$

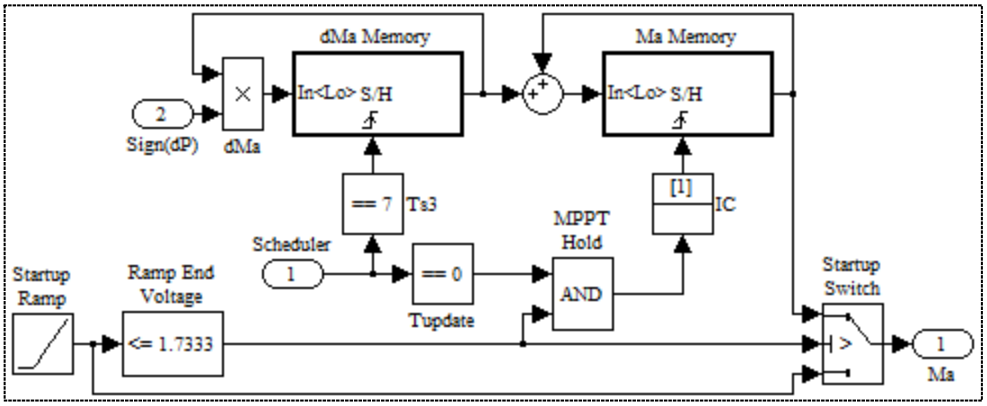
The MPPT Control block of the SB700 is similar to the SM but with the addition of the Ripple Calculation block and the modification of the M_a Calculation block to include the inverter start-up procedure, as shown in Figure 7.27. To simulate start-up a decreasing ramp in M_a is applied until the MPPT start voltage of 130V is reached, as indicated in Chapter 6. On reaching this voltage the MPPT controller is started and the Ma output is switched from the ramp to the MPPT.

To obtain the ripple voltage value V_{rip} the PV current I_{pv} is filtered to leave the DC component I_{dc} to which equation (7.19) is applied. The values of M_a and V_{rip} are then passed back to the SLPS PV System as the PCD parameters.

(a) MPPT Control Subsystem Block



(b) Ma Calculation Subsystem Block



(c) Ripple Calculation Subsystem Block

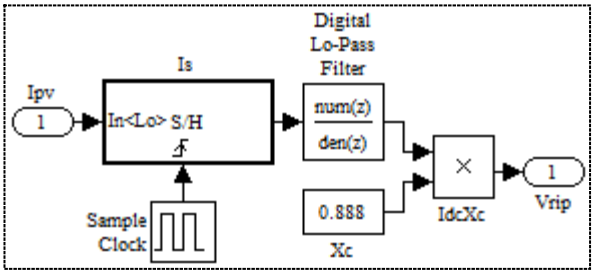


Figure 7.27: Simulink MPPT model for SB700 test

To allow verification of the SB700 start-up procedure the model was simulated with the same system conditions as the experimental results in Chapter 6 with the results displayed in Figure 7.28. It can be seen that the general pattern is similar for the experimental and simulated data but the model appears to have a much larger ripple. This could be due to the sampling of the datalogger that has an average sample time of 45ms with standard deviation of 2.2ms. The corresponding sample frequency of 22.2Hz is too low to properly sample the 100Hz ripple voltage and the variation in the sample time may make the ripple look smaller on the measured data.

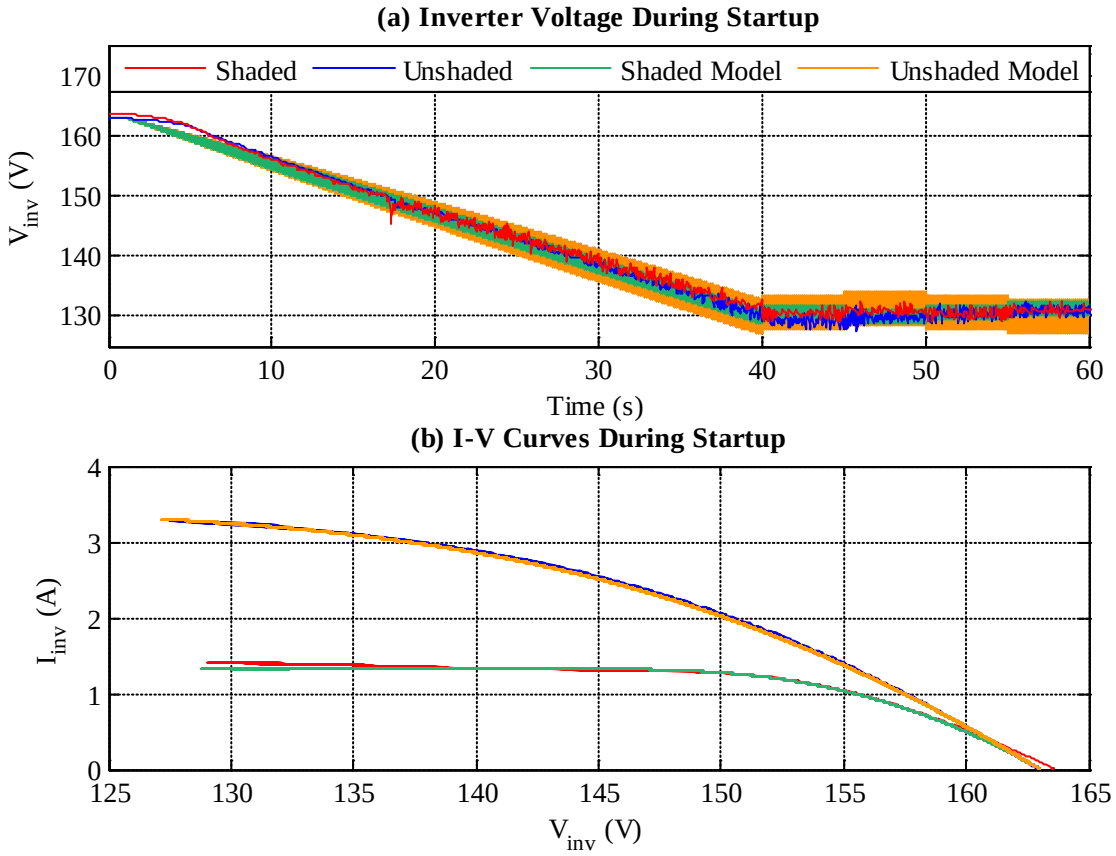


Figure 7.28: Comparison of experimental and simulated data for SB700 start-up

To check the response of the MPPT model to a change in irradiance the tests presented in Chapter 6 were simulated. Since the shading was applied to only half of one PV module the model is modified to represent 3 whole PV modules and 2 half modules to allow a different irradiance for each half.

The simulation results were plotted with the experimental data in Figure 7.29. There were a few minor challenges whilst trying to obtain a model that responded in the same way as the experimental data. Firstly, for a constant irradiance the MPPT should cause a pattern of 'steps' in the power P_{inv} where the average P_{inv} remains constant across an MPPT period. However, it can be seen in plot (b) that leading up to the step change P_{inv} is varying across an MPPT period. The deviation of V_{inv} implies that the ambient

irradiance is varying and so an approximation to the irradiance fluctuations is included in the model.

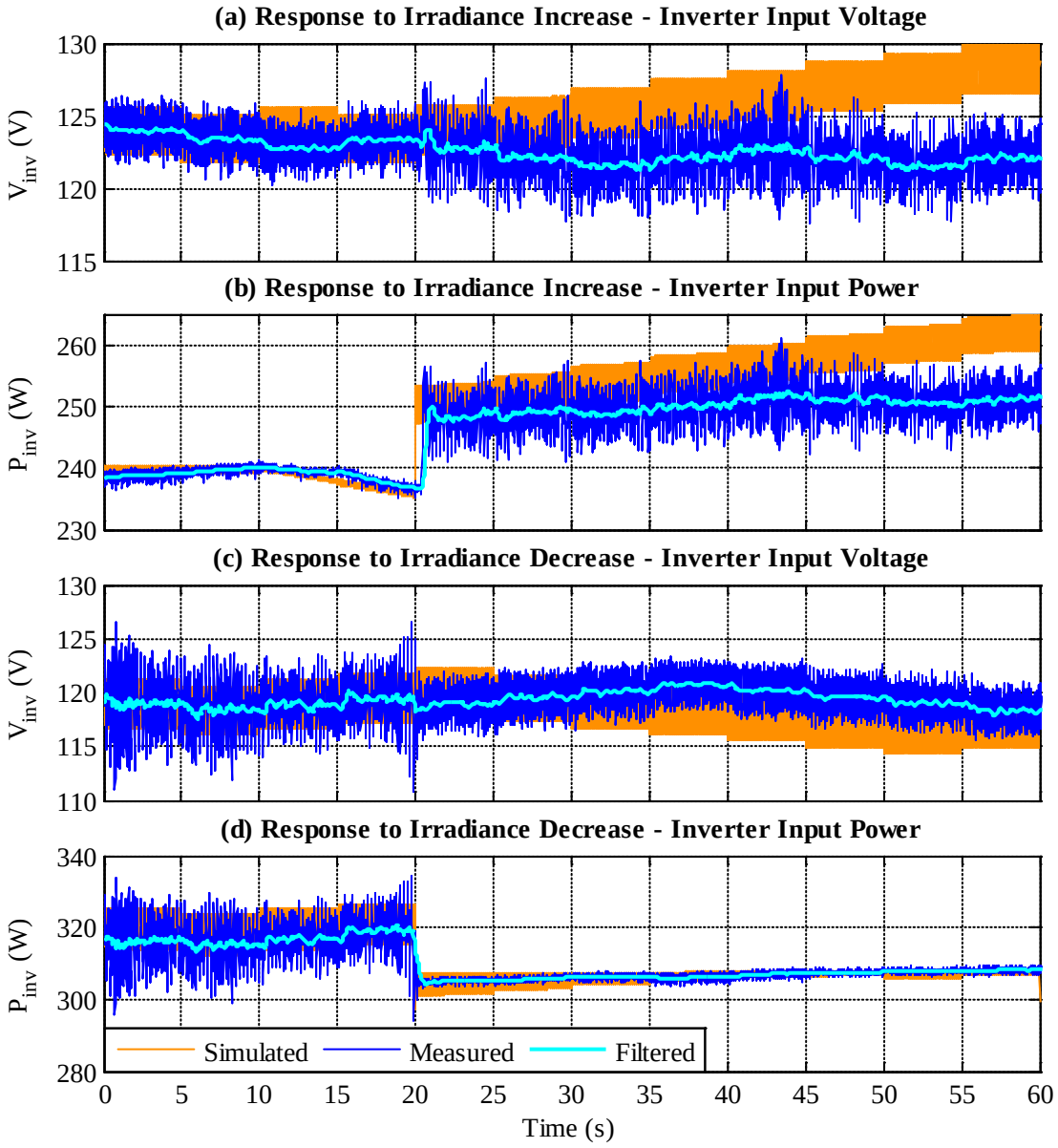


Figure 7.29: Simulation response to a step in irradiance

Also, the MPPT in the experimental setup shows erratic behaviour. For example, in plot (b) P_{inv} appears to have increased from the period of 35s-40s to the following period yet plot (a) shows the direction of V_{inv} changes at 45s suggesting a decrease in P_{inv} had occurred. The discrepancy is likely to be due to real-world disturbances, such as measurement noise, that can't be determined from the experimental results. Since the

model environment is ideal it does not account for such system disturbances and an attempt to include them would be challenging.

However, the model is to be used as part of an investigation into interactions between MPPT controllers in a DMPPT system and so for this purpose the simulation results are acceptably accurate and modelling the discrepancies encountered is deemed unnecessary.

7.3 Simulation of DMPPT Systems

The main objective of this work is to develop a method for investigating any interactions between MPPT controllers in a DMPPT system. The chosen method is the use of a computer model since this offers the greatest flexibility in terms of the simulation conditions and the system configuration.

This section describes the development of such a model through combination of the PV module model, the SolarMagic (SM) power optimiser model and the SB700 inverter model presented in the previous sections. The DMPPT system model is then compared with data from the real DMPPT system presented in Chapter 6. Once verified the model can be used in the suggested DMPPT system investigations detailed in Chapter 8.

7.3.1 DMPPT System Configuration

The developed DMPPT system model is based on the outdoor test rig described in Chapter 6 where four BP7175S PV modules, each with its own SM1230 power optimiser, are connected in series with a blocking diode. The output of the DMPPT system is connected to an SB700 inverter that also has an MPPT. The block diagram of the system is depicted, along with the PSpice model, in Figure 7.30.

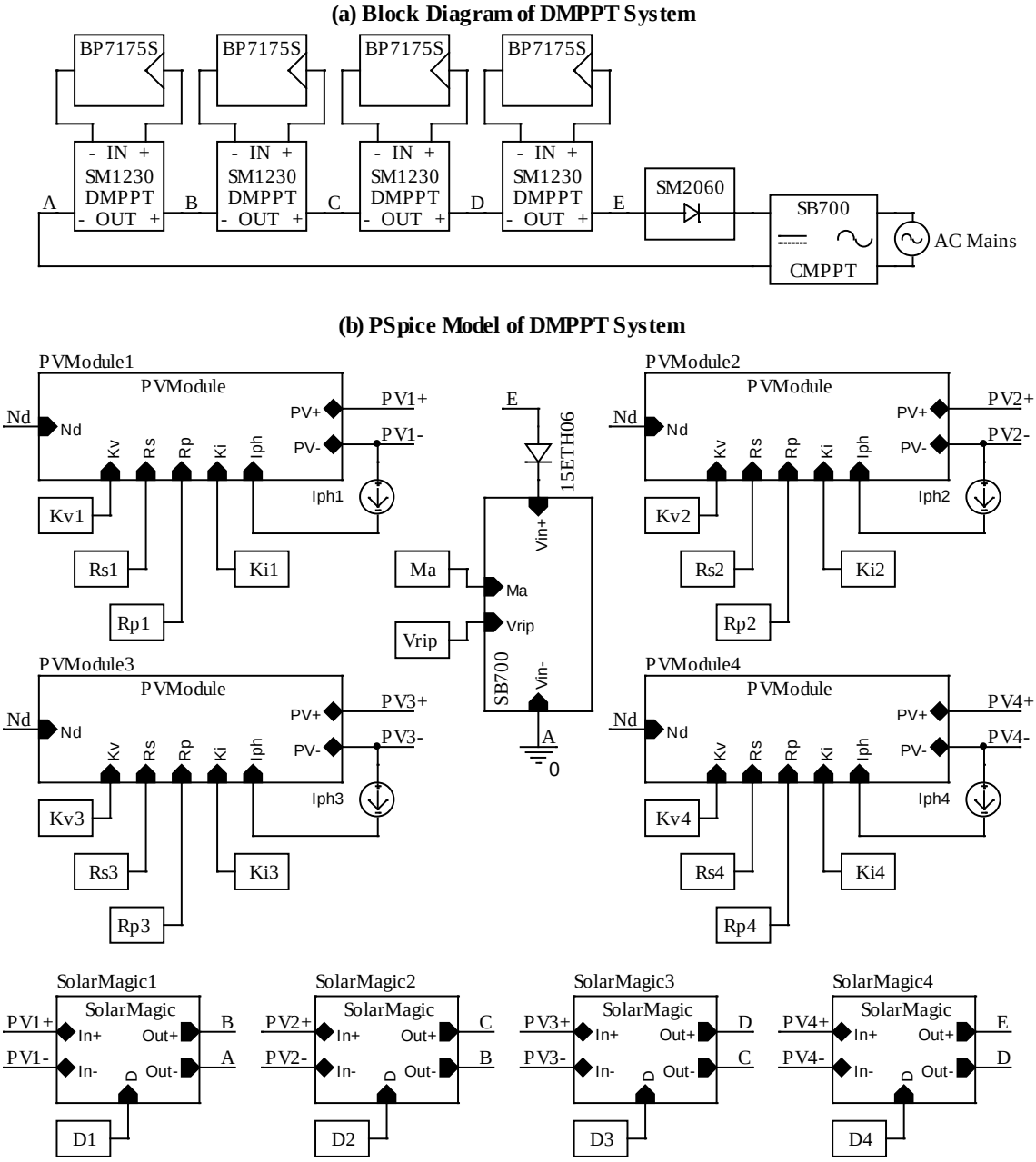


Figure 7.30: Diagrams of DMPPT system

In the previous subsections hierarchical models for each of the system components have been developed except for the blocking diode that can be represented by a PSpice model of a power diode of similar rating, such as the 15ETH06. Since all of the models were developed using hierarchical blocks they are easily combined to create the DMPPT system model shown in Figure 7.30.

To control the MPPTs of the four SMs and the SB700 the Simulink MPPT model is modified to deal with the extra signals, as indicated in Figure 7.31. All of the voltage, current and power signals returned from the PSpice model are passed to the MATLAB workspace. To simulate the MPPTs and inverter ripple the input power of the SMs and the SB700 are fed back to MPPT Control along with the SB700 input current.

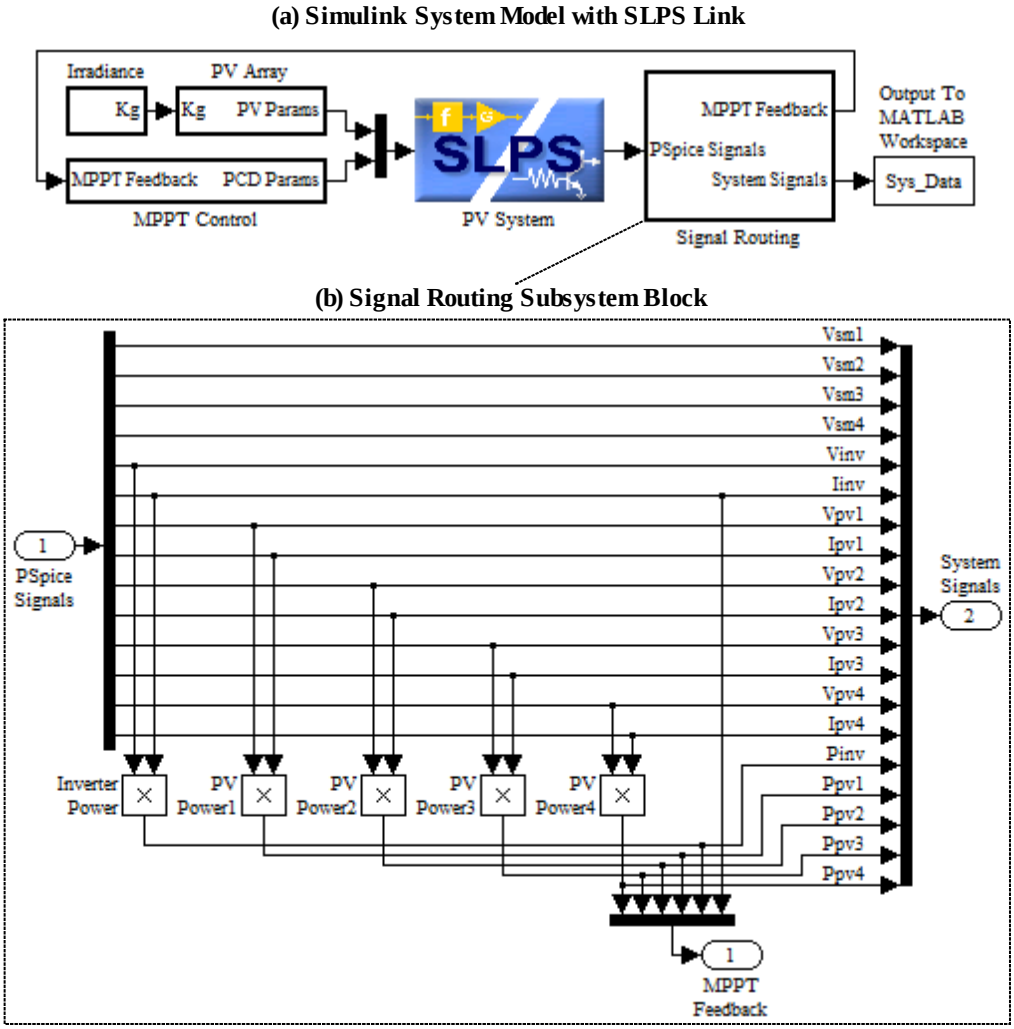


Figure 7.31: Simulink system model for DMPPT test

The MPPT Control subsystem contains the inverter MPPT and ripple calculation blocks as well as an SM MPPT block for each SM, all of which have been described in the previous sections. The output of each block is passed back to the SLPS PV System via the PCD parameters signal as shown in Figure 7.32.

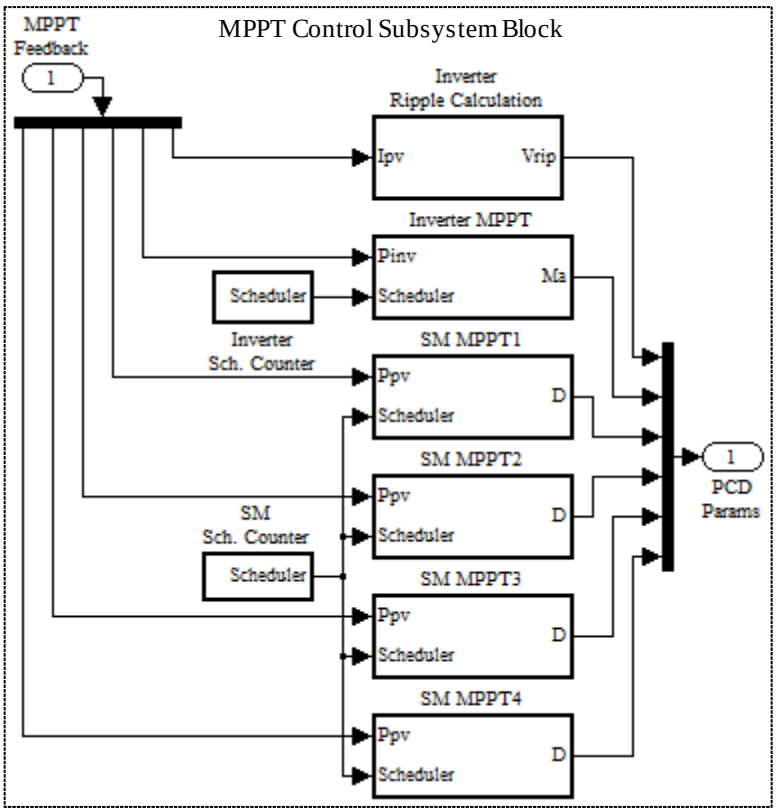


Figure 7.32: Simulink MPPT Control subsystem for DMPPT test

7.3.2 Verification of DMPPT System Model

To compare the DMPPT model behaviour with the real system the two tests of step change in irradiance using SMs were simulated. Due to the fast nature of the SM MPPTs a 60 second simulation would take a long time to execute. Therefore, the simulation has been limited to a 3 second interval centred around the time of the step change in irradiance.

To allow the irradiance change to be applied to half a PV module, the PSpice and Simulink models have been modified as illustrated in Figure 7.33. Two separate PV module models, 4a and 4b, are used to represent each half of PV module 4. To allow a difference in irradiance between them, each half has its own I_{ph} current source. To reduce the complexity of the simulation all other PV model parameters are assumed to be unaffected by irradiance. Because the parameters are applied to half modules, with

half the number of series connected cells, appropriate scaling is used in the PSpice model.

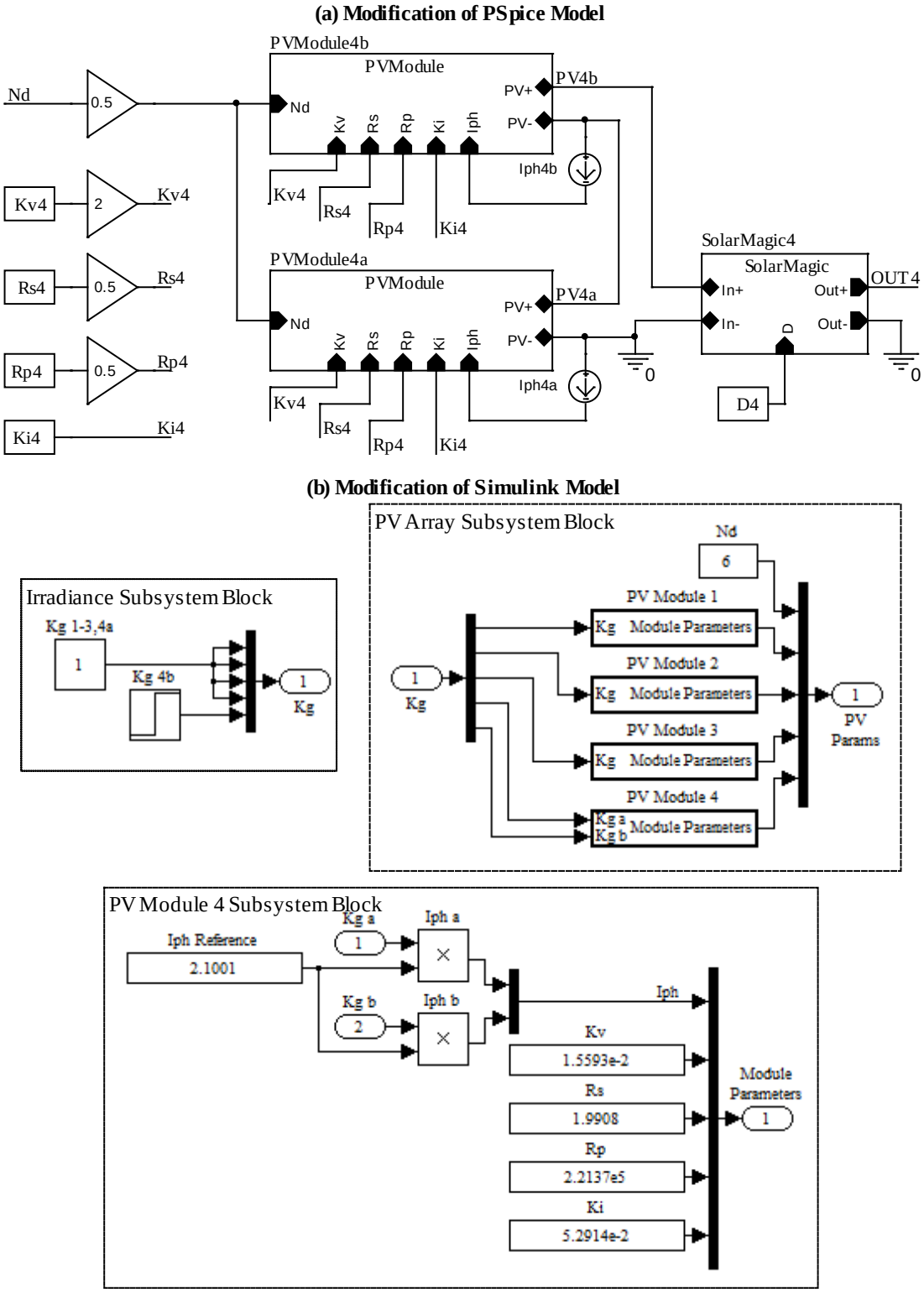


Figure 7.33: Modification of models to create two half PV modules

To observe how the simulation compares with the real system when subjected to a step increase in irradiance the simulated and measured data for V_{pv} was plotted in Figure 7.34. This shows that the overall response of the V_{pv} is similar for the simulation and experimental data. However, in the experimental data there is disturbance before the change in irradiance at 1.5s.

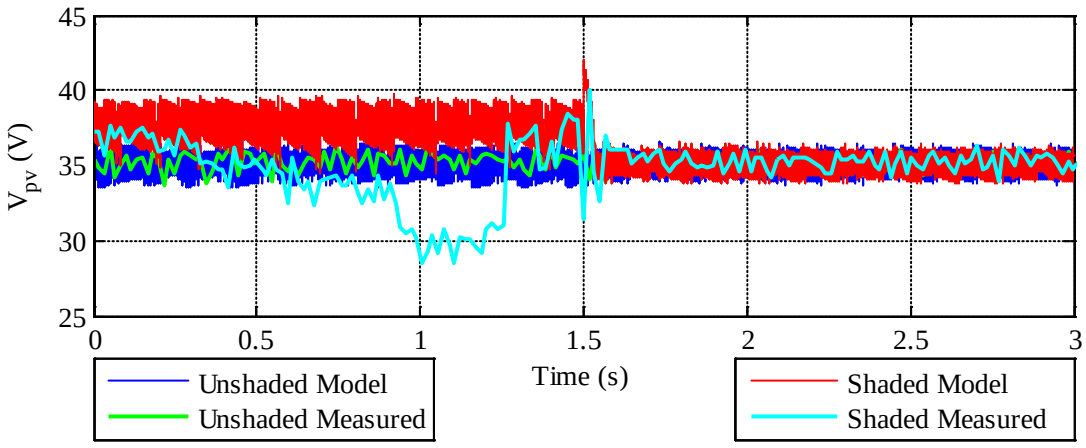


Figure 7.34: Response of V_{pv} to step increase in irradiance

To determine the cause of the disturbance, the tests were run again a number of times with a faster data-logging system and a video camera to observe the shading process. The response of V_{pv} from the shaded PV module for the test run that is closest to the same pattern as the original is presented in Figure 7.35.

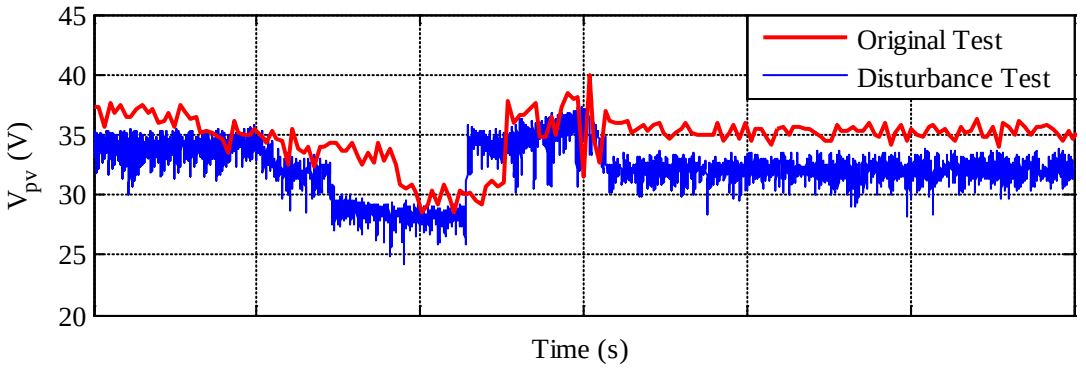


Figure 7.35: Response of V_{pv} from shaded PV module to step increase in irradiance

The PV voltage of the disturbance test appears to have a number of distinct sections. These sections have been highlighted in Figure 7.36 through the use of different colours.

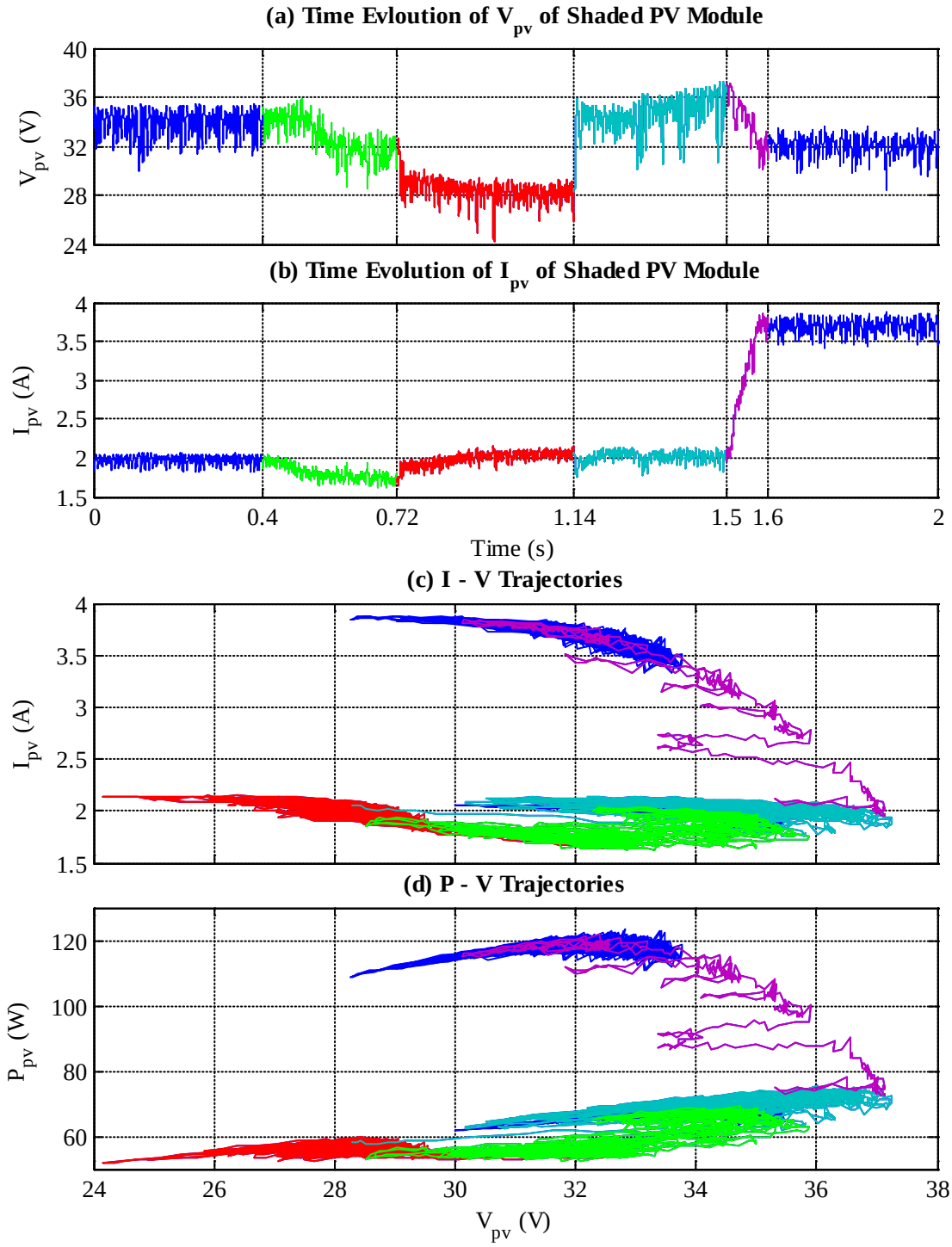


Figure 7.36: Sections occurring during Disturbance Test

To analyse the different sections the video of the shading test was studied. The frames in Figure 7.37 were extracted at the approximate intersection times of plots (a) and (b) in Figure 7.36. The frame rates of the video is about 30ms.

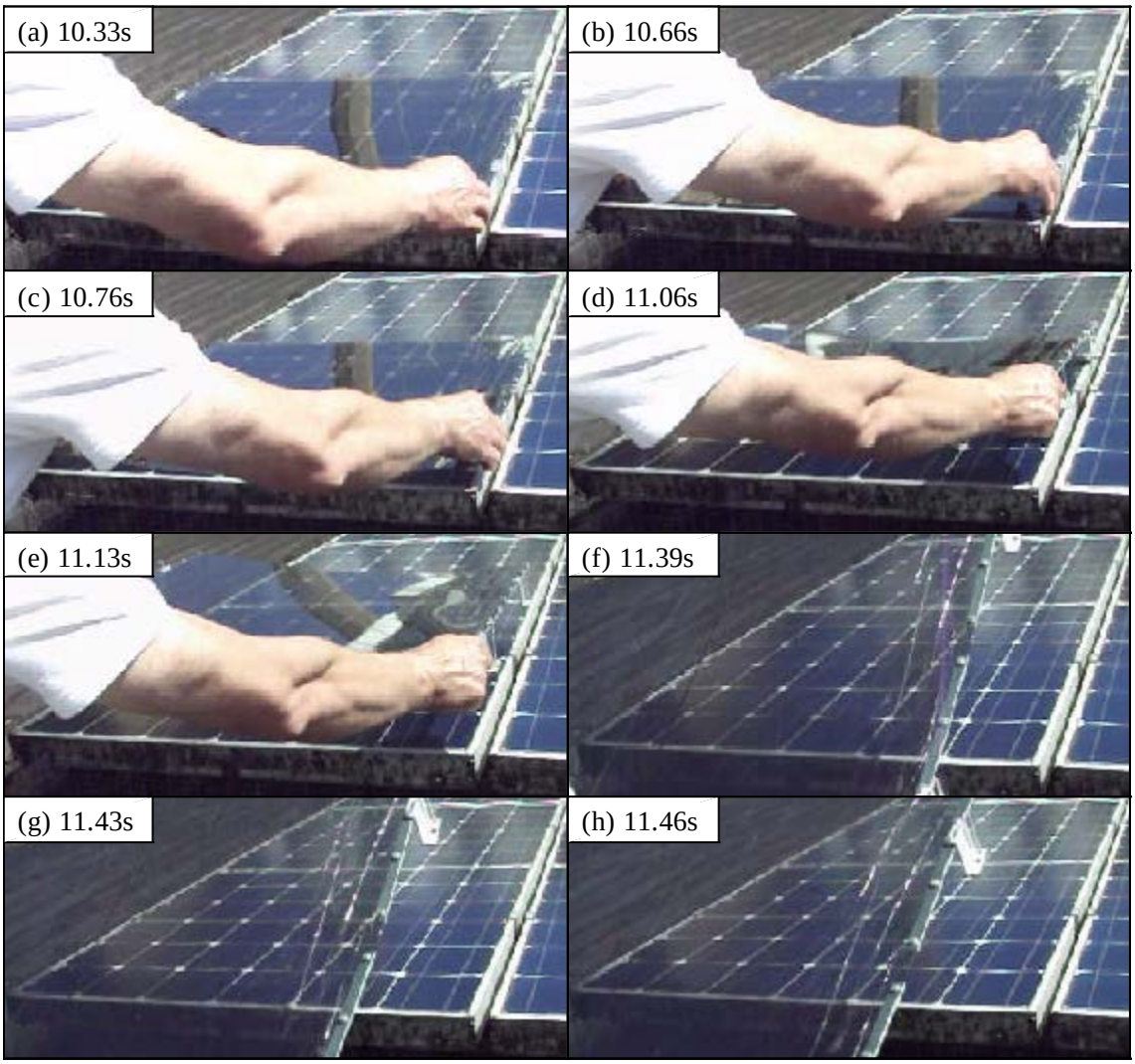


Figure 7.37: Removal of shading during Disturbance Test

In the region of 10.33s into the video recording there is slight shading from the right hand. This shading would correspond with the green disturbance section in Figure 7.36. The I – V and P – V trajectories do not show a clear MPP which could be due to the shading on the bottom right hand cell causing operation in the reverse characteristic, thus distorting the curves. Alternatively, there may be some initial interaction between the SMs.

Approximately 0.3s after the initial disturbance the shading panel is lifted ready for removal. The higher hand position would cause a larger shadow to fall on the affected cell to a point where the bypass diode for the substring containing the affected cell would begin to operate. The apparent red section MPP in the P – V trajectory is roughly 5V lower than the initial MPP at around 34V, implying that one of the 6 bypass diodes is operating.

The jump to the light blue section in Figure 7.36 at 1.14s corresponds to the point at which the shading from the hand leaves the PV module in the region of 11.1s. While the shading material is being removed from the PV module each row of cells is gradually un-shaded, moving the operating voltage closer to the unshaded characteristic while the current remains almost constant due to the limiting of the remaining shaded cells.

At round 11.45s the video shows the last of the shadow leave the PV module. This would correspond with the start of the purple section, 1.1s after the initial disturbance. The purple section shows the MPPT of the SM moving the operating point along the characteristic towards the unshaded MPP where it resumes steady state operation.

Figure 7.38 shows the response of the inverter voltage from the original test, along with the DMPPT system simulation results. The measured data shows a spike in V_{inv} just after the change in irradiance. The spike does not appear in the simulation since the inverter model involves a constant voltage source.

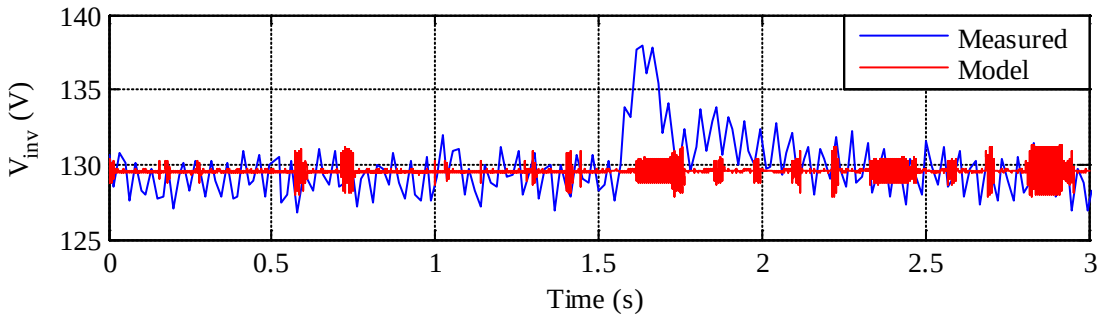


Figure 7.38: Response of V_{inv} to step increase in irradiance

The data obtained from the disturbance test was used to investigate this voltage spike as shown in Figure 7.39. This shows an interaction between the inverter and the SMs involving the input capacitance of the inverter. Between 1.5s and 1.555s the inverter current I_{inv} rises due to the additional power available from the irradiance increase. The corresponding inverter voltage V_{inv} also rises during this period, but lags I_{inv} implying the input capacitor is charging, either due to the switching circuit of the inverter not being fast enough to deal with the extra power, or the inverter inductance limiting the current.

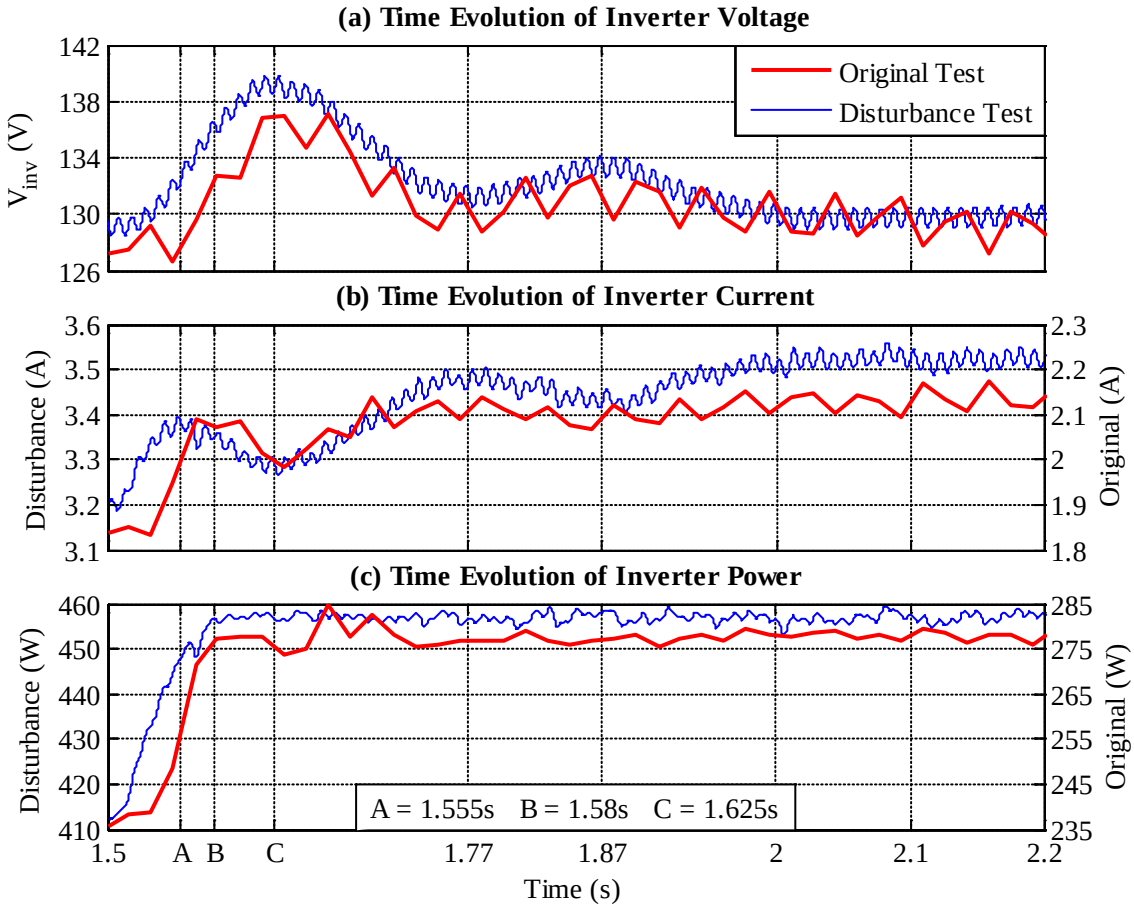


Figure 7.39: Investigation of inverter voltage spike

P_{inv} reaches a steady state at 1.58s showing that all 4 SMs are operating at the MPP of their connected PV module. Between 1.58s and 1.625s V_{inv} continues to rise after P_{inv} becomes stable indicating that the switching circuit has still not reached the required

current. V_{inv} and I_{inv} then oscillate at 180° from each other, due to the constant power, as the SMs try to establish an equilibrium point with the inverter switching circuit.

The simulated and measured V_{pv} responses to a step decrease in irradiance are compared in Figure 7.40. It can be seen that after the step decrease in irradiance, the SM of the shaded module results in a different point of operation for the simulated and measured systems.

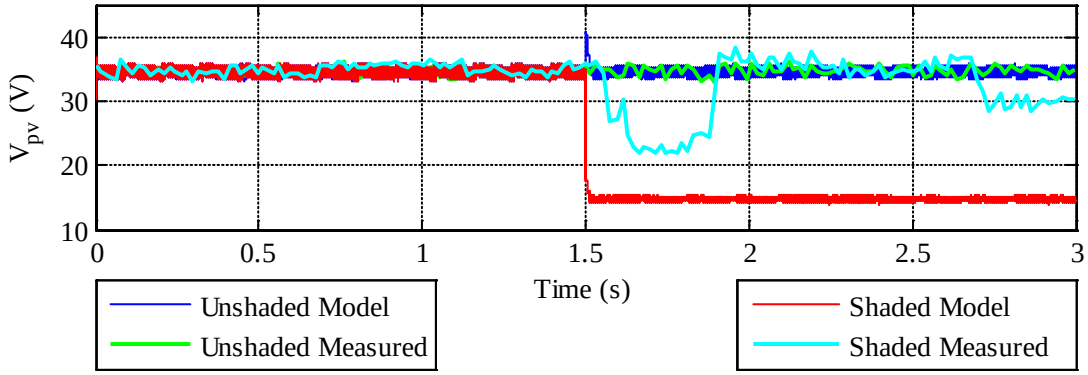


Figure 7.40: Response of V_{pv} to step decrease in irradiance

In Figure 7.40 the decrease in irradiance test shows a disturbance in V_{pv} during application of the shading. This disturbance was investigated in the same way the as the step increase test results. The disturbance test with the closest pattern is shown in Figure 7.41, which also settles to an operation point different to that of the simulation.

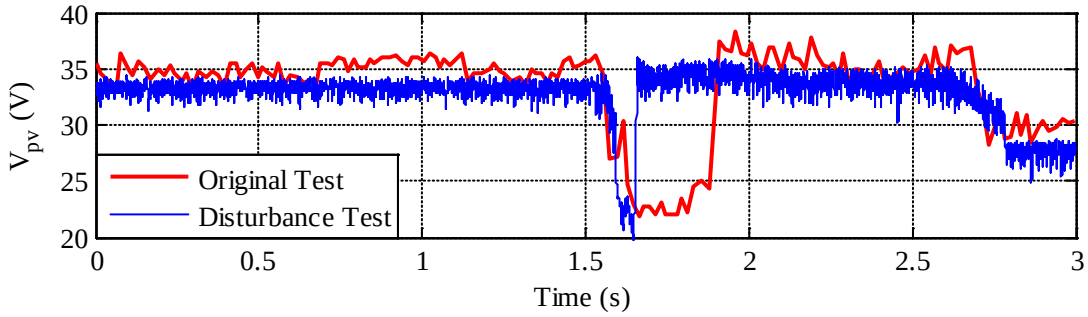


Figure 7.41: Response of V_{pv} from shaded PV module to step decrease in irradiance

To investigate the different operating points the P – V characteristics are plotted in Figure 7.42. The plot indicates two local maxima in power; the simulated SM operates at a lower voltage with the shaded half of the PV module bypassed, whereas during the practical tests the SM runs at the lower I_{mpp} of the shaded half of the PV module.

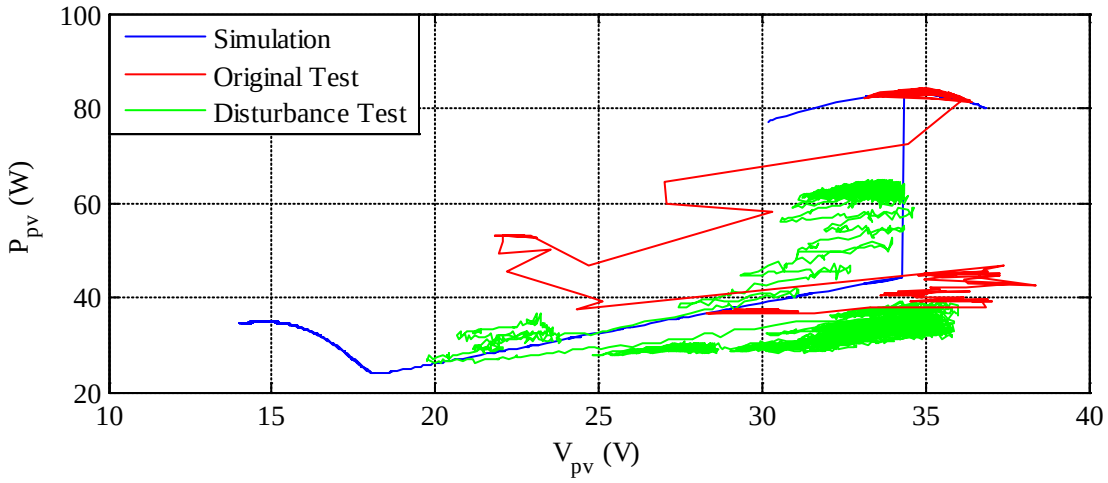


Figure 7.42: P-V trajectory of shaded PV module for step decrease in irradiance

For detailed investigation the results from the disturbance test are again broken down into the sections displayed in Figure 7.43 and are analysed using the video frames in Figure 7.44. Frame (a) corresponds to the first green section where the start of a shadow from the shading material can be seen on the edge of the PV module. As more of the bottom row of cells becomes shaded the current from the PV module reduces. This continues until enough of the cells have become shaded to activate the 2 bypass diodes for the substrings on the left and middle thus reducing the voltage by around 12V.

Frame (b) shows the shadow moving onto the right hand substring at which point all 3 substrings are shaded. The bypass diodes no longer operate and the module current drops whilst the voltage steps back up as shown in the red section of Figure 7.43.

This situation remains whilst the shading material is moved further up the module until the light blue section is reached. It can be seen in frame (c) that at this point the right hand holding the shading material causes extra shading on the bottom right cell in a

similar situation to when the shading was removed during the irradiance increase test. The shading on this cell reaches the critical point for the bypass diode of the substring to activate and the steady state of the dark blue section is reached.

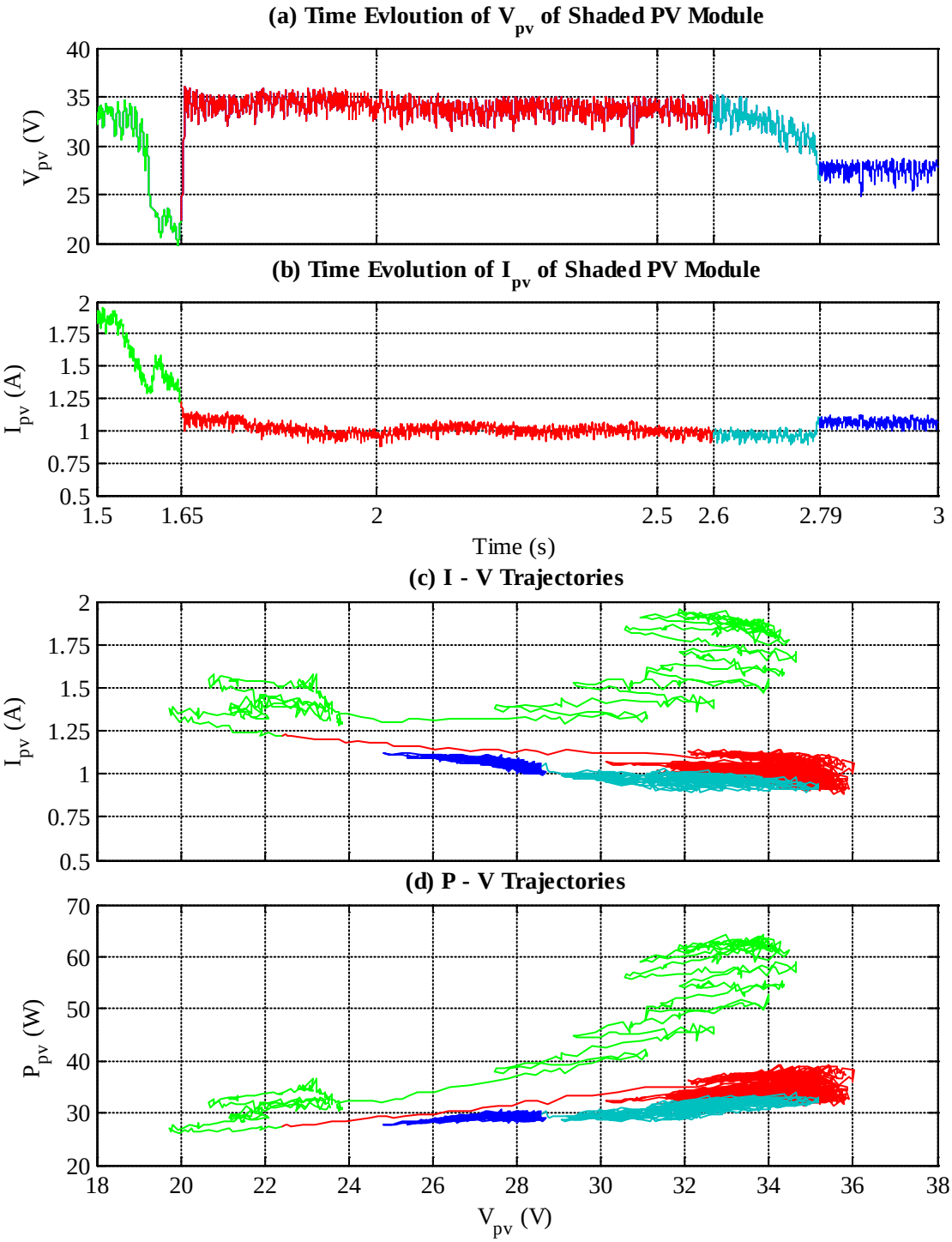


Figure 7.43: Sections occurring during Disturbance Test

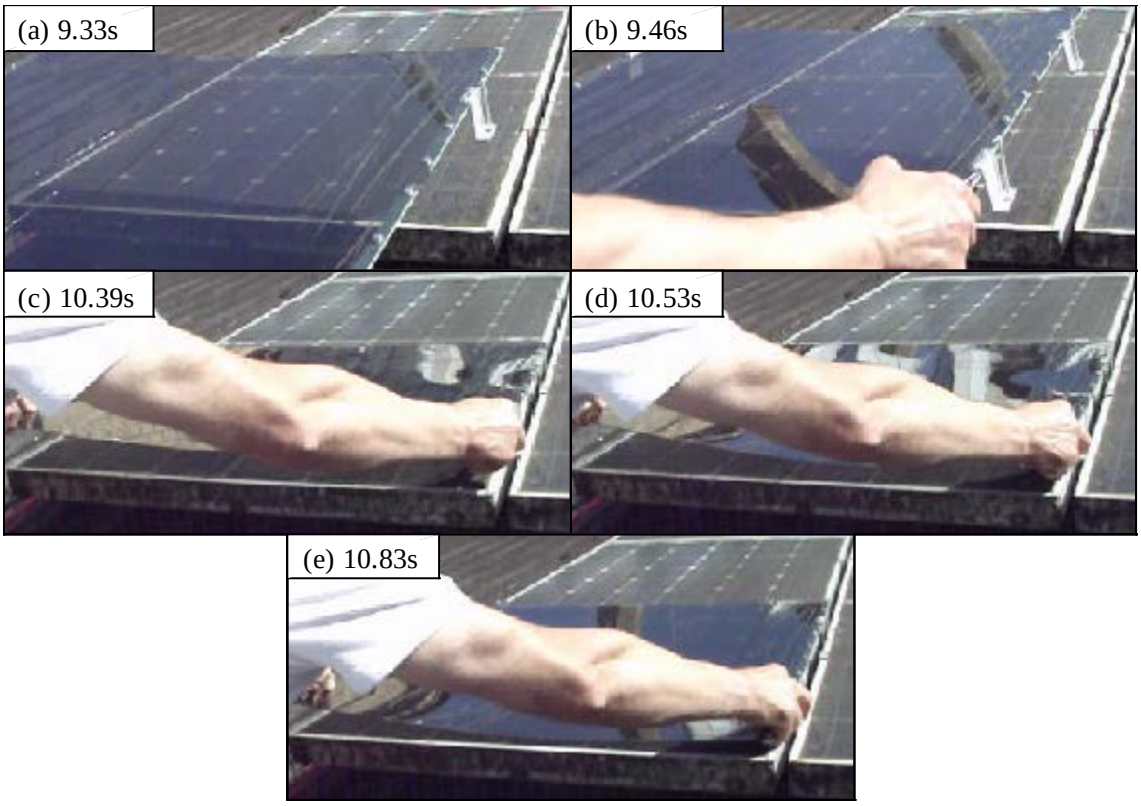


Figure 7.44: Application of shading during Disturbance Test

A detailed analysis of the SM response with the original experimental data was limited by the sampling rate of the datalogger used as indicated in Figure 7.45. The MPPT patterns of the simulated SMs are just visible, with approx. 12 MPPT periods in between each measurement of the datalogger.

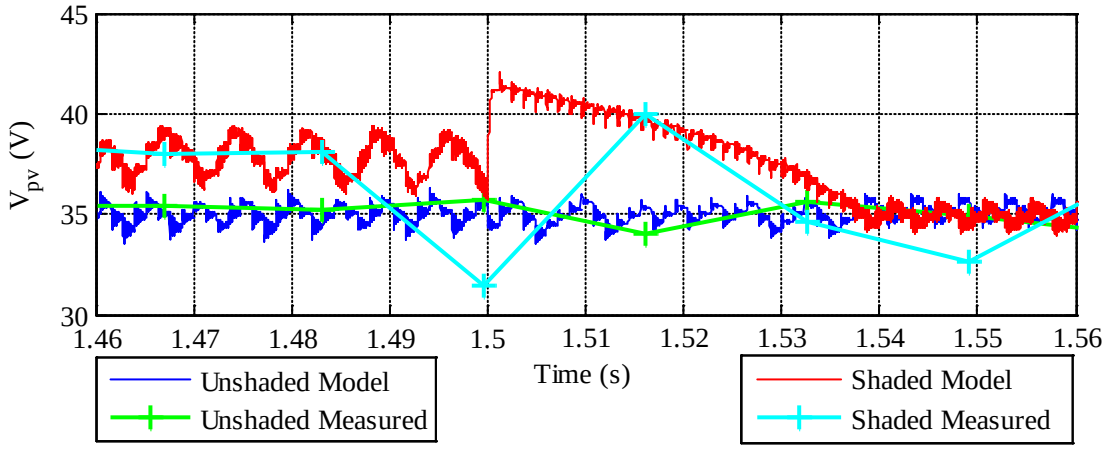


Figure 7.45: Magnified plot of PV module voltages at irradiance increase step

The set of data from the re-run tests with the least amount of disturbance before the irradiance step was plotted against the simulation data in Figure 7.46. The pattern for V_{pv} of the shaded PV module is closely matched between the simulation and experimental results with a jump in voltage preceding a gradual return to a steady state MPPT pattern.

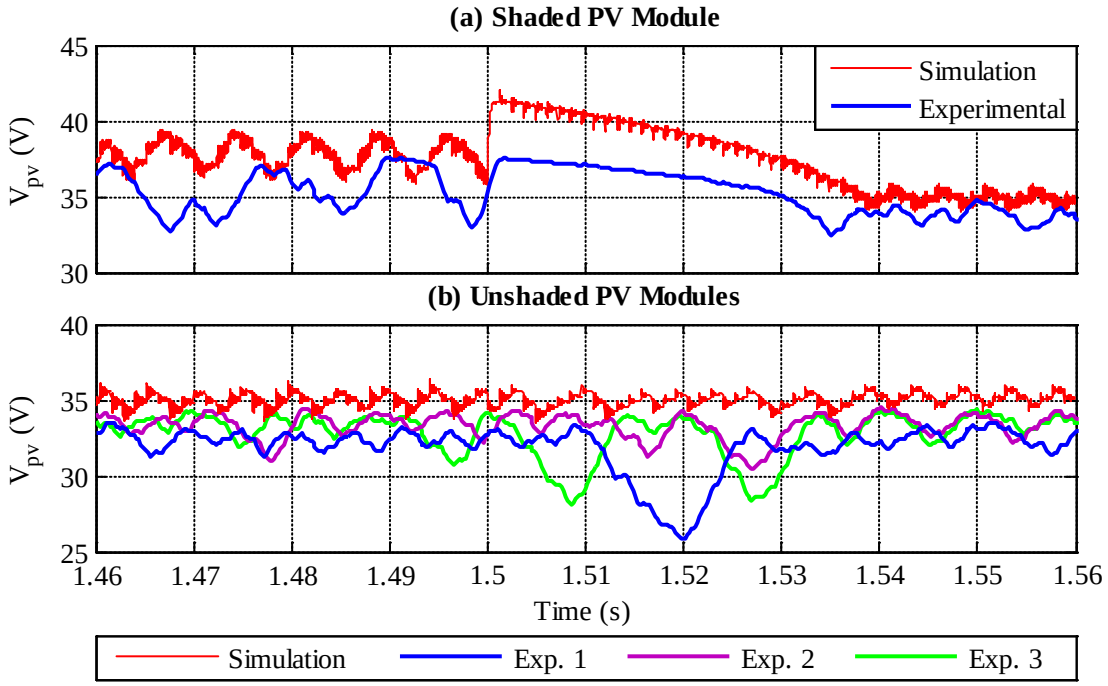


Figure 7.46: Magnified plot of V_{pv} with improved experimental data

However, the experimental data for V_{pv} of the 3 other PV modules shows a divergence from the MPP of the modules, whereas the simulated data indicates that the MPP of these modules have been maintained. The deviation from MPP may be due to the interactions between the SMs and the inverter discussed earlier.

The results of the DMPPT simulation show that overall the DMPPT model provides an accurate system response to a step change in irradiance, although the inverter model can be improved, possibly with the addition of some input inductance to limit the rate of change for the input current and allow the capacitor to charge up when an increase in PV power occurs.

The data originally collected on the outdoor system was shown to be limited; a faster data collection system provided more detailed practical results that allowed analysis of the system when combined with a video recording of the experiment. However, it has been shown that the method for application and removal of shading in the practical system produces complex patterns of shading; both physically across the PV module as well as during time. Therefore, the testing could be improved further by setting up a means of shading the PV module without causing unwanted complex disturbances.

7.4 Summary of Modelling of PV Systems

In the first section of this Chapter a PSpice model of a PV module has been developed using analogue behavioural model (ABM) blocks and a diode model to implement the single-diode equation. To simplify the use of the model in a PV system it was developed into an intuitive black box type model using a hierarchical design that takes the model parameters as inputs and provides the corresponding PV electrical characteristic at its outputs.

The second section presents the development of a block model for a SolarMagic (SM) power optimiser. To improve the simulation speed the switching components are removed since they have been shown to be unnecessary when modelling interactions between maximum power point trackers (MPPTs) in a PV system. The models use ABM blocks to implement the averaged equations for the switching power electronics. The SM dynamic components were included since they may have an effect on the MPPT. The dynamic response of the simulation was shown to closely match the experimental results.

In the third section a Simulink model of the SM MPPT controller was developed for co-simulation with the PSpice electrical model. A very close match was observed between the simulated start-up of the SM and the experimental results.

The fourth section describes the development of a block model for the SB700 PV inverter. The equation for the inverter ripple voltage, derived in Chapter 6, was applied to the model. This obtained a realistic ripple in the PV current when compared with the inverter test data. The MPPT control developed for the SM was adapted to reproduce the SB700 MPPT pattern and include the start-up procedure of the SB700.

To investigate the behaviour of DMPPT systems the SM and SB700 models were combined and used to simulate the tests of irradiance step change described in Chapter 6. A more detailed analysis required further testing of the real system with a faster data collection system to measure the SM response correctly.

The overall patterns in behaviour of the simulated PV voltages and currents exhibited a very close match to the experimental data for a step increase in irradiance with differences accounted for by the complex shading patterns caused by the test method. For a step decrease, operation at different maxima in power was observed between the simulation and real system.

The simulation did not reproduce the observed interactions between the SM outputs and the inverter input for a step increase in irradiance. To rectify this, the inverter model may require modification to limit the rate of change of current, or power flow, from the input.

Chapter 8 MPPT Interactions

The previous chapter has described the development of a ‘black box’ computer model for simulating distributed maximum power point tracker (DMPPT) systems. The model was developed for the purpose of investigating the scenarios described in this Chapter to determine whether unwanted interactions can occur between controllers in a DMPPT system.

8.1 Loss of a Power Optimiser

This section outlines the scenario of a fault in one power optimiser in a DMPPT system indicating the possibility of causing negative interactions in such a system. Methods for adapting the developed DMPPT model for this investigation are suggested.

8.1.1 Scenario Description

It is unclear how a DMPPT system would respond to a sudden loss of operation of a power optimiser. This would have the initial effect of increasing the voltage across the output of the remaining power optimisers to compensate for losing the voltage from the faulty device. The increased voltage of the power optimisers is likely to be above the rated voltage and the devices may shut down.

Also, the available voltage and power of the power optimiser string would be reduced and may be below the minimum operating voltage of the inverter. If the inverter encounters too low a voltage it may stop operating. Since it takes a few minutes for the inverter to start up this would result in a significant reduction in energy yield.

The fault could either present itself as an internal short circuit between the output terminals, or a failure of the power electronics that prevents the flow of power from the PV module to the output. In this case the bypass diode of the SM would come into operation and further decrease the available string voltage.

Whether the remaining power optimisers are able to recover the situation, or if a fault condition is developed in these as well should be investigated.

8.1.2 Adaptation of DMPPT model

The loss of a power optimiser would in effect be the same as a fast reduction of irradiance on a single PV module except with the irradiance falling to 0Wm^{-2}. A similar method for simulating the step changes in irradiance in Chapter 7 could therefore be used but applied to a whole PV module and not half.

However, the operating limits of the power optimisers and the inverter need to be added to the model. For example, the SolarMagics (SMs) used in testing will 'shut down' when the maximum output voltage of 43V is exceeded. Once this shut down mode has been entered the SM will remain inactive until the voltage at its output falls below the input voltage (usually the PV module open circuit voltage).

Further investigation into this shut down procedure is required so that the behaviour can be included in the Simulink model. Similarly, the inverter behaviour for low input voltage should also be investigated for inclusion in the Simulink model.

8.2 MPP Tracking of the Inverter

The inverter considered during this work has been the SMA SB700. The maximum power point tracker (MPPT) of the SB700 applies the perturb and observe (P&O) routine by effecting a 0.6V step every 5s. This section will discuss the need to investigate alternative inverter MPPT procedures.

8.2.1 Scenario Description

It has been observed during this work that the slow maximum power point tracker (MPPT) of the SB700 has little effect on the performance of the fast SolarMagics (SMs). However, an inverter with a faster MPPT than the SB700 may start to interact with the MPPTs of the associated power optimisers in a DMPPT system. For example,

due to the MPPT update period trade-off between a fast MPPT for quick determination of the MPP, during start-up or transient events, and the lower steady-state losses associated with a slower update period, an algorithm with a variable period can be used to achieve the best qualities of each.

To investigate this concern, the inverter MPPT model developed during this work can first be adapted to ascertain whether any negative interactions would occur with a faster MPPT algorithm. If it was established that such interactions do happen the developed model can be used to quantify a critical point at which the interactions begin. A test of variable speed MPPT procedures can then be investigated to determine if a change in the rate of MPPT will upset the MPPTs of the power optimisers.

Also, other MPPT algorithms used in PV inverters may be more prone to interactions. For example, it is not clear how the power optimisers would react to an inverter MPPT using a method of sweeping across the I-V characteristic to determine the true MPP of the array. Conversely, there is a possibility that the power optimisers may interfere with an inverter using the Ripple Current Correlation MPPT algorithm.

8.2.2 Adaptation of DMPPT Model

For the modelling of a faster MPPT algorithm it is simply a case of reducing the sample time of the MPPT schedule counter. Also, a two speed MPPT could be implemented during start-up in the same way as the SB700 ramp function in Chapter 7; except that the switchover would occur on reaching the MPP as opposed to reaching a particular inverter input voltage. However, to respond to a transient event, a method of feedback would be required to determine whether a change in conditions has occurred.

To obtain models of alternative MPPT algorithms, a review of literature would be required.

8.3 Fast Complex Transients in Irradiance

A step change in irradiance to one half of a PV module was investigated using the outdoor test rig in Chapter 6 and the DMPPT system model in Chapter 7. In both cases a fast stable system response was observed, in that the SM power optimisers were able to recover the MPP quickly. This section considers what might happen if the transients were more complex.

8.3.1 Scenario Description

Some PV arrays may be prone to a complex shading pattern with a fast transient, for example a tree branch or flag blowing in the wind may cause a shadow to move back and forth across the PV array. The quick, irregular patterns in available power from a number of PV modules in the array may upset the MPPT controllers of the power optimisers, thus causing unwanted interactions.

8.3.2 Adaptation of DMPPT Model

To produce variations in irradiance the Simulink section of the developed DMPPT model contains the Irradiance subsystem in which the user can easily apply any time varying irradiance pattern to the individual PV modules. It also allows the user to import measured irradiance patterns through the MATLAB workspace (that can deal with the majority of data formats) if such data is available.

8.4 Partial DMPPT Systems

The partial deployment of SMs on a single string is described by the manufacturer [50]. A discussion of possible MPPT interactions in such a system is provided in this section.

8.4.1 Scenario Description

A PV system configuration such as the one shown in Figure 8.1 is recommended for PV installations where there is a common source of partial shading that acts on the array over an annual cycle. It is argued that the PV modules that do not encounter this shading

are not in need of assistance from power optimisers which would only reduce their effective output power due to the losses of the SM.

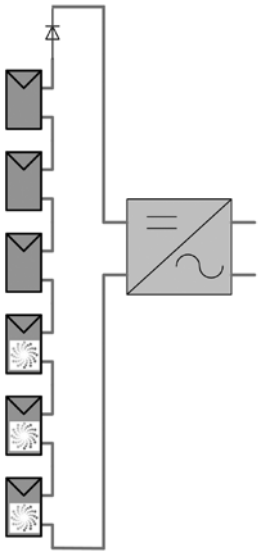


Figure 8.1: Partial deployment of SM power optimisers on the three lower PV modules [50]

In this case the inverter is required to have an MPPT. This leads to a situation where some of the PV module MPPs are being tracked by the inverter and the others by the connected power optimiser. Further investigation should be carried out to determine how the MPPT controllers interact in this scenario.

8.4.2 Adaptation of DMPPT Model

To modify the developed DMPPT model for simulating partial DMPPT systems requires the removal of a number of power optimisers and the direct reconnection of the associated PV modules to the string in the PSpice model. The corresponding power optimiser MPPT control blocks should also be removed from the Simulink model and the appropriate re-routing of the signals applied.

8.5 Blocking Diode Omission

As mentioned previously, the SolarMagic manufacturer strongly advises the use of a blocking diode for protection, as indicated in [50]. Through comparing simulations of a

DMPPT system both with and without the blocking diode it can be determined when it is required, or if it is necessary at all. The investigation can be repeated for the case of partial deployment of SMs. If it is found that for a particular system configuration the blocking diode is not necessary, installation costs could be reduced by not including one in the system.

Chapter 9 Conclusions and Indications of Future Work

The previous chapters have introduced, described and discussed the research carried out. This chapter presents the novel aspects of the research, the conclusions drawn with respect to the work done during this study and the possibilities for continuing the research in future work.

9.1 Construction of a PV emulator

The design and construction of a PV emulator (PVE) was presented in Chapters 3 to 5. This section summarises the original contribution carried out during this work along with some general conclusions.

9.1.1 Areas of Original Contribution

To improve the PVE feedback loop stability using a digital lookup table method of control was designed to use the effective load resistance or conductance as the table input, as explained in Chapter 4. To allow operation across the entire I-V characteristic a method was developed based on [88] that involves switching the controlled variable of the DC supply between voltage, using effective load resistance, and current, using effective load conductance, depending on the operating point.

For operating at the higher voltage levels of a PV array emulator (PVAE) an IGBT was used as part of a linear regulator, as described in Chapter 5. To compensate for the variable gain of the gate voltage to collector current characteristic a linearisation circuit was designed and constructed.

9.1.2 General Conclusions

A PVE allows controlled repeatable testing of PV system power conditioning devices (PCDs) with a controllable I-V characteristic.

A PVE is usually either a PV module emulator (PVME) or PV array emulator (PVAE) where a PVME is used for testing per-module power-optimisers and a PVAE for testing PV system inverters.

A PVE consists of two sections: a controllable DC power supply (CDCPS) to provide the electrical output and a 'computational control system' to maintain the electrical output on the desired PV characteristic.

There are four main variants of the computational control system:

- An analogue scaling circuit produces a realistic I-V curve from a sample PV cell and controllable light source. However, this method is rarely used now due to the requirement of a controllable light source and the limitation of the I-V characteristic to the sample cell used.
- An analogue computation circuit (ACC) utilises a low-cost circuit of diodes and resistors to reproduce the 1 or 2 diode model of a PV cell; the I-V characteristic can be modified using variable components. However, the I-V curve is set manually and to emulate partial shading patterns would require a number of circuits; the overall complexity would quickly increase.
- A real-time digital computation system uses a digital signal processor or microcontroller/processor to apply the 1 or 2 diode equation instantaneously. To calculate partially shaded conditions fast enough for use in an emulator is challenging due to the extra processing required, especially for complex shading patterns.
- To control a PVE the digital-lookup computation system (DLCS) applies pre-calculated lookup tables of the I-V characteristic through a digital signal processor or microcontroller/processor. The DLCS can emulate complex partial

shading conditions but can suffer from the quantisation and discretisation errors associated with digital systems.

For academic use commercially available PVEs offer an acceptable specification but are also too costly.

A developed PV emulator can be designed to the specification of the application for which it is required.

The ACC developed during this work produces a reference voltage from a measured current and was shown to give an acceptably accurate I-V characteristic when compared with the curves of the manufacturer.

To operate a PVE across the entire I-V characteristic requires control of both the output current and voltage.

Stability of a DLCS can be improved and the PVE operated across the entire I-V curve by switching the input to the table between effective load resistance and conductance whilst also switching between voltage control and current control respectively. The switching depends on the point of operation on the curve and is applied in a hysteresis fashion to avoid chattering.

It has been shown that due to a slow response time a commercial programmable DC power supply is not suitable for use as the CDCPS in a PVE.

The developed PVME with a linear regulator output stage and ACC control demonstrated an accurate I-V curve, even when tested with a fast active MPPT controlled device.

A high voltage PVAE constructed with a linear regulator output stage would require an extra switched-mode DC voltage source (SMDCVS) stage to limit the voltage across the regulator.

The less complex and faster diode-rectifier/boost-converter topology would be preferable to a thyristor-controlled rectifier for use as the SMDCVS in a PVAE.

9.2 Modelling of a PV System

Chapter 7 describes the development of a 'black box' PV system model that can be easily reconfigured for modelling different system topologies. The model of Chapter 7 is verified using the experimental results presented in Chapter 6. This section highlights the unique features of this work and presents the general conclusions.

9.2.1 Areas of Original Contribution

To obtain 'black box' type models of PV modules and PCDs that allow reconfiguration of the system the hierarchical block models for PSpice in OrCAD were used as detailed in Chapter 7 Sections 7.1 and 7.2.

To apply the averaged equations of the power optimiser power electronics whilst reproducing the overall dynamics of the energy storage, Subsection 7.2.2 explains how analogue behavioural model blocks were used in a similar manner to [41] and combined with energy storage components.

For the block model of a voltage-sourced single-phase PV inverter Subsection 7.2.4 describes how a controllable DC source was used to implement the MPPT algorithm whilst the ripple was applied through a combination of variable AC voltage source and input capacitance. An equation relating the size of the ripple to the input current of the inverter was derived from [91] and implemented in the model.

To utilise the accurate electrical simulation environment of PSpice for modelling PCD power electronics whilst applying an MPPT algorithm with the powerful control signal based environment of MATLAB Simulink, Section 7.3 shows how the models have been developed to exploit the SLPS co-simulation tool. Irradiance patterns can also be

applied through Simulink allowing real irradiance measurements to be imported through MATLAB if the data is available.

9.2.2 General Conclusions

The 5 single diode PV model parameters can be extracted from the voltage and current values at open circuit, MPP and short circuit.

The model characteristics of efficiency and DMPPT perturbation for a power optimiser can be derived from testing with a PV emulator.

For modelling interactions in DMPPT systems, simulating the switching of the power electronics is unnecessary and the averaged equations can be applied directly.

The dynamic response of a power optimiser can be obtained from testing with a real PV module in a solar emulator. To observe the underlying waveform, the switching frequency can be determined using an FFT plot and the switching ripple removed from the waveform by post-filtering the measured data.

An approximately linear relationship between the inverter ripple and the inverter input current was derived from theory.

To provide correct operation in a perturb and observe MPPT routine, the timing sequence of the actions is important.

An accurate reproduction of the real SolarMagic was observed from the combined Simulink MPPT model and PSpice electrical model.

The simulated inverter ripple was shown to be a close match to the real data collected using an oscilloscope.

The developed DMPPT system model was shown to produce a realistic response when compared with the data collected from the outdoor test rig.

9.3 Future Research

This section contains some suggestions for areas of research that were not possible in this work, due to either restrictions on time or not being necessary for the main objective, but these research topics should be considered for future work.

9.3.1 Construction of PVAE

An SMDCVS based on a diode-rectifier/buck-converter topology can be designed and constructed for use with the developed linear regulator as part of a PVAE. To provide a flexible PVAE that can emulate partial shading conditions, the DLCS system described in Chapter 4 can be implemented through a microprocessor.

9.3.2 Development of PVMEs for Testing DMPPT Systems

A PVE system with multiple PVMEs can be constructed to provide controllable indoor testing of a DMPPT system. Each PVME could utilise an unregulated DC supply and linear regulator configuration with ACC emulator control. To emulate a system of four 200W PV modules the supply can be taken from the 240V mains using a switched mode topology with lightweight and compact high frequency transformers to produce a manageable bench-top system.

9.3.3 Improvements to Solar Emulator

The work presented on the solar emulator in Chapter 6 shows a deviation in the MSX60 I-V curve. Such a deviation usually indicates the operation of a bypass diode due to a mismatch in currents between series connected strings. A probable cause of the mismatch is an irregular pattern of G and T across the MSX60. Further work is recommended to improve the solar emulator and remove the unwanted mismatch effects whilst making it larger to allow larger sized panels to be used.

9.3.4 Improvements to Outdoor Test Rig

During testing of the DMPPT system the application and removal of the shading material unintentionally caused complex shading patterns that are challenging to reproduce in a computer simulation. To reduce the complex disturbances during the application of a step change in irradiance the method used to apply the step change should be redesigned.

Appendix A Parameter Extraction for Single Diode Model

The single diode representation of a PV module described in Chapter 1 uses the 5 model parameters I_{ph}, I_o, R_s, R_p and γ to control the shape of the I-V curve. The extraction of the parameters using data from the manufacturer or from experimentation is required. A set of 3 equations for the 3 parameters R_p, R_s, and the thermal voltage V_{th} are solved using the generalised Newton's Method as described in this Appendix.

A1 Newton's Generalised Iterative Method

This section describes the generalised Newton's Method used extensively throughout this work. The application of Newton's Method to a single variable, for example to solve the single-diode equation, is described first and then expanded for a set of three general equations.

Figure A.1 provides a graphical representation of the iterative Newton's Method, used to determine the root x of an equation $f(x)$.

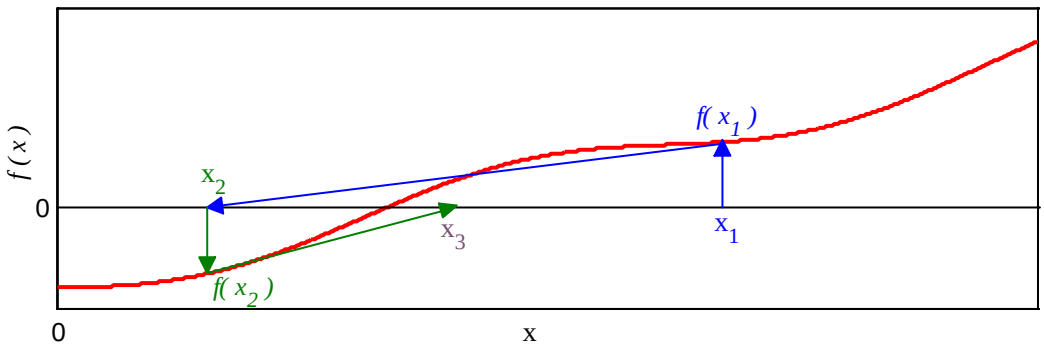


Figure A.1: Graphical representation of Newton's Method

The iterative routine is started from an initial estimate x_1 of the root. The corresponding value of $f(x_1)$ and slope $f'(x_1)$ are used in Newton's Equation to calculate the next estimate x_{n+1}:

$$x_{n+1} = x_n - \frac{f(x_n)}{\frac{df(x_n)}{dx}} \qquad \textbf{(A.1)}$$

This process is repeated so that, as can be seen in Figure A.1, the value of x_n converges on the root. The iteration is stopped when the difference in successive values of x_n is within a specified level of accuracy A:

$$|x_{n+1} - x_n| \leq A \qquad \textbf{(A.2)}$$

Whether the algorithm converges or becomes numerically unstable and diverges depends on the function $f(x)$ and the initial guess x_1. For example, if an initial guess of close to zero was used in Figure A.1, the almost zero slope of the function would result in an extremely large value for the subtracted term in (A.1) moving the algorithm far away from the root.

Newton's Equation can be expanded for a set of equations as described in [67]. In this case the partial derivative is used and the new estimate calculated for the first variable is used to obtain the next estimate of the second, and so forth.

$$x_{n+1} = x_n - \frac{f_1(x_n, y_n, z_n)}{\frac{\partial f_1(x_n, y_n, z_n)}{\partial x}} \qquad \textbf{(A.3)}$$

$$y_{n+1} = y_n - \frac{f_2(x_{n+1}, y_n, z_n)}{\frac{\partial f_2(x_{n+1}, y_n, z_n)}{\partial y}} \qquad \textbf{(A.4)}$$

$$z_{n+1} = z_n - \frac{f_3(x_{n+1}, y_{n+1}, z_n)}{\frac{\partial f_3(x_{n+1}, y_{n+1}, z_n)}{\partial z}} \qquad \textbf{(A.5)}$$

A2 Application of Newton's Method

Three equations for obtaining the parameters R_p, R_s and V_{th} from the operating points of open circuit, maximum power and short circuit are derived in [66]:

$$f_1(V_{th}, R_s, R_p) = \mathrm{I_{sc}} - \mathrm{I_{mpp}} - \frac{\mathrm{V_{mpp}} + \mathrm{I_{mpp}R_s} - \mathrm{I_{sc}R_s}}{\mathrm{R_p}} - \left(\mathrm{I_{sc}} - \frac{\mathrm{V_{oc}} - \mathrm{I_{sc}R_s}}{\mathrm{R_p}}\right) \mathrm{e}^{\left(\frac{\mathrm{V_{mpp}} + \mathrm{I_{mpp}R_s} - \mathrm{V_{oc}}}{\mathrm{N_s V_{th}}}\right)} \quad \textbf{(A.6)}$$

$$f_2(V_{th}, R_s, R_p) = \mathrm{I_{mpp}} + \mathrm{V_{mpp}} \left(\frac{-\left(\mathrm{I_{sc}R_p} - \mathrm{V_{oc}} + \mathrm{I_{sc}R_s}\right) \mathrm{e}^{\left(\frac{\mathrm{V_{mpp}} + \mathrm{I_{mpp}R_s} - \mathrm{V_{oc}}}{\mathrm{N_s V_{th}}}\right)} - \mathrm{N_s V_{th}}}{\left(\mathrm{I_{sc}R_p} - \mathrm{V_{oc}} + \mathrm{I_{sc}R_s}\right) \mathrm{e}^{\left(\frac{\mathrm{V_{mpp}} + \mathrm{I_{mpp}R_s} - \mathrm{V_{oc}}}{\mathrm{N_s V_{th}}}\right)} + \mathrm{N_s V_{th}}\left(\mathrm{R_p} + \mathrm{R_s}\right)} \right) \quad \textbf{(A.7)}$$

$$f_3(V_{th}, R_s, R_p) = \frac{1}{\mathrm{R_p}} + \frac{-\left(\mathrm{I_{sc}R_p} - \mathrm{V_{oc}} + \mathrm{I_{sc}R_s}\right) \mathrm{e}^{\left(\frac{\mathrm{I_{sc}R_s} - \mathrm{V_{oc}}}{\mathrm{N_s V_{th}}}\right)} - \mathrm{N_s V_{th}}}{\left(\mathrm{I_{sc}R_p} - \mathrm{V_{oc}} + \mathrm{I_{sc}R_s}\right) \mathrm{e}^{\left(\frac{\mathrm{I_{sc}R_s} - \mathrm{V_{oc}}}{\mathrm{N_s V_{th}}}\right)} + \mathrm{N_s V_{th}}\left(\mathrm{R_p} + \mathrm{R_s}\right)} \quad \textbf{(A.8)}$$

These equations allow the use of data given by the manufacturer, or from an experimental data set. It is not possible to solve the 3 equations analytically due to the implicit nonlinear nature of the diode junction exponential term. The approach used in [66] has not been described clearly and so an iterative routine based on Newton's Method is used to solve the derived equations as shown in the flow diagram of Figure A.2.

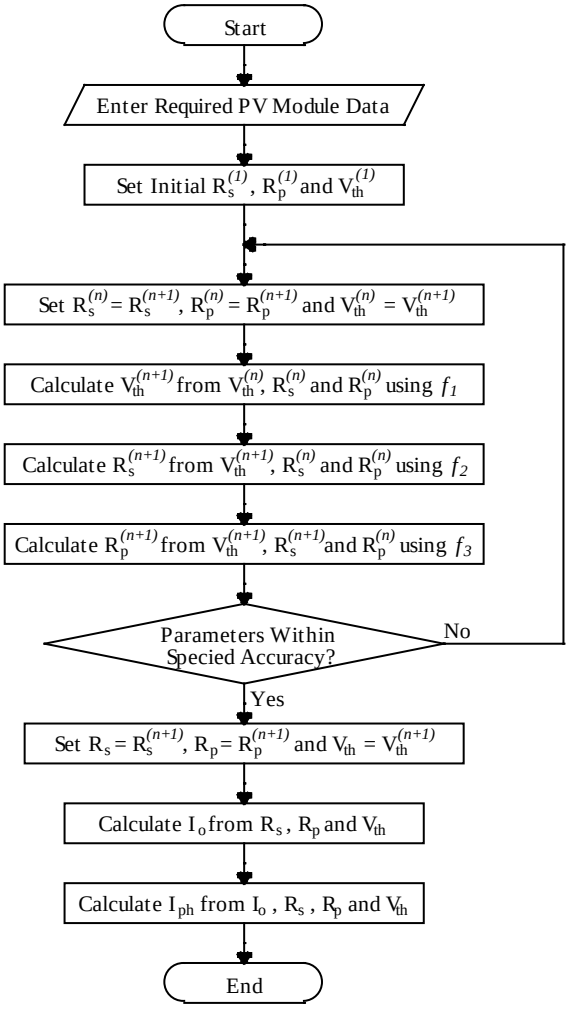


Figure A.2:Flow diagram of parameter extraction using Newton's Method

The appropriate combination of the variables R_p, R_s and V_{th} with the equations (A.6) to (A.8) is important to maintain numerical stability of the algorithm. This was discovered when the combination of R_p with f_2 as suggested in [66] gave rise to a divergence in the parameter values. This was likely caused by the generation of a small value for the derivative of f_2 with respect to R_p. Therefore the derivative of each combination was analysed to determine suitable combinations of parameter and equation that would give numerical stability where the combinations in (A.9) to (A.11) were found to be the most stable.

$$V_{th}|_{n+1} = V_{th}|_n - \frac{f_1(V_{th}|_n,\ R_s|_n, R_p|_n)}{\frac{\partial f_1(V_{th}|_n,\ R_s|_n, R_p|_n)}{\partial V_{th}}} \quad \textbf{(A.9)}$$

$$R_s|_{n+1} = R_s|_n - \frac{f_2(V_{th}|_{n+1},\ R_s|_n, R_p|_n)}{\frac{\partial f_2(V_{th}|_{n+1},\ R_s|_n, R_p|_n)}{\partial R_s}} \quad \textbf{(A.10)}$$

$$R_p|_{n+1} = R_p|_n - \frac{f_3(V_{th}|_{n+1},\ R_s|_{n+1}, R_p|_n)}{\frac{\partial f_3(V_{th}|_{n+1},\ R_s|_{n+1}, R_p|_n)}{\partial R_p}} \quad \textbf{(A.11)}$$

The application of Newton's Method is performed by a MATLAB programme described in the flowchart of Figure A.2. The required PV module data I_{mpp}, I_{sc}, N_s, V_{mpp} and V_{oc} is first entered by the user. The parameter values of $R_s^{(1)} = 1$, $R_p^{(1)} = 1000$ and $\gamma^{(1)} = 1$ are chosen as initial settings as these values are of appropriate magnitude for the majority of mono-crystalline PV modules under STCs. Likewise the specified accuracy for termination of the iterative process is given by the initial value divided by 10^6 to ensure that the result is accurate to 4 significant digits.

The 'Symbolic Math Toolbox' in MATLAB was used to generate functions from the general equations for use in iteration. The equations are used in cascade whereby the new value for V_{th} is used in f_2 and the new values for V_{th} and R_s are used in f_3.

Once acceptable values for R_s, R_p and V_{th} have been obtained, I_o and I_{ph} are calculated analytically using equations derived in [66]. I_o needs to be determined first as the equation for I_{ph} is dependent upon it. Thus, the five model parameters for the single-diode model can be extracted from values often presented on a manufacturer's datasheet.

$$I_o = \left(I_{sc} - \frac{V_{oc} - I_{sc}R_s}{R_p}\right) \exp\left(\frac{-V_{oc}}{N_s V_{th}}\right) \quad \textbf{(A.12)}$$

$$I_{ph} = I_o \exp\left(\frac{V_{oc}}{N_s V_{th}}\right) + \frac{V_{oc}}{R_p} \qquad \textbf{(A.13)}$$

Appendix B Specification Sheets

B1 BP Solar Saturn 7175S PV Module

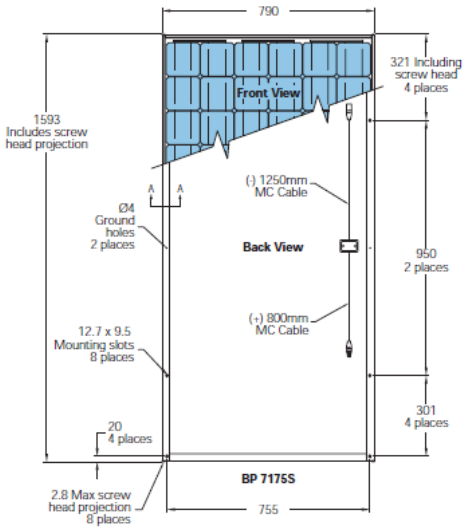
bp solar

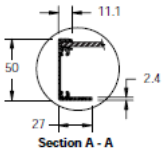
175 Watt Photovoltaic Module

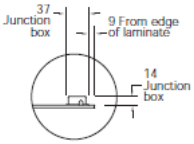
BP 7175

3018E-1 03/04

Module Diagram







Self-tapping grounding screw, instruction sheet and warranty document included with each module.

Typical Electrical Characteristics	BP 7175
Warranted minimum power*	175W
Voltage at P_{max} (V_{mp})	36.0V
Current at P_{max} (I_{mp})	4.9A
Short circuit current (I_{sc})	5.2A
Open circuit voltage (V_{oc})	44.2V
Temperature coefficient of I_{sc}	(0.065±0.015)%/K
Temperature coefficient of V_{oc}	-(160±10)mV/K
Temperature coefficient of P_{max}	-(0.5±0.05)%/K
NOCT (Air 20°C; Sun 0.8kW/m²; wind speed 1m/s)	47±2°C
Maximum series fuse rating	15A
Maximum system voltage	600V (IEC 61215 rating) 1000V (TÜV Rheinland rating)

*As measured by BP Solar test equipment to the nearest watt.

Standard test conditions - irradiance of 1000W/m² at an AM1.5G solar spectrum and a temperature of 25°C.

Mechanical Characteristics	BP 7175S	BP 7175L
Dimensions (mm) (Overall tolerances +/-3mm)	1593 x 790 x 50	1580 x 783 x 18
Weight (kg)	15.4	12.4
Frame	Clear anodised aluminium alloy type 6063T6. Silver Universal frame	
Solar cells	72 cells (125mm x 125mm) configured geometrically for a 6 x 12 matrix connected in series.	
Output cables	RHW AWG# 12 (3.3mm) cable with polarized weatherproof DC rated Multicontact connectors; asymmetrical lengths -1250mm (-) and 800mm (+).	
Diodes	IntegraBus™ technology includes for every 18 cells a Schottky by-pass diode integrated into the printed circuit board bus.	
Construction	Front: High-transmission 3mm tempered glass; Rear: White tedlar; Encapsulant: EVA.	

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www.bpsolar.com

bp solar

175 Watt Photovoltaic Module – Saturn Technology

BP 7175

3018E-1 03/04

The BP 7175 forms part of the new high efficiency Saturn 7 Series "real power" range of solar modules. Our industry leading warranty is based on nominal power output and covers the IntegraBus™ bypass diodes, meaning more power for a longer period of time. Being one of the most powerful modules manufactured by BP Solar, the BP 7175 is ideal for installations where high power is needed in a limited area. The BP 7175 has been especially designed for grid connect applications such as large commercial roofs, residential systems and photovoltaic power plants.

Performance

Rated power	175W
Module efficiency	13.9%
Nominal voltage	24V
Warranty	90% power output over 12 years 80% power output over 25 years Free from defects in materials and workmanship for 5 years

Configuration

BP 7175S	Clear Universal frame with output cables and polarized Multicontact (MC) connectors
BP 7175L	Unframed laminate version of the BP 7175S

Qualification Test Parameters

Temperature cycling range	-40°C to +85°C for 200 cycles
Damp heat test	85°C and 85% relative humidity for 1000h
Front & rear static load test (eg: wind)	2400 Pa
Front load test (eg: snow)	5400 Pa
Hailstone impact test	25mm hail at 23m/s from 1m distance

Quality and Safety

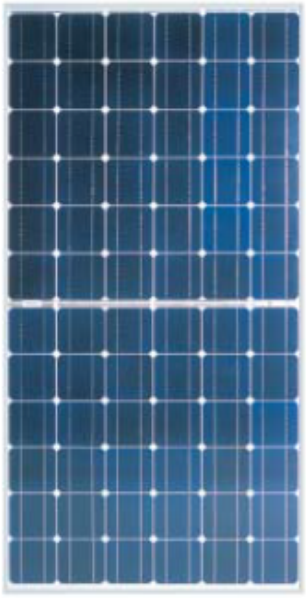
- Manufactured in ISO 9001 and ISO 14003 certified factories
- Conforms to European Community Directives 89/33/EEC, 73/23/EEC, 93/68/EEC
- Certified to IEC 61215

Module power measurements calibrated to World Radiometric Reference through ESTI (European Solar Test Installation at Ispra, Italy)

Framed modules certified by TÜV Rheinland as Safety Class II (IEC 60364) equipment for use in systems up to 1000 VDC

Framed modules listed by Underwriter's Laboratories for electrical and fire safety (Class C fire rating)

Laminates classified by Underwriter's Laboratories for electrical and fire safety (Class C fire rating)

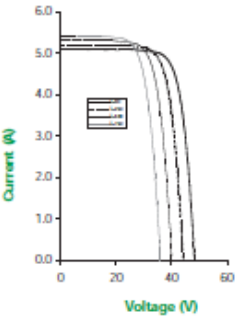


BP 7175S scale 1:14

Efficiency (%)

9-11	11-12	12-13	13-14	14-15

BP 7175 I-V Curves



B2 SolarMagic Power Optimiser

SM1230-3A1/4A1/3B1/4B1 SPECIFICATIONS

SolarMagic™
by National Semiconductor

SolarMagic power optimizers SM1230-3A1/3B1/4A1/4B1 specifications

20-Year Warranty
All SolarMagic power optimizers come with a limited 20-year warranty, ensuring the reliability of the panel-mounted electronics matches the panels themselves.

Electrical Operating Parameters

SM1230-3A1/4A1 — Operating Specifications

Symbol	Parameter	Min	Typical	Max
V_{SYS}	UL System String Voltage			600 Vdc
	CE System String Voltage			1000 Vdc
V_{MPP}	PV Module MPP Voltage	15 Vdc	28 Vdc	40 Vdc
I_{MPP}	PV Module MPP Current			8.5A
P_{MPP}	PV Module Power	5W		230W
V_{OC}	PV Module Open-Circuit Voltage			50 Vdc
$I_{SC\ (OCP)}$	PV Module Short-Circuit Current Over-Current Protection Threshold	9.2A		10.4A
V_{OUT}	Output Voltage	0 Vdc		43 Vdc
I_{OUT}	Output Current	0A		8.5A
η	Efficiency		98.5%	
T_A	Operating Temperature	-40°F (-40°C)		158°F (70°C)

Electrical Operating Parameters

SM1230-3B1/4B1 — Operating Specifications

Symbol	Parameter	Min	Typical	Max
V_{SYS}	UL System String Voltage			600 Vdc
	CE System String Voltage			1000 Vdc
V_{MPP}	PV Module MPP Voltage	30 Vdc	56 Vdc	80 Vdc
I_{MPP}	PV Module MPP Current			5.5A
P_{MPP}	PV Module Power	5W		230W
V_{OC}	PV Module Open-Circuit Voltage			100 Vdc
$I_{SC\ (OCP)}$	PV Module Short-Circuit Current Over-Current Protection Threshold	5.9A		6.4A
V_{OUT}	Output Voltage	0 Vdc		86 Vdc
I_{OUT}	Output Current	0A		5.5A
η	Efficiency		98.5%	
T_A	Operating Temperature	-40°F (-40°C)		158°F (70°C)

Physical Specifications:

Model	Body Dimension	Weight	Connector Type
SM1230-3A1 SM1230-3B1	5.27" x 4.24" x 1.86" (13.4 x 10.8 x 4.7 cm)	2.3 lbs (1.1 kg)	MC3
SM1230-4A1 SM1230-4B1	5.27" x 4.24" x 1.86" (13.4 x 10.8 x 4.7 cm)	2.3 lbs (1.1 kg)	MC4

Safety and conformance certifications
Each SolarMagic power optimizer is designed and tested to comply with the appropriate sections of the UL 1741, IEC 61010 and IEC 60529 standards.

SolarMagic blocking diodes SM2060-3A1/4A1/SM2100-3A1/4A1 specifications

20-Year Warranty
All SolarMagic blocking diodes come with a limited 20-year warranty.

Electrical Operating Parameters

SM2060-3A1/4A1 — Operating Specifications

Symbol	Parameter	Min	Typical	Max
V_{SYS}	System voltage			600 Vdc
I_{IN}	Input current (PV I_{SC})			9A
V_F	Forward voltage drop		0.7 Vdc	1.26 Vdc
η	Efficiency		99.80%	
T_A	Operating Temperature	-40°F (-40°C)		158°F (70°C)

Electrical Operating Parameters

SM2100-3A1/4A1 — Operating Specifications

Symbol	Parameter	Min	Typical	Max
V_{SYS}	System voltage			1000 Vdc
I_{IN}	Input current (PV I_{SC})			9A
V_F	Forward voltage drop		0.7 Vdc	1.26 Vdc
η	Efficiency		99.80%	
T_A	Operating Temperature	-40°F (-40°C)		158°F (70°C)

Physical Specifications:

Model	Body Dimension	Weight	Connector Type
SM2060-3A1 SM2100-3A1	3.93" x 3.33" x 1.68" (10 x 8.45 x 4.28 cm)	12.5 oz. (0.36 kg)	MC3
SM2060-4A1 SM2100-4A1	3.93" x 3.33" x 1.68" (10 x 8.45 x 4.28 cm)	12.5 oz. (0.36 kg)	MC4

Visit www.solarmagic.com and click Partner Portal for design support and more information

www.solarmagic.com

650101-001

B3 BP Solar MSX 60/64 PV Module

Typical Electrical Characteristics[1]	BP MSX 60	BP MSX 64
Maximum Power (P_{max})[2]	60W	64W
Voltage at P_{max} (V_{mp})	16.8W	17.5V
Current at P_{max} (Imp)	3.56A	3.66A
Warranted minimum P_{max}	58W	62W
Short-circuit current (I_{sc})	3.87A	4.0A
Open-circuit voltage (V_{oc})	21.0V	21.3V
Temperature coefficient of I_{sc}	(0.065±0.015)%/°C	
Temperature coefficient of V_{oc}	-(80±10)mV/°C	
Temperature coefficient of power	-(0.5±0.05)%/°C	
NOCT[3]	47±2°C	
Maximum system voltage[4]	600V	

Notes

1. These data represent the performance of typical BP MSX 60 and BP MSX 64 modules as measured at their output terminals, and do not include the effect of such additional equipment as diodes or cables. The data are based on measurements made in accordance with ASTM E1036-85 corrected to SRC (Standard Reporting Conditions, also known as STC or Standard Test Conditions), which are:

   • illumination of 1 kW/m² (1 sun) at spectral distribution of AM 1.5 (ASTM E892-87 global spectral irradiance);

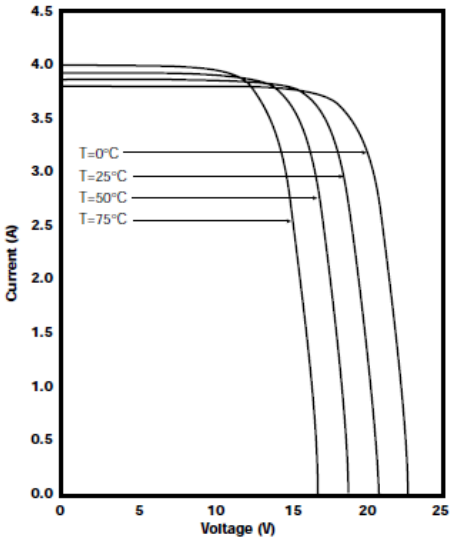
   • cell temperature of 25°C.

2. During the stabilization process which occurs during the first few months of deployment, module power may decrease approximately 3% from typical Pmax.

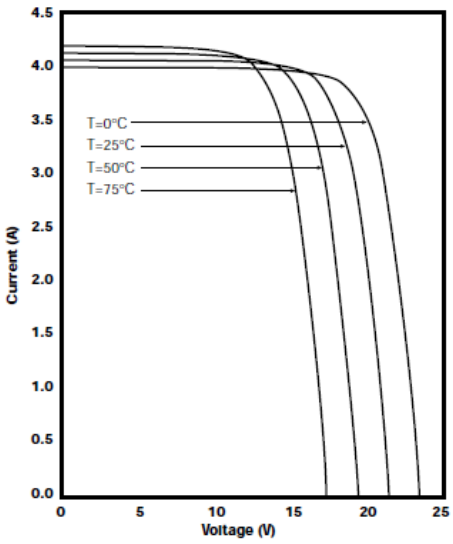
3. The cells in an illuminated module operate hotter than the ambient temperature. NOCT (Nominal Operating Cell Temperature) is an indicator of this temperature differential, and is the cell temperature under Standard Operating Conditions: ambient temperature of 20°C, solar irradiation of 0.8 kW/m², and wind speed of 1 m/s.

4. U.S. NEC rating.

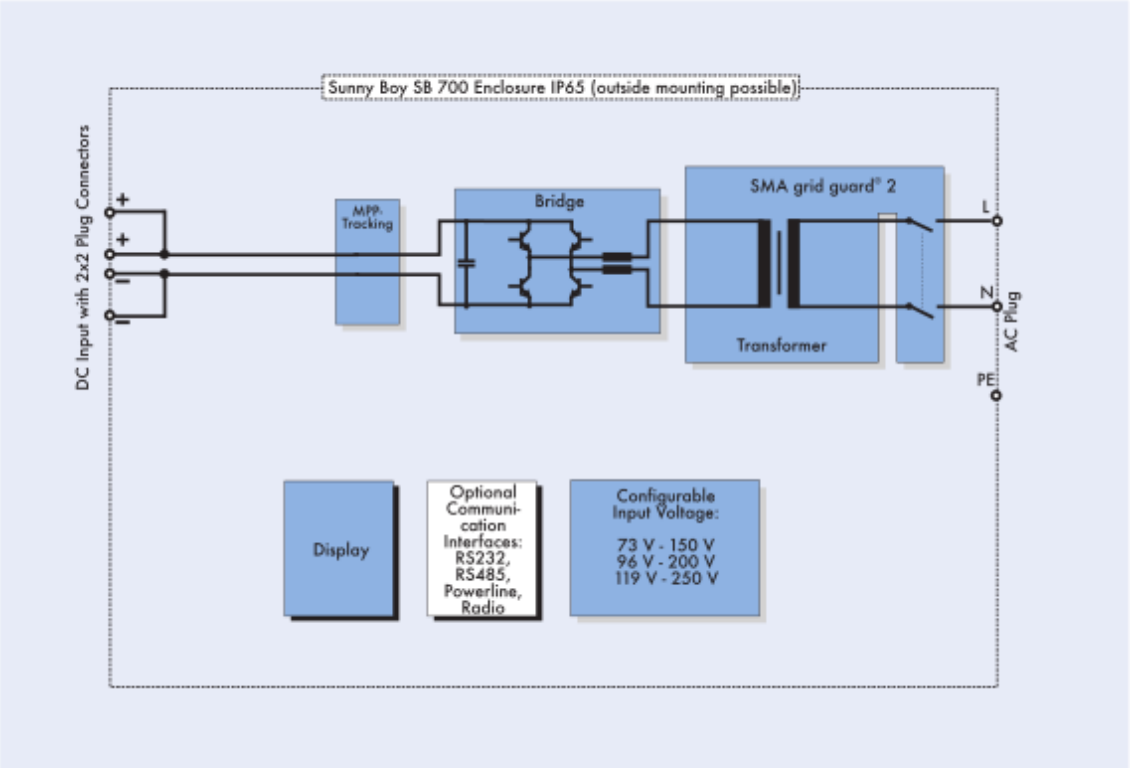
BP MSX 60 I-V Curves



BP MSX 64 I-V Curves



B4 SMA SB700 PV Inverter



Schematic diagram of the Sunny Boy SB 700

Technical Data

	SB 700 (73 to 150 V)	SB 700 (96 to 200 V)	SB 700 (119 to 250 V)
Input			
Max. DC power ($P_{DC, max}$)	510 W	670 W	780 W
Max. DC voltage ($U_{DC, max}$)	250 V	250 V	250 V
PV-voltage range, MPPT (U_{PV})	73 V – 150 V	96 V – 200 V	119 V – 250 V
Max. input current ($I_{PV, max}$)	7 A	7 A	7 A
DC voltage ripple (U_{pp})	< 10 %	< 10 %	< 10 %
Max. number of strings (parallel)	2	2	2
DC disconnection	Snap cable connectors	Snap cable connectors	Snap cable connectors
Thermally monitored varistors	yes	yes	yes
Ground fault monitoring	yes	yes	yes
Pole confusion protection	Short circuit diode	Short circuit diode	Short circuit diode
Output			
Max. AC power ($P_{AC, max}$)	460 W	600 W	700 W
Nominal AC power ($P_{AC, nom}$)	460 W	600 W	700 W
THD of grid current	< 3 %	< 3 %	< 3 %
Nominal AC voltage ($U_{AC, nom}$)	220 V – 240 V	220 V – 240 V	220 V – 240 V
Nominal AC frequency ($f_{AC, nom}$)	50 Hz / 60 Hz	50 Hz / 60 Hz	50 Hz / 60 Hz
Phase shift (cos φ)	1	1	1
Short circuit proof	yes, current control	yes, current control	yes, current control
Connection to utility	AC Plug	AC Plug	AC Plug
Efficiency			
Max. Efficiency	93.4 %	93.4 %	93.4 %
Euro-eta	92 %	92 %	92 %
Enclosure			
accord. to DIN EN 60529	IP65	IP65	IP65
Mechanical Data			
Width / height / depth in mm	322 / 290 / 180	322 / 290 / 180	322 / 290 / 180
Weight	16 kg	16 kg	16 kg

B5 BP104S Photodiode

Kennwerte (T_A = 25 °C, Normlicht A, T = 2856 K)
Characteristics (T_A = 25 °C, standard light A, T = 2856 K) (cont'd)

Bezeichnung **Description**	**Symbol** **Symbol**	**Wert** **Value**	**Einheit** **Unit**
Leerlaufspannung, E_V = 1000 lx Open-circuit voltage	V_O	360 (≥ 280)	mV
Kurzschlußstrom, E_V = 1000 lx Short-circuit current	I_{SC}	50	µA
Anstiegs- und Abfallzeit des Fotostromes Rise and fall time of the photocurrent R_L = 50 Ω; V_R = 5 V; λ = 850 nm; I_p = 800 µA	t_r, t_f	20	ns
Durchlaßspannung, I_F = 100 mA, E = 0 Forward voltage	V_F	1.3	V
Kapazität, V_R = 0 V, f = 1 MHz, E = 0 Capacitance	C_0	48	pF
Temperaturkoeffizient von V_O Temperature coefficient of V_O	TK_V	– 2.6	mV/K
Temperaturkoeffizient von I_{SC} Temperature coefficient of I_{SC}	TK_I	0.18	%/K
Rauschäquivalente Strahlungsleistung Noise equivalent power V_R = 10 V, λ = 850 nm	NEP	3.6×10^{-14}	$\frac{W}{\sqrt{Hz}}$
Nachweisgrenze, V_R = 10 V, λ = 850 nm Detection limit	D*	6.1×10^{12}	$\frac{cm \cdot \sqrt{Hz}}{W}$

Appendix C Computer Programmes

This Appendix presents sections of the computer programmes used during this work that are important but were deemed unnecessary for the main body of the thesis.

C1 PVArraySim

For reference of the code and for testing the operation, a copy of the MATLAB programme PVArraySim has been included on the accompanying CD.

C2 Code for Extraction of PV Model Parameters

The code presented here extracts the 5 single-diode model parameters, as described in Appendix A, and modifies them to obtain the parameters required for the PSpice PV model of Chapter 7. For verification of the extracted parameters, the I-V characteristic is calculated and plotted against the data to which the curve was fitted.

```
%-------------------------------------------------------------------------%
%                         PV Parameter Extraction                         %
%-------------------------------------------------------------------------%
%                                                                         %
% This program calculates the single-diode model parameters from          %
% values of voltage and current at open circuit, MPP and short            %
% circuit                                                                 %
%                                                                         %
% Written by Robert Entwistle 18/09/2012                                  %
% Last modified 07/03/2013                                                %
%-------------------------------------------------------------------------%
% Close all figures and clear the workspace and command window.
clear all; close all; clc
% Load equations for parameter extraction using Newton's method.
load NewtonFunctions.mat
% Define PV cell physical constants.
q = 1.602e-19;      % Electron charge magnitude
k = 1.381e-23;      % Boltzmann's constant
% Set reference temperature
T = 298;            % Absolute temperature in K
% Set initial value for gamma
gamma = 1;          % usually 1 <= gamma <= 2
% Enter the PV module datasheet values
Voc = 44.;          % Open circuit voltage
Vmpp = 35;          % Voltage at maximum power point
Isc = 2.1;          % Short circuit current
Impp = 2.;          % Current at maximum power point
Ns = 72;            % Number of series connections
Np = 1;             % Number of parallel connections
Nbp = 6;            % Number of bypass diodes
% Calculate the initial value for the thermal voltage
Vth = gamma * k * T / q; % gamma found from Vth in iterative equations
```

```
% Set initial values for the model resistances
Rs = 0.5;           % Series resistance: usually 0.1 <= Rs <= 1
Rp = 500;           % Parallel resistance: usually 100 <= Rp <= 10000
% Set the accuracy of the variables to give at least 4 SFs
VthAcc = 1e-7;      % order of magnitude ~ 1e-2
RsAcc = 1e-6;       % order of magnitude ~ 1e-1
RpAcc = 1e-3;       % order of magnitude ~ 1e+2
% Set iteration limit
Iteration_Limit = 1000;
% Initialise variable for counting iterations
Iteration_Count = 0;
% Perform iterative algorithm until all variables are within specified
% accuracy
while (~Iteration_Count || ((VthErr > 1e-6 || RpErr > 1e-1 ||...
        RsErr > 1e-6) && Iteration_Count < Iteration_Limit))
    % Store previous values
    Rs2 = Rs;
    Rp2 = Rp;
    Vth2 = Vth;
    % Calculate next values using generalised Newton's Equations
    Rp = Rp2 - (Eq3(Isc,Ns,Rp2,Rs2,Voc,Vth2)/...
        Deriv3Rp(Isc,Ns,Rp2,Rs,Voc,Vth));
    Vth = Vth2 - (Eq1(Impp,Isc,Ns,Rp,Rs2,Vmpp,Voc,Vth2)/...
        Deriv1Vth(Impp,Isc,Ns,Rp,Rs2,Vmpp,Voc,Vth2));
    Rs = Rs2 - (Eq2(Impp,Isc,Ns,Rp,Rs2,Vmpp,Voc,Vth)/...
        Deriv2Rs(Impp,Isc,Ns,Rp,Rs2,Vmpp,Voc,Vth));
    % Calculate accuracy of variables
    VthErr = abs(Vth - Vth2);
    RpErr = abs(Rp - Rp2);
    RsErr = abs(Rs - Rs2);
    % Increase iteration count variable
    Iteration_Count = Iteration_Count + 1;
end
% Calculate Io and Iph analytically
Io = (Isc - (Voc - Isc * Rs)/ Rp) * exp(-Voc / (Ns * Vth));
Iph = Io * exp(Voc / (Ns * Vth)) + Voc / Rp;
% Extract gamma from Vth
gamma = Vth * q / (k * T);
% Calculate values of parameters used in PSpice PV model
Kv = 1 / (Ns * gamma);
Ki = Np * Io * 1e10;
% Store the required variables
PV_Data = [0 Iph Kv Ki Rp Rs Nbp;...
    Isc Iph Kv Ki Rp Rs Nbp];
% Clear MALAB workspace of unwanted variables
clearvars -except PV_Data q k T Voc
%-------------------------------------------------------------------------%
% This section generates the PV characteristic from the single-diode %
% equation using the extracted parameters. The characteristics are
%
% then plotted against the simulated curve.                               %
%-------------------------------------------------------------------------%
% Define symbolic Maths variables
syms I Iph Io Rp Rs V Vth
% Define symbolic Maths functions of the single-diode equation
f = Iph - Io * (exp((V + I * Rs)/Vth) - 1) -...
    (V + I * Rs) / Rp - I;
df = diff(f,V);
% Convert the equations into MATLAB functions
F = matlabFunction(f);
```

```
dF = matlabFunction(df);
% Remove the intermediate symbolic Maths variables and equations
clearvars -except F dF PV_Data q k T Voc
% Define the system constants
q = 1.602e-19;
k = 1.381e-23;
T = 298;
% Reload the extracted parameters
Iph = PV_Data(1,2);
Vth = k * T / (q * PV_Data(1,3));
Io = PV_Data(1,4) * 1e-10;
Rp = PV_Data(1,5);
Rs = PV_Data(1,6);
% Initialise the PV current from 0A to Isc
I = 0:0.01:PV_Data(2,1);
% Initialise the PV voltage to Voc
V(1:length(I)) = Voc;
% Calculate the PV characteristic using Newton's Method
for n = 1:length(I)
    x = 0;
    Err = 1;
    while abs(Err) > 1e-12 && x < 1000
        V2 = V(n);
        f(n) = F(I(n),Io,Iph,Rp,Rs,V2,Vth);
        df(n) = dF(I(n),Io,Rp,Rs,V2,Vth);
        V(n) = V2 - (f(n) / df(n));
        Err = F(I(n),Io,Iph,Rp,Rs,V(n),Vth);
        x = x + 1;
    end
end
% Load data for desired curve
load('13_5_11_SM1.mat')
% Plot calculated data with desired data
subplot(2,1,1)
plot(Vd1(183:3824),Id1(183:3824),V,I,V1,I)
grid on
subplot(2,1,2)
plot(Vd1(183:3824),Pd1(183:3824),V,I.*V,V1,I.*V1)
grid on

%-------------------------------------------------------------------------%
%---------------------------- END OF FILE ----------------------------%
%-------------------------------------------------------------------------%
```

C3 PSpice Models; Definitions of ABM Components

This section contains the non-essential extra details on the PSpice model.

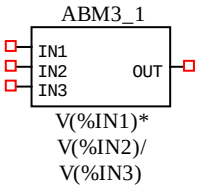
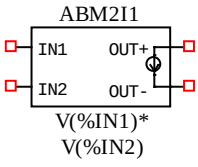
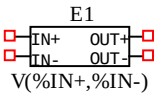
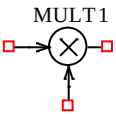
Block Name	Diagram	Description
ABMn_		ABMn_ has n single ended voltage inputs and a single ended voltage output that are referenced to the circuit ground. The output is programmed by a user set expression dependent on the inputs. A differential voltage input can be created by subtracting one input from another.
ABMnI		ABMnI has the same functionality as ABMn_ except that the output is a 2 terminal floating current source. This is useful for simulating the current drawn by a variable parallel resistance.
EVALUE		EVALUE has a 2 terminal floating voltage source output programmed by a user set expression dependent on a 2 terminal differential voltage input. The expression can be rewritten to use single ended inputs. This is useful as part of simulating the voltage dropped across variable series resistance.
MULT		MULT is a pre-programmed block that gives a single ended voltage output as a product of 2 single ended voltage inputs.
Current Controlled Voltage Source (CCVS)		The CCVS has a floating voltage source output that multiplies the current through the input terminals by a preset fixed gain. All CCVS blocks in the model convert a current for application to an ABM voltage input and are set to a gain of 1.
CONST		CONST outputs a single ended voltage which can be set by Simulink using SLPS.
Voltage Controlled Voltage Source (VCVS)		The VCVS has a floating voltage source output that takes the differential voltage between the + and – input terminals and multiplies this by a preset fixed gain. All VCVS blocks in the model are used for isolation and are set to a gain of 1.
Current Controlled Current Source (CCCS)		The CCCS has a current source output that multiplies the current through the input terminals by a preset fixed gain. All CCCS blocks in the model are used for isolation and are set to a gain of 1.

Table C3.1: Explanation of PSpice Components

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