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PERFORMANCE ANALYSIS OF SRAM CELL USING REVERSIBLE LOGIC GATES

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ABSTRACT: Reversible logic shows a great potential in the design of Low-power circuits. Remarkable work has been done in design of basic arithmetic circuits. Present day progress in sequential circuit design of reversible logic circuits has shown new ways in performance of Static random access memory (SRAM) and Dynamic random access memory (DRAM). As the memory size is increasing exponentially, the power absorbed by memory cells is also growing rapidly. In recent years reversible logic has achieved great interest because of its low power performances. This paper proposes a new SRAM cell which uses Feynman gates. The proposed SRAM cell shows reduction of 66% in terms of quantum cost, 66% reduction in quantum delay, 60% reduction in number of gates count and 50% reduction in number of transistors count.

Keywords: Arithmetic circuits, static random access memory, reversible logic, feynman gate.

1. Introduction

The integral part of any digital system is Memory. Every typical digital system require static random access memory (SRAM) for processing and storing. Several authors [1], [2] have proposed various methods of constructing SRAM arrays and shown their performance parameters. For the purpose of testing, extended peres [3] and extended toffoli [4] can be used. Static memories maintain their state as long as power is supplied to it. The high speed features of SRAM cell made it popular in memory cells.

To provide memory to a digital circuit, there are mainly two methods. The first method is to provide positive feedback that can be adjusted to make available with two stable states. Such a bistable digital circuit is used to store bit of information. Each stable state corresponds to store binary-0 and other to binary-1. In order to hold a bit of data, SRAM cell uses a bistable latch. Bistable circuit remains in one or the other state indefinitely and thus is Static. The second method is storing binary bit of information as charge on capacitor. It is treated as storing binary-1 when the capacitor is charging and as storing binary-0 when capacitor is discharging. This form of memory uses periodic recharging called "refresh" and thus is Dynamic. Now-a-days as applications of memory are increasing, interest in designing memory cells that consumes low power is also increasing.

In scaling of technology, reduction of active power requires minimizing loading from the wire by decreasing capacitance. The switching activity can be reduced by reducing the clock frequency because $P = \alpha C_L V_{dd}^2 fC LK$. Idea of low power VLSI circuits acquired great concern in present years due to its extensive applications. Reversible logic shows significant promise in designing circuits with low power. Now-a-days VLSI chips integrate megamodules, memories and random logic. Launderer [5] has suggested in that (KT)(ln2) J of energy would be dissipated in form of heat energy where K(= 1.38 × 10−23 m2 kgs−2 K −1) is Boltzmann's constant and T is temperature in kelvin for every information bit loss. Bennet [6] demonstrated that there is possibility of power dissipation becoming zero if the circuit is built with reversible logic gates. Thus reversible logic gates do not lose any information. The dissipation of energy due to loss of information is not noteworthy in present clock speed of computers. As clock speeds of computers are increased in future technologies, the dissipation plays a very important role. The energy loss in reversible logic circuits is removed by "un-computing" the information that is already computed.

Designing reversible logic is independent from designing boolean logic in following ways [7]

1) Unlike boolean logic, reversible logic circuits require equal number of inputs and outputs i.e Number of Inputs = Number of Outputs

2) Irreversible operations like feedback and fanout are not used.

3) Minimum usage of garbage outputs and constant inputs.

2. Conventional 6T SRAM Cell

A conventional 6T SRAM cell is discussed in this section and is shown in Fig.1. To store one bit of information, SRAM cell contains two cross coupled NOT gates (Inverters) which form a latch. The access transistors (T_1 and T_2) are used to connect the SRAM cell to the bit lines (BL and $\overline{BL}$) SRAM cell function in one of the following modes. Read mode, write mode or hold mode. When word line (WL) = 0 then SRAM holds the data that is stored because the access transistors T_1 and T_2 are in OFF state [15]. Word line (WL) has to be enabled to close access transistors T_1 and T_2 so that SRAM cell will read the data. To set the cell state or to check the states of BL and $\overline{BL}$, sense amplifiers are used at the bitlines. In conventional SRAM to excel the functionality, the row cells are enabled by using WL output. fredkin gates which forms a latch and MLMRG gate controls it. The total quantum cost of SRAM cell is 21 and worst case delay is given by 19.

A novel SRAM cell is designed in [16] using 3 × 3 fredkin gate and 2 × 2 feynman gate. In this paper, feynman gate and fredkin gate are used to implement latch. The quantum cost of feynman and fredkin gates are 1 and 5 respectively. Similarly the quantum delays of feynman and fredkin gate are 1 and 5 respectively.

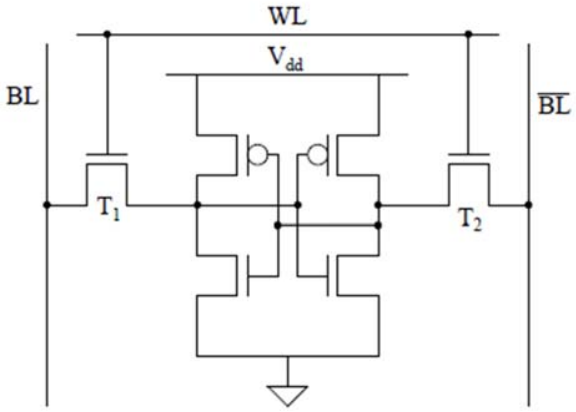

Fig. 1. SRAM cell

3. Proposed Work

This section explains the proposed SRAM using reversible logic gates. Fig.2 shows the proposed SRAM cell. As the latch consists of back to back connected inverters, it can be implemented with feynman gates, toffoli gates and fredkin gates.

But for a single XOR operation with feynman, toffoli and fredkin separately, feynman gate shows less power dissipation than toffoli and fredkin.

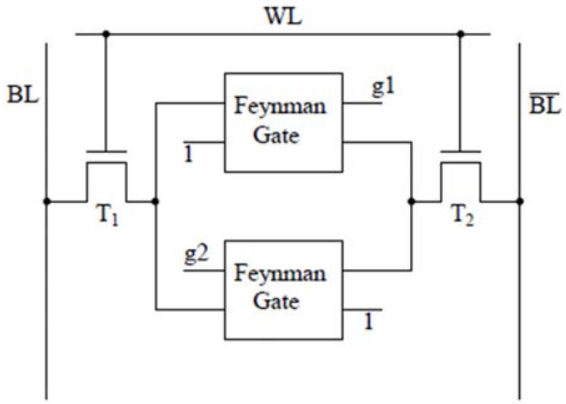

Fig. 2. Proposed SRAM cell

Thus feynman gate is used to implement an inverter (NOT gate). A latch is formed by connecting such inverters back to back as shown in Fig.2. At the time of write operation, the table 1 shows the truth table of access transistors.

Table 1:
TRUTH TABLE DURING WRITE OPERATION

Bit	WL	Stored data
0	1	0
1	1	1
X	0	No change

Table 2:

PERFORMANCE OF DIFFERENCT SRAM STRUCTURES

SRAM type	Constant Inputs	Garbage Outputs	Quantum cost	Quantum delay	Number of gates	Number of transistors
[1]	3	3	21	19Δ	5	60
[16]	1	1	6	6Δ	2	24
Proposed	2	2	2	2Δ	2	16

Fig.2 displays the proposed SRAM cell with write and read signals. SRAM cell studied in earlier section is used for storing bits of data. The data is saved in SRAM cell initially used SRAM reversible cell as explained in earlier section. The quantity saved will be transferred through 2×2 Feynman gate with binary-1 as one of the input. This generates the complement output at the output of feynman gate. It also generates a garbage output. The complement output is given as input to the other 2×2 feynman gate along with binary-1 as other input. This feynman gate also functions as inverter which is fed to the original input. In this way the back-to back connected inverter action is performed using Feynman gates. Here also a garbage output is generated. SRAM cell will either be in write mode or read mode if WL=1. Whatever the value of data input will be stored in SRAM cell if WR=1. If RD=1 and WR=0 then value saved in SRAM cell will be data output which mirror physical
Performance of proposed SRAM cell.

1) Read operation: Assuming that cell initially storing logic-1, during read operation Q is saturated at V_{dd} and Q at 0 V. The BL and BL lines are initially precharged (Pre) between 0 V and V_{dd} before the read operation begins (usually to $V_{dd}{}^{2}$). The BL and BL of SRAM cell are coupled to sense amplifier during read operation to produce output data correspondingly.

2) Write operation: Considering the write operation, assuming that cell is storing logic-1 initially and we would like to write logic-0. For this BL is discharged to 0 V, BL is charged to V_{dd} and cell is selected by making WL to V_{dd}.

The suggested architecture of SRAM cell is simulated in Cadence GPDK 180nm technology. The architecture is improved and design is minimized in terms of quantum cost and worst case delay. The garbage output of suggested architecture is 2. The quantum cost is minimized to 2 and worst case delay to 2Δ

4. Conclusion

A new SRAM cell is proposed in this paper and it is analyzed with existing designs. Decreasing garbage outputs and ancilla inputs is the most essential need in the architecture of Reversible logic. The proposed SRAM cell shows reduction in quantum cost by 66%, quantum delay by 66%. It also shows decrement of 60% in gate count and 50% in number of transistors.

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