

Time synchronization over a free-space optical communication channel: supplementary material

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This document provides supplementary information to "Time synchronization over a free-space optical communication channel," <https://doi.org/10.1364/OPTICA.5.001542>. Here, we provide a supplementary figure on the real-time implementation in a field-programmable gate array (FPGA) and on the determination of timestamps with sub-sample precision.

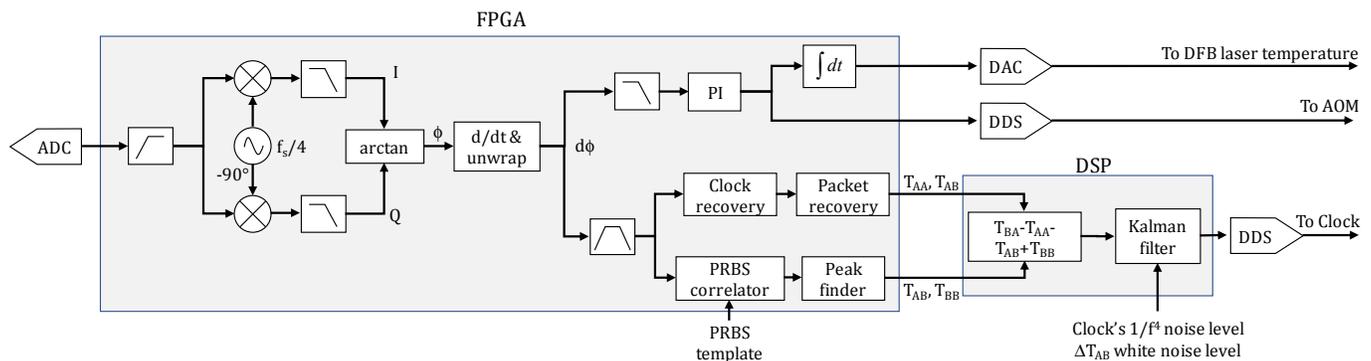


Fig. S1 Details of the frequency lock and phase demodulation at the remote site. The input to the analog-to-digital converter (ADC) is the heterodyne signal between the incoming light and local oscillator distributed feedback (DFB) laser (see Figure 1c). The signal is demodulated and then split to provide (i) feedback to stabilize the frequency of the local DFB laser, (ii) data from the master site, and (iii) timestamps from the local received pseudo-random binary sequence (PRBS) signal. As shown, a simple derivative yields the instantaneous relative laser frequency from the phase, while the data is bandpass-filtered prior to the data receiver and PRBS receiver in order to reject most of the $1/f^2$ phase noise of the DFB lasers. The local DFB laser frequency is controlled by two actuators: a fast branch by use of an AOM with a narrow frequency range, and a slow branch by use of the laser temperature to correct for larger excursions. Although not shown on the figure, the incoming signal's amplitude is measured simultaneously and compared to a threshold: if there is a sufficiently large signal, the lock is active, otherwise, it is kept in a hold mode. The feedback locks the heterodyne signal to around 250 MHz, which is in the 3rd Nyquist zone of the 200-MHz ADC. This approach avoids the extra low-frequency noise caused by the laser interference with local back reflections. The communication branch follows standard coherent binary phase-shift keying (BPSK) communication signal processing. The PRBS correlator yields the signal shown in Fig. S2, which is processed as described in the caption of Figure S2 to yield the local timestamps. These are combined with the remote timestamps, retrieved via the data link, within a digital signal processor. The resulting clock offset is fed into a Kalman filter whose output controls the local clock. FPGA: field-programmable gate array; DDS: direct digital synthesizer

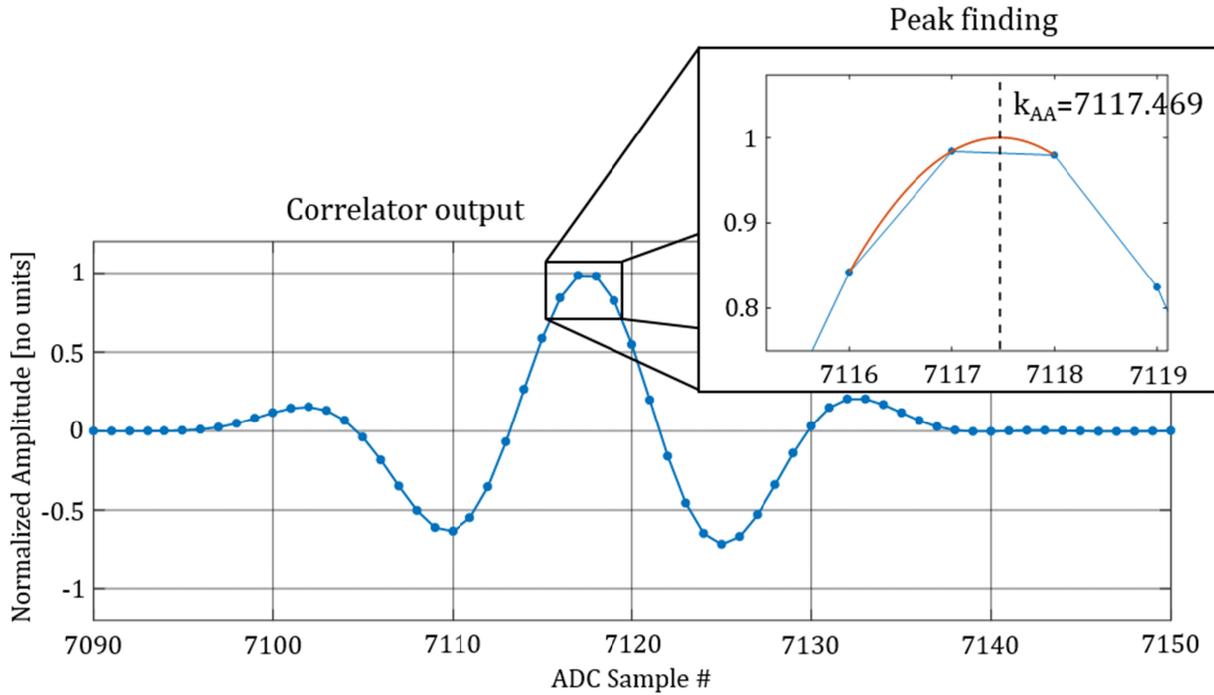


Fig. S2 Extraction of a timestamp based on a parabolic fit to the correlator output. The data here correspond to the outputs of the modules labeled “PRBS correlator” and “Peak Finding” within the receiver of Fig 1c and that of S1 above. The output of the PRBS correlator is shown versus the sample number of the local clock (blue dots). The larger structure of the correlation of the incoming PRBS waveform with the template is due to the Manchester encoding and demodulation. The correlation signal is approximately parabolic, rather than triangular, around the peak due to the factor of 20 oversampling ratio and the bandwidth limiting filters. The upper right plot displays the region of the correlation close to the peak with a parabolic fit to the three data points closest to the maximum indicated by the red line. The choice of a three-point parabolic fit made implementation on the field-programmable gate array (FPGA) straightforward and thus the computation is done in real-time with very little overhead. The vertical dashed line indicates that maximum of the parabola returned from the fit and thus the value of the timestamp with sub-sample precision. As this parabolic fit is not a perfect representation of the signal between samples, this causes (very small) errors in the peak location which follow a deterministic function of the sub-sample delay. This error is measured at calibration time and removed via a lookup table in the real-time system.