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ROCOF DETECTION

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A new algorithm and hardware for high accuracy and low latency mains voltage, phase, frequency and rate of change of frequency (RoCoF) detection.

Introduction

A high rate of change of frequency shut down the SA power network in 2016.

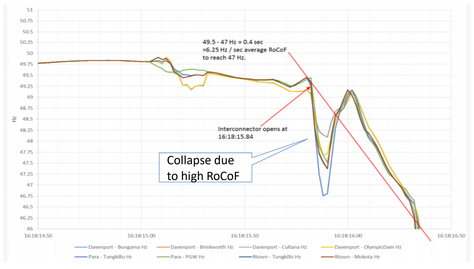

Fig. 1 SA Blackout on September 2016

Revelation: Traditional PMU is not fast and accurate enough for today's power network protection.

1. **Mains Frequency:** The key indicator of network stability.
2. **Importance:** To keep balance between supply and demand.
3. **Phasor Measurement Unit (PMU):** IEEE Std C37.118.1 requires less than 2 main cycles delay. Difficult to obtain with good accuracy.
4. **New Algorithm:** Can achieve low delay and very high accuracy.

FPGA Based PMU

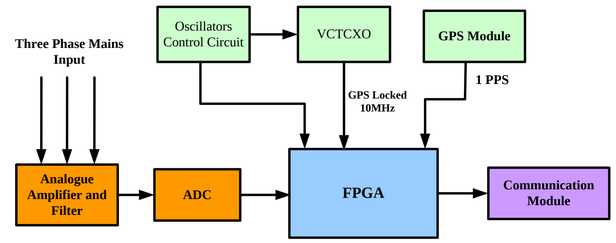

Fig. 2 System Block Diagram

1. GPS Timing and Frequency Lock

A GPS based time stamp uses on all commercial PMU for complex network stability investigations. The one pulse per second signals are used to maintain the accuracy of the system clock.

Fig. 3 GPS Timing

2. Hardware Design

Fig. 4 Analogue Input and ADC Board

Fig. 5 Frequency Lock Board

The analogue board coverts the 3ph mains input to 16-bit digital output for the FPGA.

Simulation and Implementation

1. Simulation

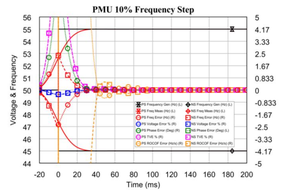

Fig.6 10% Step Frequency Change

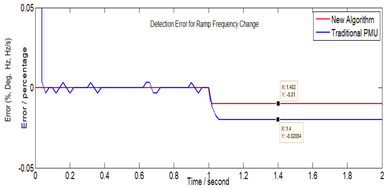

Fig.7 Detection Accuracy Comparison

IEEE Std requires detection delays no more than 3.5 mains cycles for frequency step changes. The new algorithm achieves 1.5 cycle delays. When detecting ramp frequency changes, the new algorithm has a doubled accuracy than traditional PMUs.

2. Algorithm Implementation

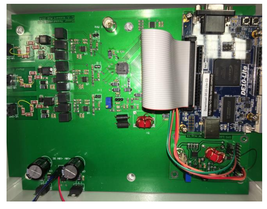

Fig. 8 FPGA with ADC Board

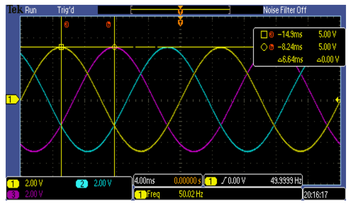

Fig. 9 Input Voltages on ADC Board

FPGA drives ADC to measure voltage signals and reads the ADC results at 10kHz. The new algorithm written in VHDL operates in the FPGA to calculate the real-time mains frequency and RoCoF.

3. Communication and Monitor

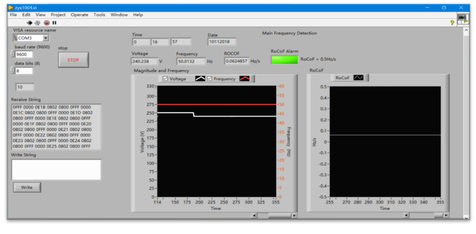

Fig. 10 Monitor Software on PC

The detection results are sent to host computers via serial communication. The communication protocol and UART are built in the FPGA using VHDL.

A monitor software is designed using LabVIEW to collect and display the PMU and GPS data.

Future Work

- Optimisation of hardware and VHDL codes.
- More functions in the host computer software such as data storage and bidirectional communication.