Study of Thermal-induced Threshold Switching Devices for Selector Applications

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Abstract

As the demand for big data applications and faster computation increases, there is an ever-growing need for memory devices with high performance, low cost, and large storage density. Emerging Non-Volatile Memory (NVM) devices such as Phase Change Memory (PCM), Resistive Random Access Memory (RRAM), and Spin-Transfer-Torque Magnetic Random Access Memory (STT-MRAM) are promising candidates for the Storage Class Memory (SCM), which was proposed to be a new class of memory devices to fill the gap between Dynamic Random-Access Memory (DRAM) and storage memory. One of the advantages of NVM is the simple two-terminal device structure, allowing for the crossbar memory array with smallest $4F^2$ (F being the lithography feature size) footprint possible. However, such structure needs an access device at each crosspoint in order to reduce the so called "sneak path" effect. The CMOS transistor could serve as an access device but it requires 12 F^2 area. Therefore, the transistor needs to be replaced by a two-terminal selector device that could be stacked on top of the memory element. Threshold switching devices appear to be the best candidate for selectors due to their extreme nonlinearity of *I-V* characteristic. However, the mechanism responsible for the threshold switching has not been well understood in many materials systems. This study focused on understanding the switching mechanism and its characterization in binary transition metal oxide-based devices.

To understand the threshold switching behavior, I have started with VO_2-based two-terminal planar devices. I developed an electrothermal model based on Joule heating to simulate the quasi-DC device *I-V* and transient response of the device under short pulses at various stage temperatures. The electrothermal model fully reproduced the *I-V* of VO_2 devices in both OFF-state

and ON-state, which allowed to follow the formation and evolution of the conductive filament within the device. The simulated dynamics of threshold switching agreed well with the experimentally measured data across 6 orders of magnitude. The good agreement between simulation and experimental results indicated temperature induced insulator to metal transition in VO_2-based devices with no evidence of electronically-induced effects. Therefore, the threshold switching behavior in VO_2-based devices can be explained by a more general Joule heating induced thermal runaway model.

Furthermore, the electrothermal model was applied to TaO_x-based threshold switches and successfully reproduced the S-shape threshold switching *I-V* characteristic due to thermal runaway mechanism. To experimentally discriminate the thermal-induced switching from other proposed mechanisms, I used Scanning Thermal Microscopy (SThM) and Scanning Joule Expansion Microscopy (SJEM), two scanning probe thermometry techniques to characterize the temperature profile and thermal expansion profile on the top surface of the TaO_x-based devices. During the measurements, the devices were biased at several voltages below and up to the threshold voltage (V_{TH}). The measurement showed that the temperature increase of 80 K was reached at V_{TH} to cause the thermal runaway leading to threshold switching behavior. The measurement results experimentally supported the Joule heating induced thermal runaway as the mechanism of threshold switching in TaO_x-based devices.

By confirming the validity of the thermal-induced threshold switching behavior, I completed a comprehensive simulation study using the electrothermal model on the scaling behavior of three transition metal oxide (VO_2, TaO_x and NbO_2) based selector devices with a vertical crossbar

structure. The device characteristic was simulated as a function of device lateral size, oxide thickness, and stage temperature. The device performance, such as *I-V* characteristic, leakage current, filament size, and temperature in the ON-state were simulated and compared between devices with different dimensions and different materials. The benchmarking of one selector/one resistor (1S1R) cell using the scaled device characteristics with a set of parameters of a generic memory element was also evaluated. Further, the ideal material properties for selector application was calculated based on the figures of merit of the device performance.

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1 Introduction

1.1 Background

The Von Neumann model has been proposed for more than 70 years and it is still an accepted architecture used in modern digital computer.[1] In Von Neumann architecture, the computer consists of four parts: (1) a central processing unit (CPU), including a control unit and an arithmetic logic unit; (2) a memory unit, containing a main memory and an external storage memory (3) an input device and (4) an output device. The memory unit is used to temporarily or permanently store the data and instructions needed to complete tasks, which is an essential part for operating the computer. There is more than one component in the memory unit, forming the memory hierarchy based on the access time of each component, shown in Table 1.1.[2] The cache usually uses static random access memory (SRAM), with a six-transistor per bit cell structure and is located very close to the CPU, having the fastest access time (1-10 CPU cycles) but the smallest capacity due to the low density. The second component in the hierarchy is dynamic random access memory (DRAM), which uses one transistor/one capacitor per bit cell structure. The smaller cell area gives larger capacity than SRAM, but the physically more distant location increases the access time to 10^2 CPU cycles. The DRAM is a volatile memory and requires periodical reading and rewriting the stored data to preserve the information, leading to extra power consumption. The last ring in the hierarchy is the main storage memory consisting of the magnetic hard drive and/or the NAND Flash memory (produced after 2009). The main storage memory is located farthest from CPU, showing the slowest access time (>10^4 CPU cycles) but the highest capacity due to the smallest bit cell area.

Table 1.1 Memory hierarchy in a computer system.

CPU Cycles	Device	Comment
10^7 - 10^8	Disk	Nonvolatile, slow and inexpensive
10^4-10^6	FLASH	Nonvolatile, fast and expensive
	SCM	Nonvolatile, fast and inexpensive
10^2	DRAM	Volatile, fast and expensive
1-10	Cache	Volatile, fast and expensive

It is obvious that there is a gap in the current memory hierarchy between DRAM and NAND Flash memory. As the increasing demand on the big data application and faster computation ability, memory devices with high performance, low cost and large storage density are always in need. The storage class memory (SCM) is therefore proposed to fill the gap with a non-volatile memory technology[2,3] that would have faster access time and be less expensive than NAND Flash memory. Another reason to investigate the new memory devices is that both DRAM and NAND Flash memory are charge-based devices,[4] which is approaching the physical scaling limit at 20 nm technology node.[5] The cell-to-cell uniformity and reliability are becoming worse and worse due to the small amount of charge stored in the scaled devices and the cost is increasing due to the difficult patterning process. As a result, a successor of the charge-based memory devices is needed in the near future as the technology node is still shrinking and will become less than 10 nm in 2019.[6]

The emerging non-volatile memory (NVM) technologies such as phase change random access memory (PCRAM),[7] ferroelectric RAM (FeRAM),[8] spin-transfer torque magnetic RAM (STT-

MRAM),[9] and resistive RAM (RRAM)[10]are considered to be promising candidates for SCM application. Among them, the STT-MRAM seems to be a good replacement of DRAM or even SRAM due to its small cell area, fast speed, low programming voltage, and long endurance.[11] RRAM and PCRAM are attractive as the SCM or replacement of NAND Flash memory because of the simple cell structure, short write/read time and lower programing voltage compared to NAND memory devices.[12] The PCM is quite mature today, having good manufacture compatibility with the silicon CMOS technology and Intel has announced the 3DXpoint™ product in 2015,[13] which is speculated to be based on phase change materials. However, RRAM devices are still under active research and this study mainly focuses on the selector devices used for RRAM application.

1.2 Resistive Random Access Memory

Resistive switching memory is a type of device that can be switched to different resistance states by application of electrical bias. For example, PCRAM is one kind of resistive switch in which the resistance of the chalcogenide material is changed between the crystalline and amorphous states.[7] The RRAM usually employs resistive switching devices with simple two-terminal vertical metal-insulator-metal (MIM) structure. There is a wide range of materials that have been reported to show resistive switching behavior, including metal oxides,[10] nitrides,[14,15] ternary perovskites,[16] and organic materials.[17,18] Among these materials, binary metal oxides have attracted the most interest due to their compatibility with CMOS fabrication process, simple structure and excellent device performance. Here, I will briefly review the metal oxide-based RRAM devices and explain their basic characteristic.

1.2.1 Basic operation of RRAM

RRAM stores the information in a form of different resistance states of the insulator layer, normally one high resistance state (HRS) and another low resistance state (LRS). Initially, the RRAM device is in a pristine resistance state after fabrication with a higher resistance than HRS. A one-time "electroforming" (or "forming") process is needed before the device can show repeatable memory switching behavior. The forming process is commonly interpreted as a soft breakdown of the oxide layer and creating a local conductive filament within the oxide layer.[19] The following resistive switching behavior is due to the formation and rupture of the conductive filament that connects the two electrodes. The operation of switching the device from HRS to LRS is called SET, and the operation of switching the device back to HRS is called RESET. The forming step usually requires higher voltage than the switching voltage that follows.

1.2.2 Classification of RRAM

According to the switching modes, the RRAM can be categorized into two groups, unipolar switching and bipolar switching. Figure 1.1 shows the typical DC *I-V* characteristic of RRAM devices. For unipolar switching (Figure 1.1a), the device can show memory switching on both polarities of the applied voltage (SET and RESET occur in the same polarity), as long as the voltage is above the switching voltage. On the other hand, for bipolar switching (Figure 1.1b), the SET and RESET occur in different polarities. Usually, the unipolar switching mode occurs in the RRAM with noble metal, such as Pt or Ru, as both top and bottom electrodes.[20, 21] If one electrode is replaced by TiN, Ti or Ta, which are oxidizable materials, the device exhibits bipolar

switching.[22] The switching mode does not simply depend on the properties of oxide material, but the combination of oxide material and the oxide/electrode interfaces.[23]

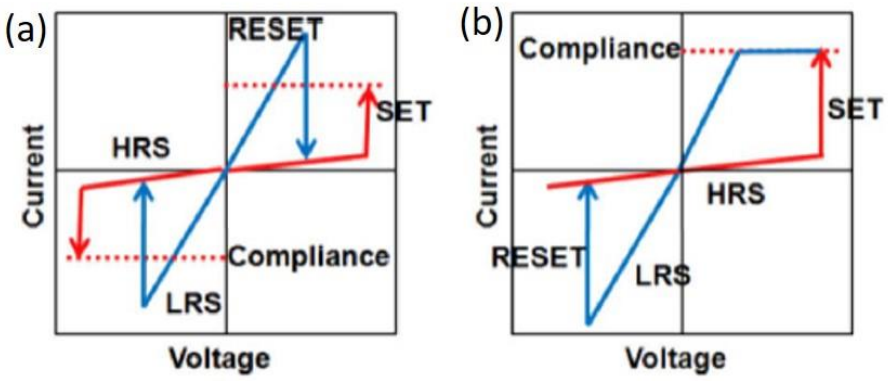

Figure 1.1 Typical DC switching *I-V* of RRAM devices. (a) Unipolar switching and (b) bipolar switching. Reprinted from reference [10].

Another categorization of RRAM is based on the type of the mobile ion. The electrochemical metallization mechanism (ECM) relies on the motion of metal cations while valance change mechanism (VCM) relies on the motion of anions.[24] The ECM cell usually consists of an electrochemically active electrode, such as Ag and Cu, and an electrochemically inert counter electrode, such as Pt and W.[25, 26] The switching mechanism of ECM is well understood and is induced by the growth and dissolution of the filament consisting of metal inclusions due to the cation migration under electric field. The metallic filament has been directly observed in TEM by Yang *et al*,[27] and is shown in Figure 1.2. The Ag/SiO2/Pt device was fabricated on an electron transparent 15 nm thick SiN membrane, with a planar device structure instead of crossbar. In this way, authors were able to directly image the device right after fabrication and during electrical testing, without destructive cross-sectional TEM sample preparation. From the TEM images, the

device was in LRS after forming and the filament was connecting the two electrodes (Figure 1.2a). After RESET, a gap was observed between the filament and the Pt electrode (Figure 1.2b). Another point to notice is that there were several partially formed filaments observed in the device, but these filaments did not contribute to the conductivity of the device.

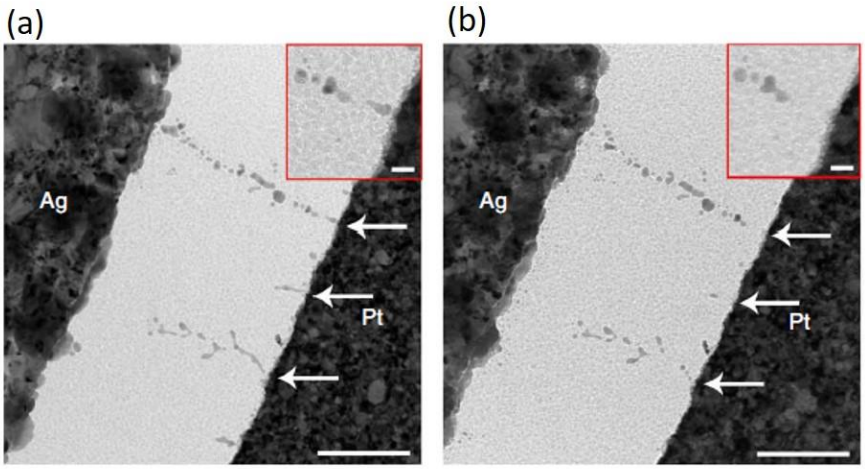

Figure 1.2 (a) TEM image of SiO_2 based CBRAM after forming. (b) TEM image of the same device in (a) after RESET. Reprinted from reference [27].

For the VCM, the switching mechanism is still under debate due to the wide range of material systems that exhibit resistive switching behavior, therefore, a universal switching mechanism may not exist. A widely accepted model is based on the motion of oxygen vacancies in the electric field and concentration gradient with a local valence change[24, 28, 29] and shown in Figure 1.3. The forming process is thought to be a "soft dielectric breakdown", during which oxygen ions are displaced from their lattice sites at the anode leaving oxygen vacancies behind.[10] If the anode material is a noble metal, the oxygen ions are discharged as neutral nonlattice oxygen, while if it is an oxidizable material, the oxygen ions react and form an interfacial oxide layer. The charged

oxygen vacancies drift under the applied electric field toward the cathode and pile up at the interface of insulator and cathode, creating the local filament. As a result, the filament consists of oxygen-deficient material, which is electrically more conductive than the surrounding region. Therefore, the current only goes through the filament region and the tip of the filament becomes the active cathode. The forming itself is a complex process that has not been well understood. Various techniques have been used to try to image and characterize the filament,[30-35] such as scanning electron microscopy (SEM), transmission electron microscopy (TEM), X-ray energy dispersive spectroscopy (XEDS), conductive atomic force microscopy (CAFM), etc. However, there are still many remaining questions related to the forming, for example, what is the composition of the filament? What is the size and shape of the filament? Is the filament created purely by oxygen leaving lattice sites or by nucleation and growth of another phase within the insulating layer?

The SET process is considered to have the same mechanism with the forming process, the oxygen vacancies drift under electric field toward cathode and the conductive filament fully connects the top electrode and bottom electrode. The difference between SET and forming is that during SET operation, the device has a partially formed filament, while the insulator layer is uniform during forming, requiring a larger voltage than SET. During RESET, the oxygen ions migrate back to the insulator layer to recombine with oxygen vacancies, forming a gap between the filament and electrode, and the device returns to HRS.[36,37]

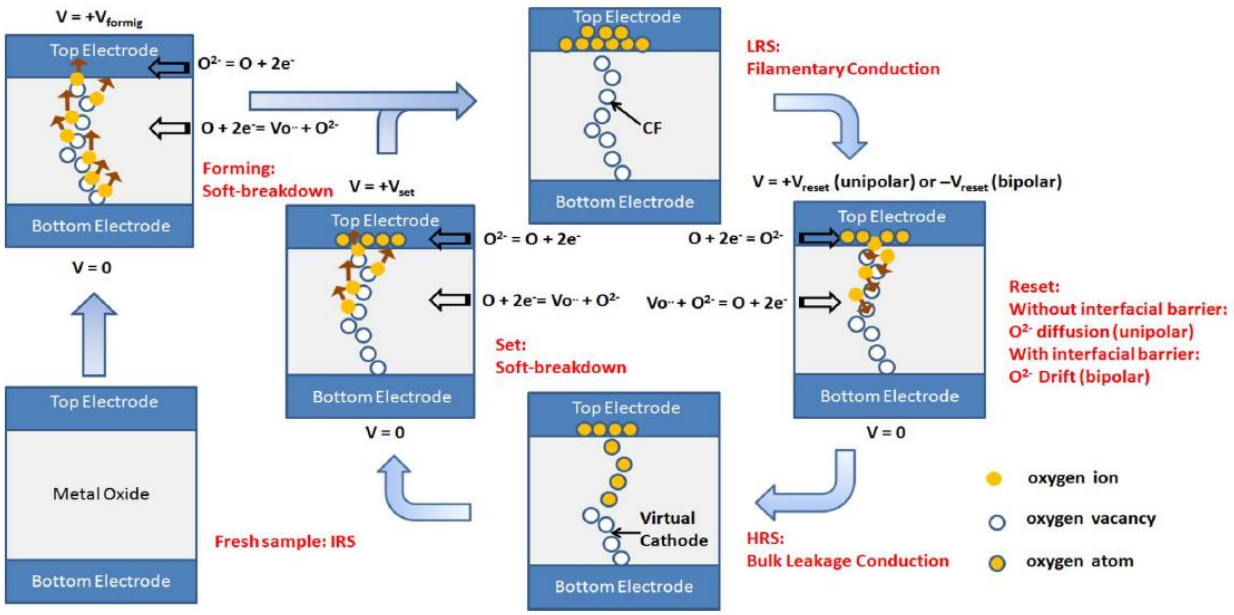

Figure 1.3 Illustration of the switching process in VCM based RRAM. Reprinted from reference [10].

1.3 Crossbar array

1.3.1 Array configuration

One of the advantages of the emerging NVM devices is the simple metal-insulator-metal (MIM) cell structure, which allows the architecture of crossbar memory array to achieve a footprint of $4F^2$, the smallest possible footprint (F: feature size of a technology node) as shown in Figure 1.4.[38] Crossbar architecture consists of perpendicular word and bit lines (Figure 1.4a), which form the bottom and top electrodes of the NVM devices, and the insulator layer is sandwiched in between at each of the crossing points. By stacking the 2D planar array into *n* layers of 3D structure, the memory density can be further increased to $4F^2/n$ shown in Figure 1.4b.

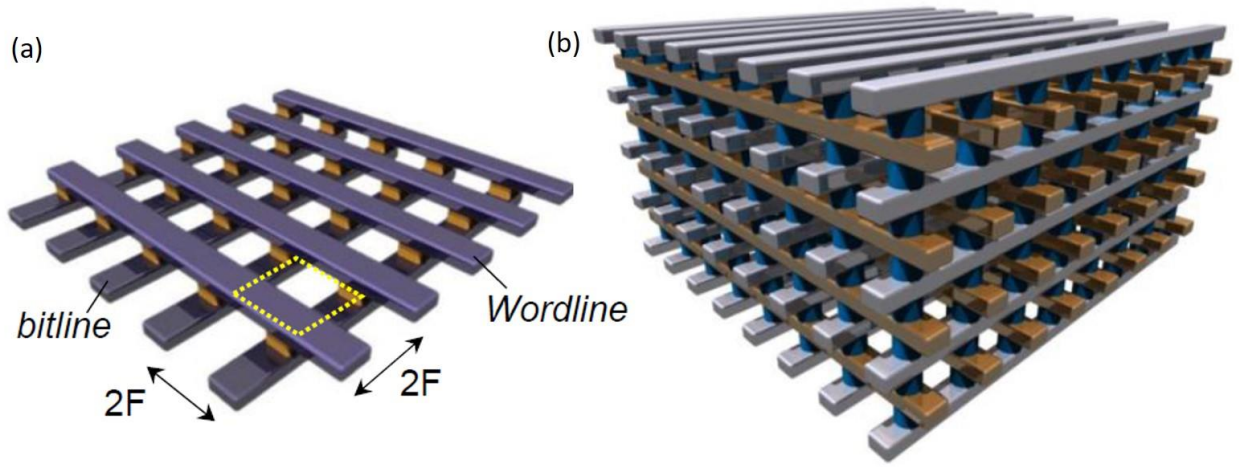

Figure 1.4 Illustration of (a) 2D cross-point array, and (b) 3D cross-point array. Reprinted from reference [38].

1.3.2 Sneak path current

Although the crossbar array is a potential candidate for the high-density memory application, it still suffers from several problems. One of them is the large sneak path current (explained below), where the leakage current is defined as the device current at half of the applied bias. To enable the memory array operation, the memory cell at each intersection of word and bit lines needs to have good selectivity, which is a high non-linearity in the device *I-V* characteristic. However, most of the reported RRAM and PCM devices have nearly ohmic behavior in both low (LRS) and high resistance states (HRS). Figure 1.5 shows a selected cell in a planar crossbar array and the example of the sneak path.[39] The write operation of the crossbar array is usually using V/2 bias scheme as shown here. In Figure 1.5, device R_j is selected with V_{dd} applied to the wordline and 0 V applied to the bitline. All the other unselected wordlines and bitlines are under bias at $V_{dd}/2$. Therefore, only R_j is under bias of V_{dd}, while the other half-selected devices along the selected wordlines and

bitlines see $V_{dd}/2$, and all the rest unselected devices are at zero voltage. The dashed line in black shows the desired current path through R_j, and the red dotted dash line shows an example of a sneak path consisting of three unselected memory cells (R_1, R_2 and R_3). In a crossbar array with *m* wordlines and *n* bitlines, there are (*m*-1) × (*n*-1) possible sneak paths consisting of three unselected cells. The total current goes through the sneak paths could be in the same order of magnitude or much higher than the current going through R_j, making it difficult to differentiate whether R_j cell is in HRS or LRS (READ error). Also, due to the line resistance, the sneak path increases the line current and reduces the effective voltage across selected cell, causing an increase of V_{dd} in order to successfully switch the selected device. The sneak current problem is getting even worse with increasing array sizes due to the possibility of more sneak paths, which limits the size of NVM array.

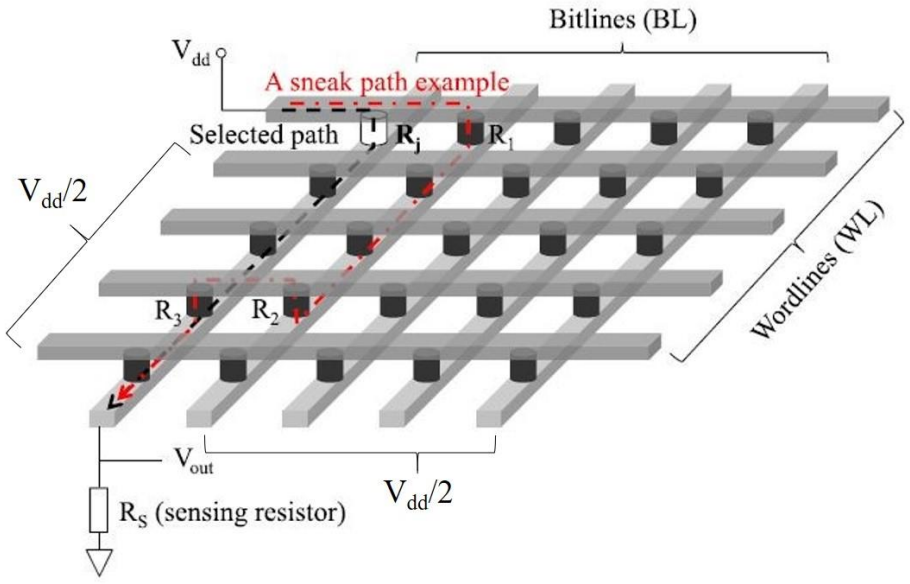

Figure 1.5 Illustration of sneak path current in a cross-point array. Reprinted from reference [39].

There are two possible solutions to solve the sneak path current problem. One approach is to use the memory cells with the non-linear *I*-*V* characteristic, referred to as the self-rectifying cells (SRC) or selector-less memory devices.[40-42] The SRC devices could consist of multiple oxide layers or a tunnel barrier layer as the functional layer to increase the resistance in the HRS and the non-linearity of the device *I*-*V*. This is a straightforward solution that does not require any changes to the existing crossbar array structure and without extra fabrication steps. However, it is very challenging to find the proper material system that can achieve all the performance requirements for NVM devices, such as long endurance, high cyclability, low cell-to-cell variation, low switching voltage and current, etc.

The other solution is to introduce another element with highly non-linear *I*-*V* characteristic into the memory cell stack, which is called a selector device. In this way, the two-terminal selector is connected in series with the memory cell at each cross point in the memory array forming one selector/one resistor (1S1R) structure. The high resistance of the selector device at low bias greatly suppresses the leakage current of the half-selected memory cells and reduces the sneak path current of the entire crossbar array.

1.4 Selector devices

1.4.1 General requirements

In order to be considered as a selector device, there are five general requirements that the devices need to meet.

(1) The selector should be a two-terminal device. Generally, the transistor can be used as a selector,

as it exhibits highly nonlinear *I-V* characteristic. The transistors, however, consume a large area with the typical $12F^2$ footprint of the one transistor/one resistor cell.[43] In addition, the cost of using transistors is also much higher due to the much more complicated fabrication processes than using simple metal-insulator-metal devices.

(2) The selector should have highly non-linear *I-V* characteristic. This is the most critical requirement for selector devices. In a memory array, there are many more unselected cells than selected ones, therefore, the selector devices should have a high resistance at low bias in the OFF-state to suppress the leakage current as much as possible, and to achieve acceptable power consumption and circuit performance. The acceptable leakage current decreases with the increasing memory array size. On the other hand, the selector device should drive enough current through the memory cell during SET and RESET operations. For example, to drive the 30 μA RESET switching,[44] the 10 nm diameter selector should have the ON-state current density of 30 MA/cm^2. The requirement for the ON-state current density depends on the memory cell, therefore, the expected value of non-linearity for the selector device is different for different memory applications, but the ON/OFF current ratio of 10^6 is desired. [45]

(3) The selector should have the highly non-linear *I-V* in both polarities. As mentioned above in Section 1.2.2, RRAM devices show both unipolar and bipolar switching modes depending on the material systems. However, most of the reported bipolar switching devices have better performance than unipolar devices, in terms of longer endurance, better cycling reliability, and lower switching power. As a result, ideally the selector device should also operate in bipolar mode for RRAM memory applications. Unipolar selector devices, such as diodes, can be used in the

unipolar PCM applications.

(4) The operation voltage of a selector should be compatible with the memory cell. In the 1S1R cell, the selector device is much more resistive in the OFF-state than the memory cell, and most of the applied voltage drops on the selector device. The switching voltage of the selector devices should enable low leakage current in both half-selected and unselected cells. The critical point in this requirement is the selector device voltage after the switching, as most of the applied voltage falls on the memory cell at this time. The voltage difference of the selector device before and after the switching should be smaller than the SET and RESET voltage of the memory cell. If not, once the selector device switches on, the memory cell would switch immediately, leading to the failure of read operation and undesired switching event. The desired switching voltage of selector devices depends on electrical property of the paired memory cell and it is better that the switching voltage can be tuned by changing the material properties during fabrication, such as film thickness and material composition, in order to accommodate the voltage requirement from memory cell.

(5) All the other device performance merits should be as good as or better than the memory cell. Since the selector device should not be the component limiting the performance of the entire crossbar array, the device properties should be better than those of the memory cell including reliability, endurance, switching speed, yield, and device-to-device variation. Also, the selector device should use materials that are compatible with traditional CMOS fabrication process. It would be better if the materials are back-end-of-line compatible in order to put the NVM array physically as close to the CPU as possible, meaning maximum fabrication temperature below 400 °C and thermally and electrically stable around 400 °C for 2 hours.[45]

1.4.2 Classification of selector devices

Currently, researchers are exploring different types and materials for selector devices,[45-47] such as Si-based PN diodes,[48,49] oxide-based diodes,[50-54] threshold switches[55-58] and Mixed Ionic-Electron Conduction (MIEC).[59] Among these devices, threshold switches are considered as the most promising candidate due to simple structure, CMOS process compatibility, and good electrical performance. Here, I will discuss different types of threshold switching devices.

1.4.2.1 Threshold switches

Threshold switching devices could be ideal for selector application, as the device turns to a highly conductive ON-state from an initially high resistance OFF-state once the threshold voltage or current is reached. Several types of threshold switching devices have been proposed for application as selectors such as ovonic threshold switches, metal-insulator-transition based devices, thermal-runaway induced threshold switches, and Ag-based oxide threshold switches.

a) Ovonic threshold switches

Ovonic threshold switch (OTS) was first reported in thin films of amorphous chalcogenide alloys.[60] A typical *I-V* characteristic of OTS is shown in Figure 1.6.[61] The device is initially in the high resistance OFF-state and switches along the load line corresponding to the resistor connected in series with the selector to the conductive ON-state as soon as the threshold voltage is reached. With the applied voltage ramping down, the device stays in the ON-state until reaching the holding voltage, and the device switches back to the OFF-state when the voltage is further reduced. Unlike

the memory switching behavior in the chalcogenide alloys, there is no permanent conductive filament formed during the threshold switching, therefore the switching is repeatable and nondestructive. The threshold switching occurs after a delay time which can be reduced by increasing applied voltage, and a ~ns switching time can be achieved.[62] Also, the threshold voltage decreases with decreasing functional layer thickness and higher stage temperature, indicating the switching mechanism is electric field dependent. The holding voltage is independent of the thickness and temperature, but it is affected by the electrode materials.[63] Koo *et al*. reported binary SiTe based OTS selector devices, showing high OFF resistance (~20 GΩ at 0.2 V), high selectivity (10^6), fast switching speed (10 ns delay time) and good endurance (> 500k cycles).[64] Alayan *et al.* integrated a GeSe based OTS with HfO_2-based RRAM to form 1S1R cell.[65] It showed a selectivity ~20 between V_{read} and $V_{read}/2$ and could withstand up to 10^6 reading cycles without any degradation in the 1S1R structure. Further, with the N and Sb doping in the GeSe material, the selectivity was improved to ~10^5 due to the formation of Ge-N bonds improving the stability in the OFF-state. Currently, the OTS devices have achieved leakage current of 10^{-11} A, ON-state current density of >1.6 MA/cm^2, selectivity >10^6 with endurance more than 10^9 cycles.[66]

One important issue for chalcogenide materials as selector devices is the failure due to crystallization. The same material system can be used as phase change memory devices where the chalcogenide functional layer crystallizes during forming process and stays in ON-state. The crystallization could be prevented by engineering the composition of the chalcogenide alloys.[67]

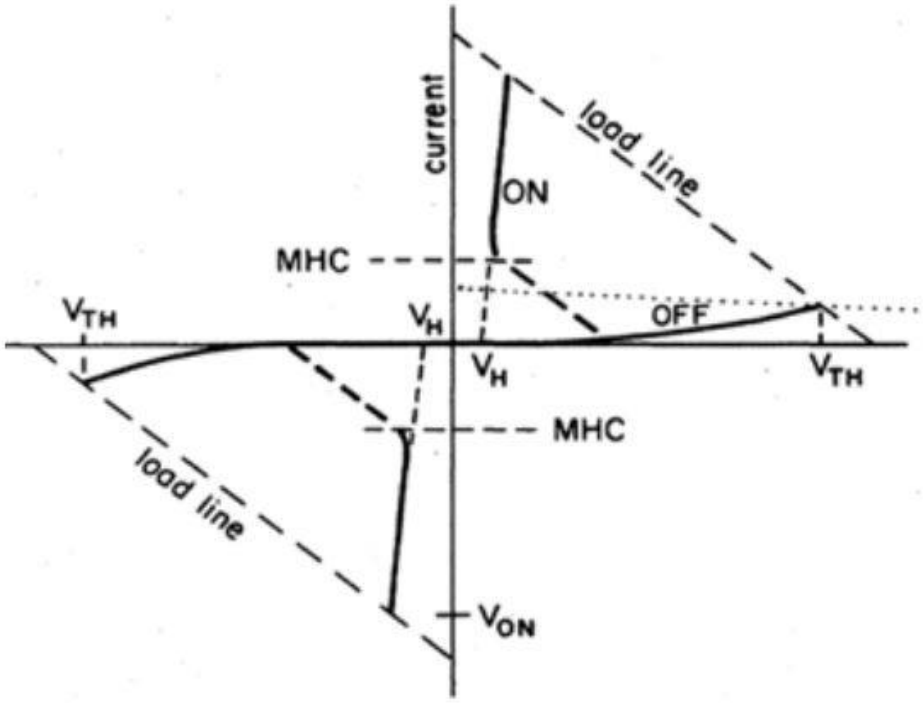

Figure 1.6 The typical *I*-*V* characteristic of ovonic threshold switches. Reprinted from reference [61].

b) Metal-insulator transition

Metal-insulator transition (MIT) behavior has been reported in many materials and can be induced by various stimuli, such as electric filed, temperature, light and pressure.[68] The electrically and thermoelectrically triggered MIT devices have become potential selector devices because of the simple MIM structure, fast switching speed, and high ON/OFF ratio. Nanoscale Pt/VO_2/Pt structure can achieve ON/OFF ratio >50, <20 ns switching time, and >1 MA/cm^2 ON-state current density.[55] Zhang *et al.* fabricated W/VO_2/Pt selector device and externally connected it to a HfO_2-based RRAM cell. With the integration of VO_2 selector, the RRAM array size can be increased from 8×8 to 128×128.[69] However, the transition temperature of MIT of VO_2 is only 67 °C, making

it not suitable for any applications that can be expected to operate at temperatures above that. Recently, Rupp *et al.* reported that the Cr doped VO_2 can achieve a higher transition temperature than bulk VO_2 and the selector devices showed stable threshold switching behavior up to 90 °C,[70] which provided a method of engineering the material properties.

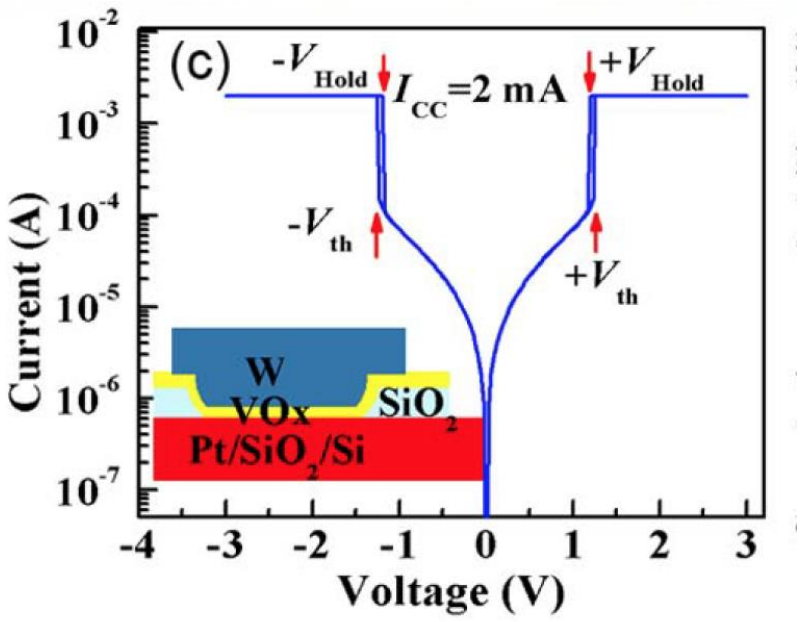

Figure 1.7 *I-V* characteristic of $W/VO_2/Pt$ selector device. Reprinted from reference [69].

NbO_2 is another candidate for MIT threshold switching material, with a much higher transition temperature (1081 K) than VO_2. The $TiN/NbO_2/W$ structure which was fabricated by Cha *et al.*[71] showed a >0.1 MA/cm^2 current density, ~500 selectivity and tunable threshold voltage by changing the NbO_2 thickness. Liu *et al.* reported that by inserting an additional Nb_2O_5 or HfO_2 layer in the MIM structure, the threshold current was further reduced due to thermal confinement in the ON-state.[72] However, the threshold voltage of NbO_2 devices is larger than VO_2 device, and leakage current is still too high to support a large memory array, which needs further engineering

and improvement.

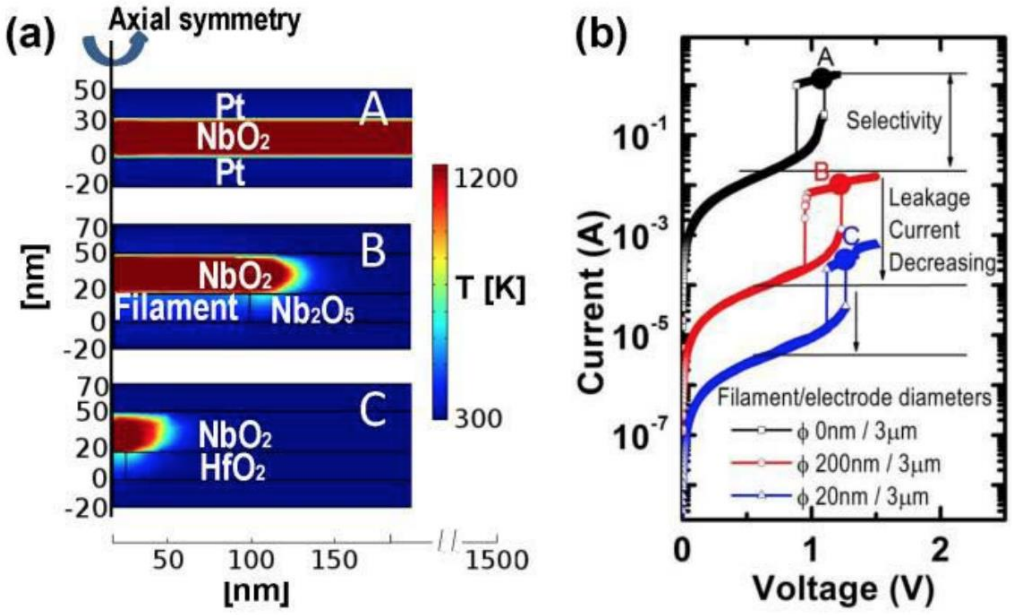

Figure 1.8 Calculated (a) temperature distributions and (b) *I*–*V* characteristics for three devices: Pt/NbO_2/Pt, Pt/NbO_2/Nb_2O_5/Pt and Pt/NbO_2/HfO_2/Pt. Reprinted from reference [72].

c) Field assisted superlinear threshold switches

Jo *et al*. reported a 4Mb 1S1R integration using a Field Assisted Superlinear Threshold (FAST) selector device.[57, 73] The leakage current was less than 100 pA using 100 nm × 100 nm device. With a selectivity of 10^{10}, the device can drive > 1 mA in the ON state. Also, the device showed sub-50 ns operation speed, >100 M endurance, and less than 300 °C process temperature. The FAST devices show larger selectivity and faster switching speed than OTS and MIT devices, but the actual material used in this selector or a mechanism of operation has not been revealed.

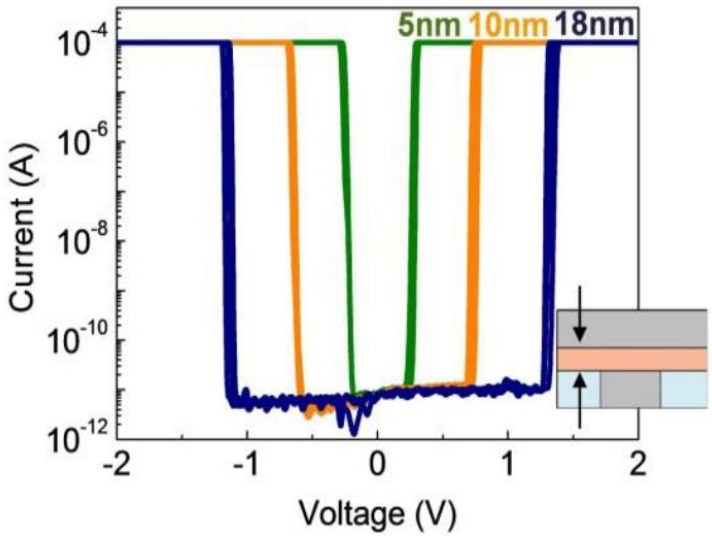

Figure 1.9 *I-V* characteristic of FAST selector with different thickness of functional layer. Reprinted from reference [57].

d) Diffusive memristors

Recently, two groups reported Ag/HfO_x based threshold switching selector devices.[58, 74] The device showed a leakage current less than 10 pA, high selectivity up to 10^{10}, and stable threshold switching up to 90 ºC. The switching mechanism is due to migration of the Ag ions under electric field to form a conducting bridge between two electrodes under. HfO_x is a poor Ag conductor and is unable to hold Ag ions in solution. Once the electric field is removed, the nanoscale Ag filament shrinks and relaxes back to the electrode due to Ostwald ripening.[75] Therefore, this type of devices has similar filament behavior as ECM but exhibits threshold switching. The switching mode can be tuned by the electrode material, as the devices show unipolar switching with only one electrode being Ag, while the device shows bipolar switching with two Ag electrodes. Several Ag/dielectric material systems have shown the threshold switching behavior, such as SiO_2,[76] MgO_x,[75] and TiO_2,[77] but Ag/HfO_x/Ag based devices showed the best performance.

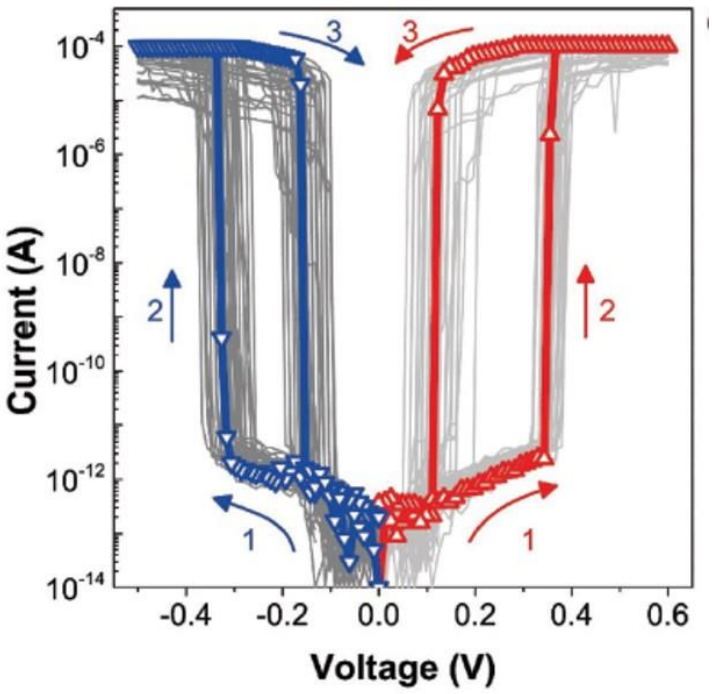

Figure 1.10 *I-V* characteristic of Ag/HfO_x/Ag based selector. Reprinted from reference [58].

1.4.2.2 Mixed ionic-electron conduction devices

IBM Research reported Mixed Ionic-Electron Conduction (MIEC) selector[59,78] based on Cu-containing material (more than 50% copper by weight) as the functional layer (the exact composition of the materials has not been revealed), which can conduct both electronic charges and ions. At low voltage, the Schottky barriers are formed at the interface of the MIEC and the electrode, leading to a low leakage current. With the increasing voltage, the Cu ions and vacancies drift within the device, modifying the interface and leading to an increase in current. The selector itself has a switching voltage less than 1V, a leakage current < 10 pA, a large selectivity (> 10^7), a high ON current density (up to 50 MA/cm^2), and >10^8 endurance. The integration of 1S1R structure with PCRAM has also been demonstrated with 35 nm device size.[79] The endurance of

more than 100k cycles was achieved with RESET pulse > 200 μA and 5μs long SET pulses at 90 μA. The concerns of the MIEC devices are the agglomeration of Cu-rich region leading to the device failure and the much lower threshold voltage than most of the demonstrated memory switching devices.

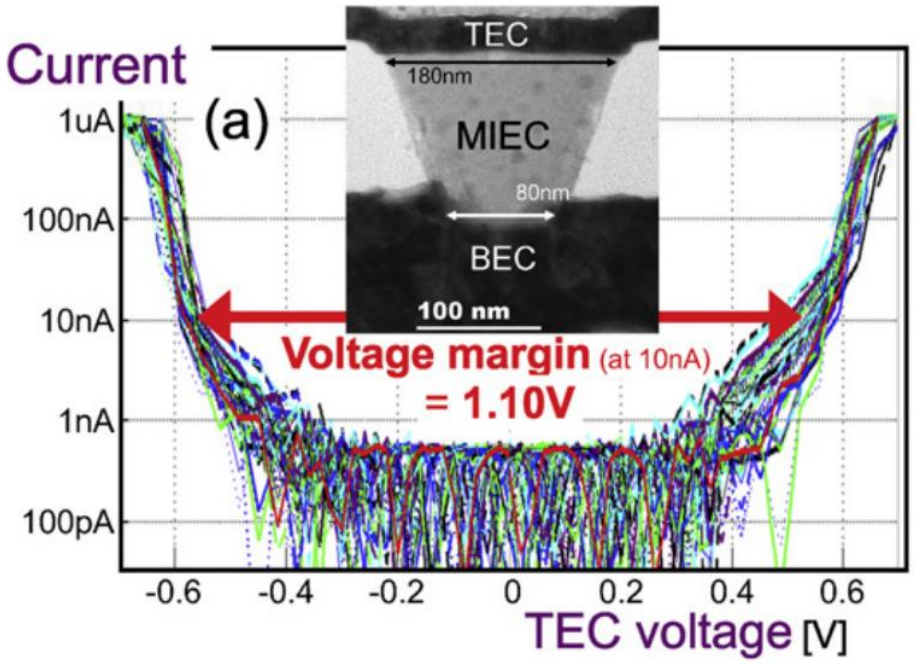

Figure 1.11 *I-V* characteristic of MIEC selector. Reprinted from reference [59].

1.4.3 Switching mechanism of threshold switches

Since the reporting of threshold switching behavior in 1968,[60] researchers have been trying to understand the mechanism behind the switching in order to not only improve the performance the devices for commercial applications but also to understand the fundamental conduction mechanism of the amorphous semiconductor materials.

Adler *et al.* proposed the purely electronic induced threshold switching mechanism for amorphous chalcogenide thin films.[61, 80] They discarded the thermal induced switching [81] because the temperature predicted by the thermal mechanism was above the glass transition of the chalcogenide materials and this high temperature would lead to gross instability in the devices. This is contrary to the threshold switching enduring up to 10^{14} ON/OFF cycles. In addition, the experimental results based on exchanging n-type and p-type Ge electrode with the same thermal property resulting in different switching characteristic strongly against the thermal model as switching mechanism.[82] Adler *et al.* argued that the current conduction involved both the electron-hole generation depending on the electric field and concentration of free carriers and the Shockley Hall Reed recombination through trap levels. In low fields, most of the generated electron-hole pairs recombine through the traps. When the free carrier generation is greatly enhanced by the electric field and concentration of free carriers, all the traps that close to the band edge are filled and the recombination rate is lower than the generation rate. This, leads to a strong increase of the density of free carriers in the conduction band and an enhanced mobility as well. Therefore, the electrical conductivity of the chalcogenide increases and the device switches to the ON-state. This mechanism can explain both the *I-V* characteristic of the amorphous chalcogenide-based threshold switches and the delay time observed prior to the switching event in short-pulse measurements.

Ielmini *et al.* developed a model based on trap-limited conduction.[83,84] Amorphous chalcogenide materials have a large concentration of traps in the forbidden gap due to the disordered atomic structure of amorphous material. Therefore, the Fermi level is located in the middle of the energy gap, resulting in a relatively large activation energy and high resistivity. The sub-threshold *I-V* characteristic is described by the Poole-Frenkel conduction mechanism, where the activation

energy is reduced by the applied electric field, enhancing the electron hopping conduction and leading to an exponential increase of the device current. The electric field and temperature effect increase the trap-limited current to a comparable degree, therefore, Ielmini referred to this combined mechanism as thermally assisted hopping. The model can also be extended to the high field region and the following threshold switching event, assuming a nonequilibrium population of shallow traps and resulting in a nonuniform electric field in the negative differential resistance (NDR) region and ON-state. This model can reproduce the device *I-V* in OFF-state, the following NDR, and ON-state regions (Figure 1.12), but it may not be applicable to crystalline materials due to the assumption of a deep Fermi level and large concentration of traps.

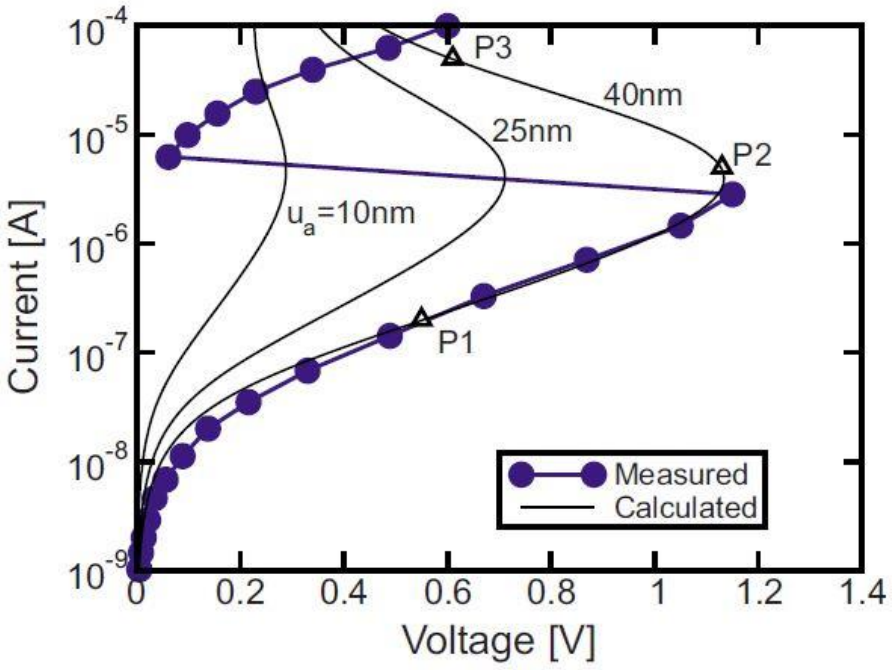

Figure 1.12 Measured and calculated *I-V* characteristic of amorphous $Ge_2Se_2Te_5$ devices. Reprinted from reference [84].

Karpov *et al.* proposed a field induced nucleation model for chalcogenide-based devices.[85,86] The

energy barrier for the formation of a conductive nucleus (second phase) is lowered by the electric field and accordingly, the critical size of the nucleus is smaller in the presence of the field. The presence of the conducting nucleus in the highly resistive material reduces the electrostatic energy and free energy of the device. In Karpov's model, the nucleation starts with a needle-shaped embryo, which concentrates the electric field and facilitates the growth of nucleus by adding ions at its end. Once the filament fully connects the two electrodes, the threshold switching happens as the device resistance greatly diminishes and the current only flows through the conductive filament. If the electric field is removed before the nucleus reaches the critical size, the filament dissolves and the device switches back into the high resistance OFF-state, showing the threshold switching behavior. The evidence supporting the nucleation model is that it can reproduce the delay time before the switching event in amorphous chalcogenide-based devices, which agrees well with the experimentally measured data at various stage temperatures.[85] Further, the nucleation model was applied to other material systems, such as VO_2,[87] TaO_x[88] and NbO_2[89] based threshold switches and showed agreement with the measured delay times.

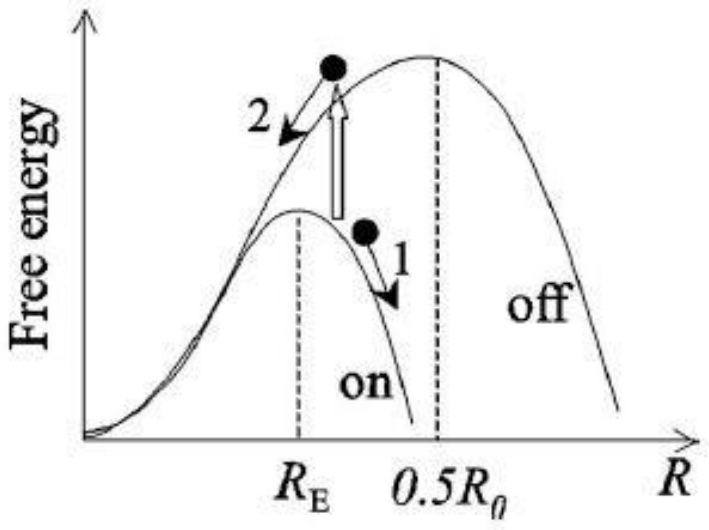

Figure 1.13 The free energy of the nucleus vs its radius for the cases of on and off electric field. Arrows 1 and 2 represent the filament radial growth and decay when the field is off, respectively. Reprinted from reference [86].

Recently, several papers have reported a thermal runaway mechanism for threshold switches based on NbO_2 and TaO_x devices.[90-93] The model uses Poole-Frenkel formula to describe the electrical conductivity of the oxide material with both the electric field and temperature contributing to the increase of conductivity. With the applied voltage, the current in the device leads to Joule heating and increases the device temperature. The temperature and current forms a positive feedback loop due to the conductivity vs temperature profile, where the increased temperature in turn increases the current. At certain value of the feedback gain, the temperature runs away and the device switches to the ON-state. The model suggests that the threshold switching in NbO_2 based devices is not due to the MIT at 1080 K, as the temperature increase in the devices at switching point is less than 150 K.[90] The evidence of this model is that it can successfully reproduce the device *I-V*

characteristic in OFF-state, NDR region and the ON-state at different stage temperatures as shown in Figure 1.14.

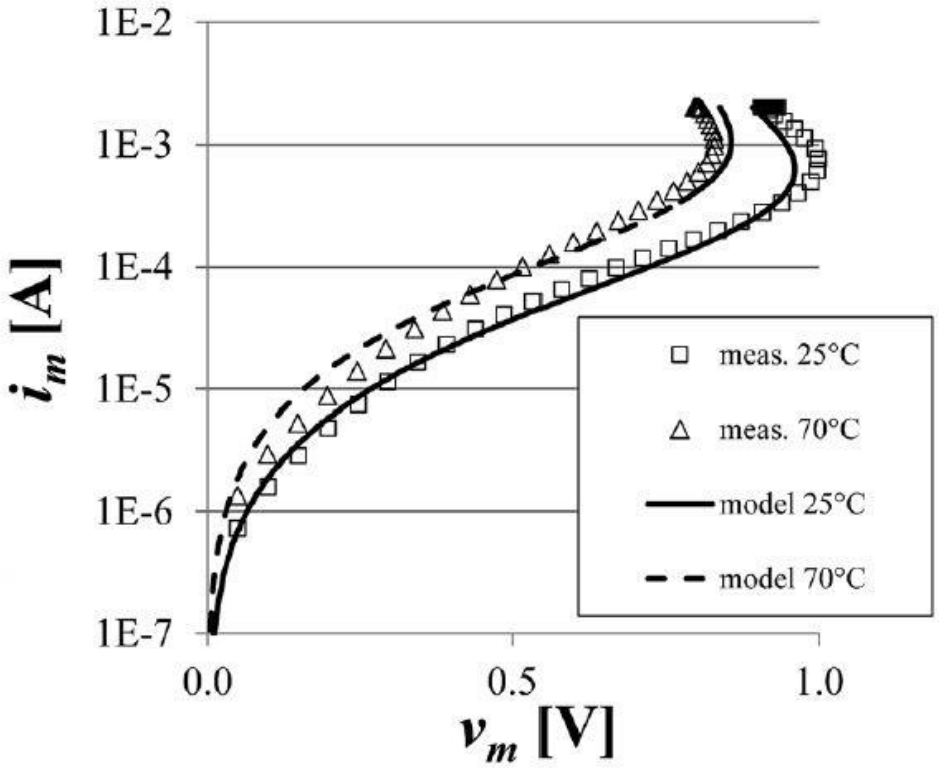

Figure 1.14 Measured and calculated NbO_2 device *I-V*. Reprinted from reference [90].

1.5 Thesis objective and outline

The research on emerging NVMs has been ongoing for more than two decades and ~ns switching, μA programming current, and up to 10^{12} endurance cycles have been demonstrated.[43] However, until now, only PCRAM has been successfully commercialized in the form of 3D XPoint™ Memory introduced by Intel and Micron, although the actual material used in this technology has not been revealed. The other technologies: RRAM, STT-MRAM, and FeRAM are still in the pre-

commercialization stage. For the case of RRAM, one of the major remaining challenges is the selector device that can fit all the requirements to integrate the 1S1R cell structure in a high-density crossbar array. One of the reasons that the selector device is still missing is that researchers have not fully understood the switching mechanism of the reported threshold switches. Therefore, it is difficult to engineer and optimize the device performance from the fundamental material properties and the design of device structure. This Ph.D. work is focused on the thermal-induced binary metal oxide-based (VO_2 and TaO_x) threshold switching devices to shine light on the understanding of the switching mechanism of these devices.

In Chapter 2, an electrothermal finite element model based on Joule heating effect will be presented and is used to simulate the *I*-*V* characteristic of two-terminal planar VO_2-based threshold switches. The VO_2 devices were experimentally tested at various stage temperatures to measure the device *I*-*V* and incubation time before the switching event. The comparison between the experimental data and simulation results will be presented, indicating that the thermal effect fully explains the threshold switching in VO_2 devices.

In Chapter 3, the electrothermal model developed in Chapter 2 is applied to TaO_x-based selector devices to reproduce the device *I*-*V* characteristic. The direct temperature measurements of TiN/TaO_x/TiN threshold switches using the Scanning Thermal Microscopy (SThM) and Scanning Joule Expansion Microscopy (SJEM) will be presented. The measured device temperature profile is compared to the electrothermal simulation results, yielding the experimental confirmation of the thermal runaway model as the mechanism of the threshold switching in TaO_x-based devices.

In Chapter 4, based on the understanding of the switching mechanism of VO_2 and TaO_x-based threshold switches discussed in the previous two chapters, a comprehensive scaling study on VO_2, TaO_x and NbO_2 (already reported to have thermal-induced threshold switching) based selector devices using the electrothermal model will be presented. The size of the vertical metal-insulator-metal device structure is scaled down to 10 nm in diameter and the device performance, such as device *I-V*, current density, and temperature in the ON-state as a function of device diameter and oxide thickness are extracted from the simulations. Further, a benchmarking analysis of these scaled devices connected to a generic phase change-like memory element forming 1S1R cell structure is discussed. In the end, the ideal material properties for selector application is calculated.

Chapter 5 will summarize the main results, list the main contributions, and discuss the possible future work based on the understanding from this work.

2 Electrothermal model of threshold switching of VO_2-based devices

2.1 Introduction

Vanadium dioxide (VO_2) undergoes an insulator-to-metal transition (IMT) at 68 ^oC [94] corresponding with a structural phase transition from an insulating monoclinic phase to a metallic tetragonal phase.[95] At the transition point, the electrical resistivity of VO_2 changes by several orders of magnitude, making it a potential candidate for many transformative applications, such as threshold switching devices,[55,96,97] field effect transistors,[98,99] and oscillators.[100-102] In two terminal devices, IMT materials show a threshold switching behavior when the voltage across it exceeds a certain 'threshold' value. At this point, the resistance of the device decreases by several orders of magnitude and remains low as long as the voltage exceeds another value V_{HOLD} referred to as the "holding voltage".[103] At biases below V_{HOLD}, the device returns to its initial high resistance state, as shown in Figure 2.1.[104]

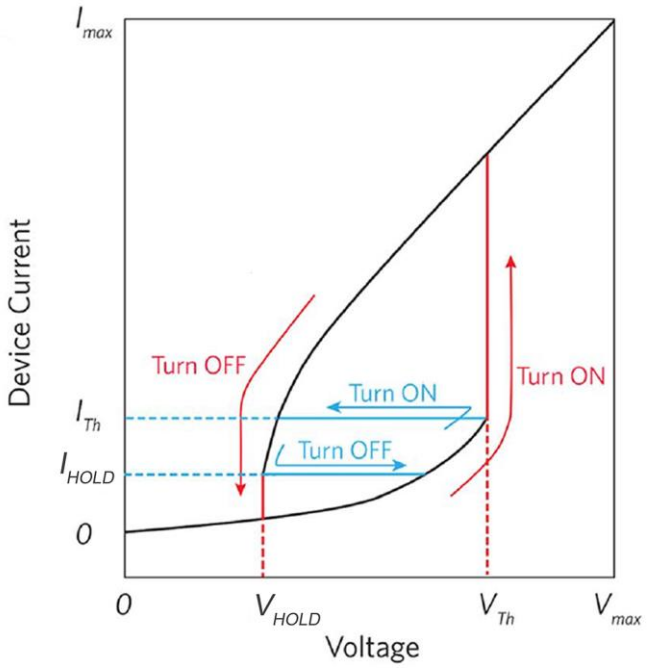

Figure 2.1 *I-V* characteristic of VO_2 devices. Reprinted from reference [104].

It has been a long-standing question whether the transition from an insulator to a metal that is responsible for the resistance change is caused by the increase of the temperature above the transition point due to Joule heating, or by other effects. The difference is an important one from the point of view of applications: the electric field or carrier injection-based mechanism could open a wide range of possible ultrafast device applications.

The arguments for Joule heating-induced transition were based on DC bias or low frequency pulse measurements. Mun *et al.*[105] measured the threshold voltage at different stage temperatures and argued that the dependence agrees with the Joule heating effect. Radu *et al.*[106] measured the threshold voltage values as a function of electrode separation and power necessary to switch the structure to the ON-state and found that both change in agreement with the thermal model. Lee *et*

al.[107] applied low frequency triangular pulses to lateral structures and measured the dependence of the threshold voltage (V_{TH}) and V_{HOLD} as a function of frequency, load resistor, and stage temperature, also obtaining good agreement with the Joule heating model. The most direct argument was presented by Zimmers *et al.*[108] who measured the temperature of the functional layer during quasi-DC voltage sweep by monitoring the fluorescence of micron size particles deposited on the VO_2 layer. The temperature in all cases corresponded to the transition temperature of the IMT when the resistance drop was observed.

The evidence in support of the non-thermally induced transition ranges from simulations of the temperature distribution in devices under DC bias, which show that the device could not reach the transition temperature,[109,110] to ultrafast voltage or light pulse experiments which monitored the delay time for the transition. All fast pulse experiments indicated that the transition occurred before the device could reach the transition temperature.[96,111-113] Two groups argued that the switching time[114] or power necessary for switching[115] are independent of stage temperature which is in clear contradiction with the thermally induced transition. Concomitantly, others have produced evidence of IMT being due to carrier injection from electrodes,[116,117] by photoexcitation[118,119] or by avalanching.[120-122]

In this Chapter, an electrothermal finite element model based on Joule heating effect is presented. Using VO_2 as a model material, the simulation results on the threshold switching device behavior is compared with the experimental data to investigate the mechanism of threshold switching in VO_2-based devices.

2.2 Two-terminal VO_2-based devices

The two-terminal VO_2-based threshold switching devices were provided by Prof. Schlom's group at Cornell University and Prof. Datta's group at University of Notre Dame.

10 nm-thick VO_2 thin films used in this work were grown on TiO_2 (001) substrates by reactive molecular-beam epitaxy in a Veeco GEN10 system.[123] The layer thickness was less than the critical thickness (30 nm) and films were fully strained. The two-terminal devices were fabricated with 20 nm thick Pd/80 nm thick Au metal stack electrodes and a 6 μm (length) by 10 μm (width) VO_2 channel.[124] A plan view SEM image of the device is shown in Figure 2.2a. The devices were tested using a variable temperature Lakeshore cryogenic probe station with a 5.5 kΩ load resistor in series during DC and pulse measurements. Figure 2.2b shows the electrical conductivity of the VO_2 film as a function of stage temperature measured at 0.1 V applied voltage. The transition temperature was determined to be 272 K, lower than the normal transition temperature because of the biaxial in-plane tensile strain effect.[123] The device characteristics showed some variation across the wafer with the resistances varying by up to a factor of two and the transition temperature changing by less than 2 degrees.

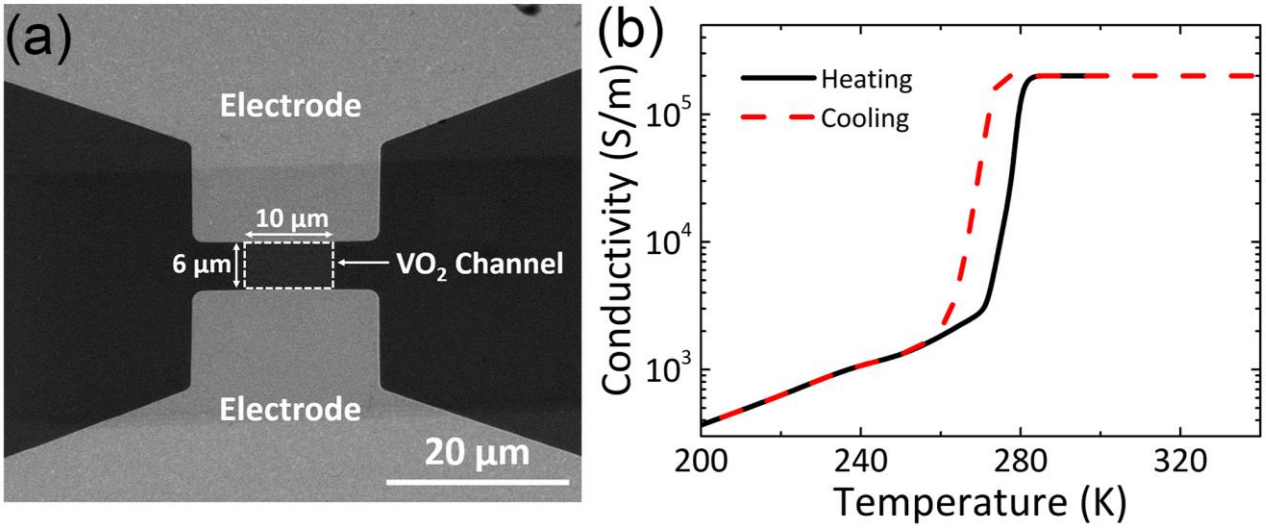

Figure 2.2 (a) SEM image showing VO_2 device layout and (b) plot of the electrical conductivity of VO_2 as a function of stage temperature. The black and red lines are, respectively, the heating and cooling curves for the conductivity.

2.3 Modeling methodology

The finite element simulation of the device *I-V* characteristic was performed using the COMSOL Multiphysics package. The 3-dimensional device geometry used in the simulation is shown in Figure 2.3. The TiO_2 substrate used in the model has a size of 750 µm length, 500 µm width and 900 µm thickness (actual thickness of the substrate), in order to reproduce the thermal environment of the chip. The size of the substrate is an important parameter in the simulation model, as a small substrate would produce a different thermal resistance than the real chip, leading to a different temperature increase of the device under bias. The substrate size was chosen by conducting a series of simulations with the same applied voltage but different substrate sizes to calculate the steady-state temperature of the VO_2 device. The simulation results suggested that a substrate of 500 µm

× 500 µm area with the 900 µm thickness is large enough to mimic the thermal environment of the real chip.

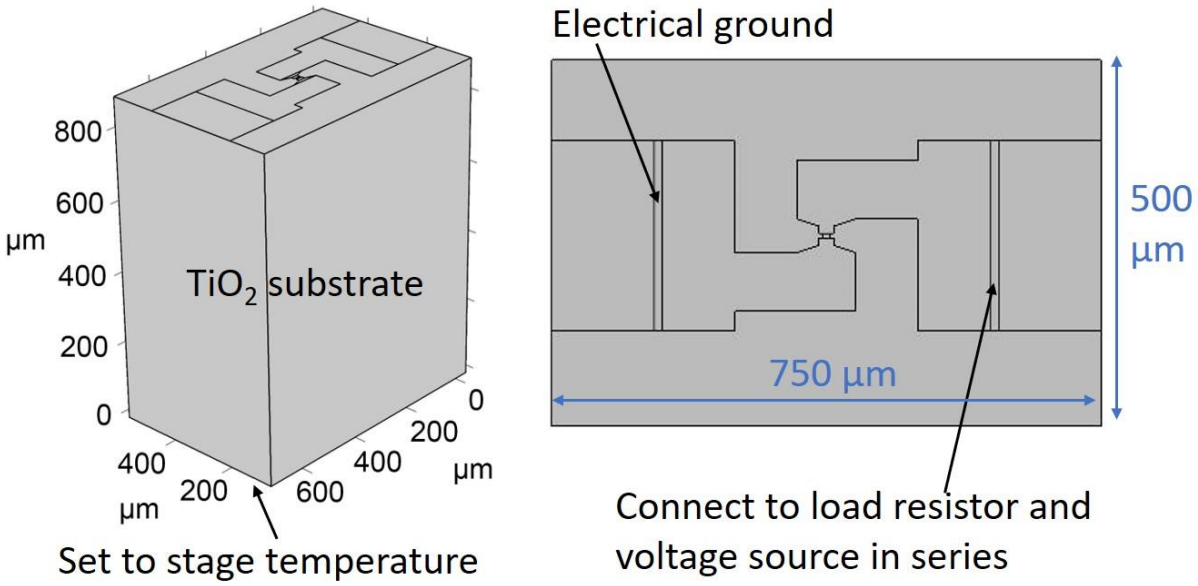

Figure 2.3 VO_2 device geometry used in the simulation model. Left: the entire device geometry, with the TiO_2 substrate of 750 µm length, 500 µm width and 900 µm thickness. Right: plan view of the top of the geometry.

To fully reproduce the experimental measurement setup, the electrical circuit model including a load resistor is coupled with the Joule heating physics model. The input parameters of the simulation are the 3-D device geometry, materials properties (thermal conductivity, material density, specific heat, electrical conductivity) for VO_2, as well as the electrodes and the substrate materials, the experimental applied voltage, the resistance of the load resistor (5.5 kΩ) and the stage temperature. The values of material properties are listed in Table 2.1.

Table 2.1 The material properties used in the simulation of VO_2-based devices.

Material	Density ($kg \cdot m^{-3}$)	Thermal conductivity ($W \cdot m^{-1} \cdot K^{-1}$)	Electrical conductivity ($S \cdot m^{-1}$)	Heat capacity ($J \cdot kg^{-1} \cdot K^{-1}$)	Relative permittivity
Au	19300	317	4.56×10^7	129	6.9
VO_2	4340	Insulating phase: 3.5 Metallic phase: 6[125]	Measured data	690	36[126]
TiO_2	4230	8	N/A	691	50

The COMSOL Multiphysics package solves two coupled differential equations. The temperature distribution *T(x,y,z,t)* in the device is the solution of the heat flow equation:

$$\rho C_p \frac{\partial T(x,y,z,t)}{\partial t} - \kappa \Delta T(x,y,z,t) = \frac{J^2(x,y,z,t)}{\sigma(T)} \quad (2.1)$$

where ρ is the material density, C_p is the heat capacity, κ is heat conductivity, J is current density, σ is the electrical conductivity and Δ is the Laplace operator. For $\sigma(T)$, I have neglected the mesoscopic structure of VO_2 induced during the IMT and used the spatially averaged electrical conductivity as a function of temperature with no dependence on electric field. The boundary conditions included the top and side surfaces being thermally insulated (no heat flux) and the bottom surface of the substrate is assumed to have a fixed temperature. Current density is obtained by solving the current continuity equation with an additional restriction imposed by the circuit that the device is part of: the source voltage was applied to the device under test and a load resistor connected in series.

2.4 Understanding the mechanism of IMT in VO_2-based devices

Figure 2.4 shows the quasi-DC *I-V* characteristic of the threshold switching behavior of the VO_2 devices at stage temperatures from 230 K to 270 K with a current compliance of 500 μA. At low

applied voltages, the *I-V* is linear. But at voltages exceeding half the threshold, the dependence becomes superlinear. This behavior is due to the temperature increase in the VO_2 channel as argued below. At the threshold voltage (V_{TH}), the device suddenly changes from the high resistance state to a low resistance state and the current reaches the compliance limit at 500 μA. Then, with the decreasing source voltage, the device switches back along the load line (marked with a thin continuous grey line) to the high resistance state. The threshold voltage varies from 15.8 V at 230 K to 3.5 V at 270 K. Thus, the electric field at the IMT, defined as V_{TH}/length of the VO_2 channel (6 μm in our case), has the highest value of 2.63 V/μm at 230 K. This value is significantly less than the estimated critical electric field (50 V/μm) required to generate sufficient carrier concentration (~ 3×10^{18} cm^{-3}) for an electric field induced IMT in VO_2.[127] The dissipated power at the onset of the IMT decreases linearly with the increasing stage temperature, from 5.7 mW at 230 K to 0.7 mW at 270 K, which is a characteristic of Joule heating driven process.

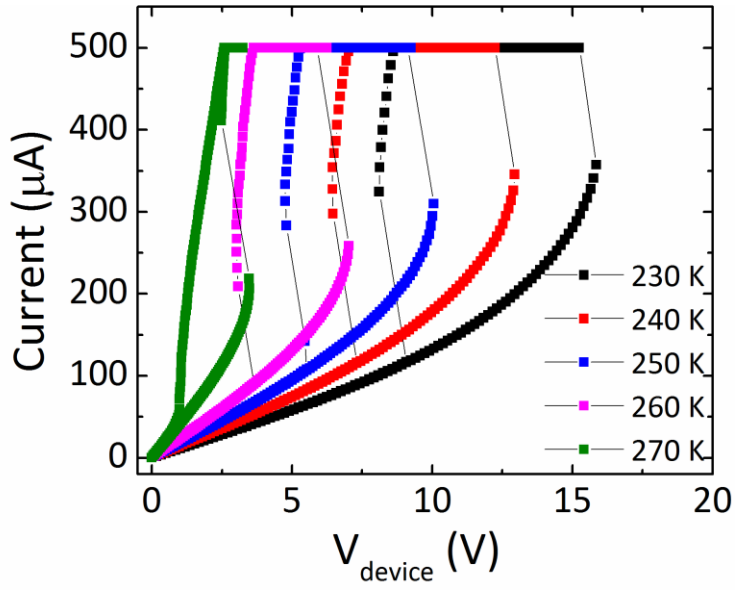

Figure 2.4 DC *I-V* characteristic of the VO_2 devices at different stage temperatures.

To understand the role of Joule heating, I have used the electrothermal model described in Section 2.3 to simulate the device *I-V* characteristics in the OFF-state at different stage temperatures. Figure 2.5a shows the measurement and simulation results at 240 K. The simulated *I-V* curve shows a good agreement with measured values. The simulated temperature profile of the VO_2 device at V_{TH} (V_{device} = 13 V, current = 350 μA) at stage temperature of 240 K is shown in Figure 2.5b. The simulation result shows that the temperature of the VO_2 channel actually reaches 270 K, the transition temperature of IMT, which indicates the mechanism of threshold switching in VO_2 devices is thermal-induced IMT.

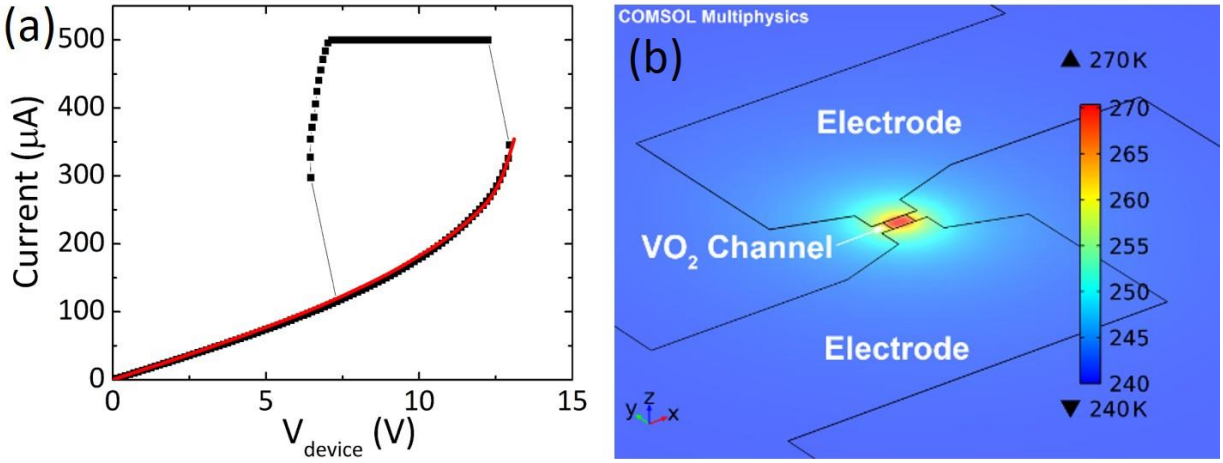

Figure 2.5 (a) Experimental quasi-DC *I-V* characteristic at 240 K stage temperature (black squares) and the simulated one using σ(T) in Figure 2.2. (b) The simulated device temperature profile at V_{TH} at stage temperature of 240 K.

In threshold switches, a delay time (also referred to as incubation time) prior to the actual switching event has been observed in VO_2,[96,106] phase change devices,[128] and dielectric oxides.[88] The

measurement and analysis of the incubation time provides another piece of information to determine whether the threshold switching is thermally induced. Transient voltage and current measurements were performed using a pulse generator and digital oscilloscope with a load resistor (5.5kΩ) in series at stage temperatures from 230 K to 250 K. A series of rectangular source voltage pulses with a 2 ns rise time and increasing amplitude were applied to the devices and the device voltage was recorded as a function of time. At amplitudes below the threshold voltage (note that devices switch at lower voltages for long voltage pulses), the transient showed only a gradual change during the pulse due to uniform current flow and Joule heating (not shown). At a certain value of the pulse amplitude, the device underwent the IMT within the pulse width, its resistance decreased and the voltage across the device dropped abruptly (Figure 2.6a, black squares). The red curve in Figure 2.6a represents the simulated transient response of the device. It reproduces well the initial resistance decrease due to uniform Joule heating and the rapid drop due to IMT. Similar transients were collected as a function of the pulse amplitude and stage temperature and simulated. It is worth noting that the simulation does not have any adjustable parameters and values of the materials parameters were the same as DC *I-V* simulation described before. The incubation times measured at three different stage temperatures as a function of source voltage are shown as squares in Figure 2.6b. At high source voltages, the devices switched to the ON-state within 400 ns. When the source voltage approached V_{TH} observed in quasi-DC voltage sweep (Figure 2.4), the incubation times increased rapidly. Within the entire range of incubation times exceeding six orders of magnitude, the simulated values show good agreement with experimentally measured ones (Figure 2.6b). This is the strongest indication to date that the IMT in VO_2-based devices is induced by Joule heating alone.

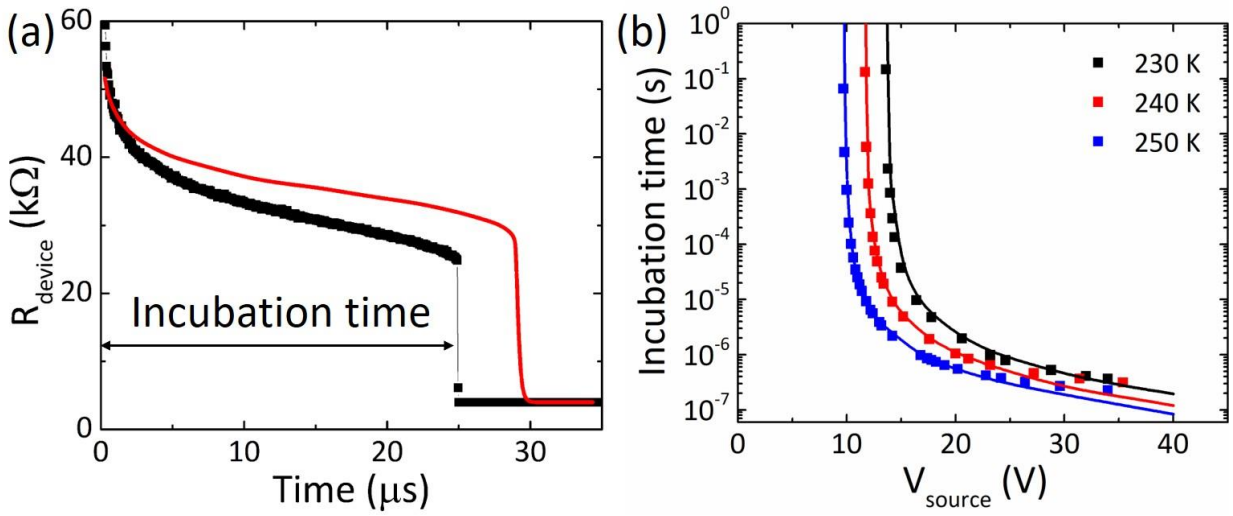

Figure 2.6 (a) The device resistance as a function of time at 240 K stage temperature and source voltage = 13.2 V. Black squares represent experimental points and red line as simulation result. (b) Incubation time observed from experimental measurement (dots) and simulation results (solid lines) as a function of source voltage at various stage temperatures.

The very good agreement between the simulation and experiment poses the question why similar attempts have produced grossly diverging results.[105] One of the explanations could be related to the microstructure of the functional layer. Virtually all data on VO_2-based devices have been obtained on layers deposited by sputtering or oxidation of a metal layer[96,105,129] and are expected to be polycrystalline with small grain sizes. This can result in the formation of nonuniform current flow and reduction of the active volume that needs to be heated. This, in turn, would lower the incubation time before transition. Some experiments indicate that this is indeed the case with the spatial inhomogeneity related to the grain size.[121] The functional layer used in this study is an epitaxial thin film, which is expected to promote uniform current flow and only thermally induced current filamentation in the ON-state discussed below.

Additionally, multiple thermal time constants in the device have been observed in the finite element simulation (Figure 2.7). The system of the small device and the thick substrate heat sink at the bottom to the thermal stage can be thought of as a distributed network of heat resistances and capacitances. At the initiation of the pulse, only a small volume around the device heats up (Figure 2.7b) resulting in a fast time constant. This component of the temperature rise is important at high pulse amplitudes, which leads to the almost linear temperature rise in the device and the device reaching the transition temperature in about a microsecond or less (Figure 2.7d). At long times, the heat spreads in a much larger volume (Figure 2.7c), giving rise to much slower temperature increase with longer time constants (Figure 2.7e). This phenomenon of the temperature rising beyond the primary thermal time constant could have easily led to an underestimation of temperature in earlier works that discussed steady-state (DC and long incubation time) responses.[105] The inclusion of the multiple thermal time constants in this electrothermal model (by including the actual thickness of the substrate) is the key to reach agreement between experimental and simulated incubation time across six orders of magnitude (Figure 2.6b). Figure 2.6b shows the change in incubation time increases more rapidly with reducing voltage for times longer than the primary thermal time constant of 4 μs. Following the fact that the primary thermal time constant has been reached and the device has heated up significantly, the time it takes for the slower time constant to gradually heat up the device results in longer incubation times. In such cases, a lower voltage would dissipate significantly less power and leave the device at a lower temperature at the end of the primary time constant, thus slowing down the incubation process by several orders of magnitude (example: 4 orders of magnitude change in incubation time between 13 V and 15 V at 230 K, in Figure 2.6b).

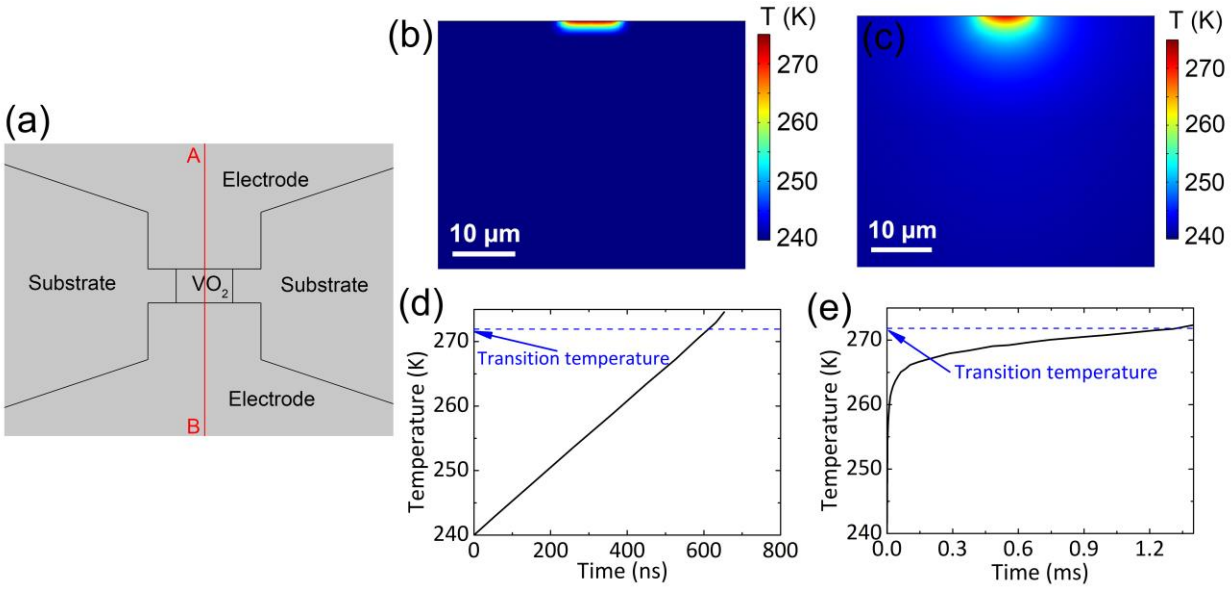

Figure 2.7 (a) The top view of the device structure used in COMSOL simulation. The temperature distribution along the vertical slice through the structure (the A-B line in (a)) at the time that the temperature reaches transition temperature during source voltage of (b) 27.2 V and (c) 12 V. Corresponding simulated maximum temperature rise in the VO_2 channel with time under source voltages of (d) 27.2 V and (e) 12 V.

2.5 Filamentary behavior in the ON-state

The OFF-state behavior of VO_2-based devices has been discussed in the previous section and the simulation results show good agreement with experimental data. In this section, the simulation is extended to the ON-state *I-V* to show the filamentary behavior of conduction.

The experimental *I-V* obtained at the stage temperature of 260 K is compared to simulation results in Figure 2.8. The black squares and red continuous line represent the experimental and simulated

I-V curves, respectively. The parts of both curves between the origin and point A correspond to the OFF-state.

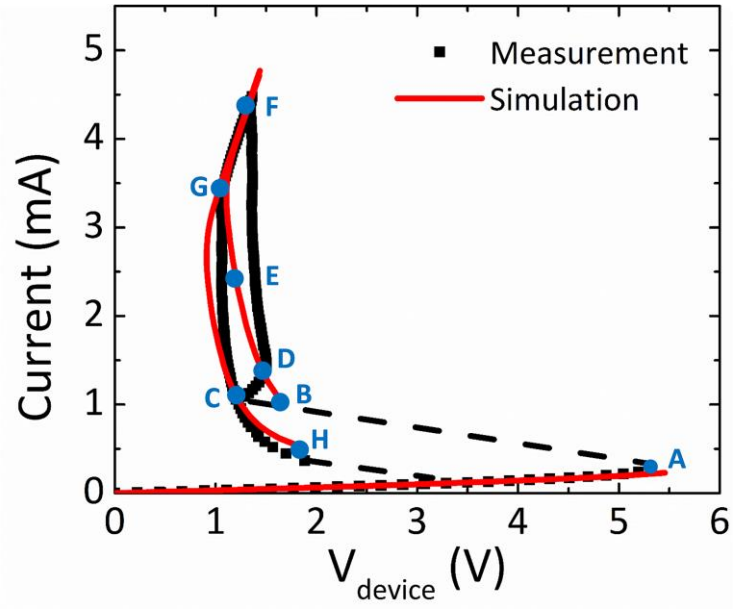

Figure 2.8 Experimental and simulated *I-V* characteristic at 260 K.

With current increasing past the threshold, the device enters into a Negative Differential Resistance (NDR) region and transitions along the load line of the 5.5 kΩ resistor (marked by black dashed line) to the ON-state. The transition occurs in a time too short for the experimental set up to record any data points in this interval of voltage and current. The experimental data starts again at point C with the initially positive *I-V* slope. The simulation results start at point B with the negative value of $\partial I/\partial V$. The difference is likely due to the fact that, in the experiment, the metallic domains created during the transition to the ON-state remain isolated.[130] With further increase of current, the domains grow and, at point D, form a continuous path between the two electrodes. The simulation could not capture this process as I assumed the spatially averaged conductivity measured in the experiment. Further increase of the source voltage results in increasing current

with very little change of device voltage (points D to F in Figure 2.8). At point G, where the slope of the *I-V* changes from negative to positive, the entire VO_2 channel has transitioned to metallic phase. At still higher currents, the characteristics become linear with the VO_2 channel acting as a fixed resistor.

On the downward sweep of the source voltage, the *I-V* evolves along a different path than for the increasing voltage (point F to G and C). The hysteresis in the ON-state is due to growth and shrinkage of the metallic domains within the VO_2 channel.[131] The spatially averaged conductivity corresponding to downward sweep (red dashed line in Figure 2.2b) faithfully reproduced this behavior. Eventually, the path reaches a line that's almost parallel to the *I-V* for increasing voltage. With the decreasing voltage, the device reaches the holding voltage V_{HOLD} at point H, and transitions along the load line back to the OFF-state.

Figure 2.9 plots the current density profile of VO_2-based devices at point B, E and G in the ON-state of *I-V* characteristic. The light blue area within the VO_2 channel corresponds to the conductive filament. The filament is wider in the middle and narrows down closer to either electrode due to electrodes acting as heat sinks. Similar shape of the filament was observed by optical microscopy.[132] At the beginning of the ON-state, point B, the filament width is about 2 μm at the widest point. The evolution of device along the ON-state corresponds to the increase of the filament width as is apparent from examination of Figure 2.9(a)-(c). Since the conductivity of the VO_2 above the transition region is almost constant, the device resistance is decreasing in inverse proportion to the filament width. At point G, the filament fills up the entire oxide layer and the slope of the *I(V)* turns positive corresponding to the characteristics of a fixed resistor.

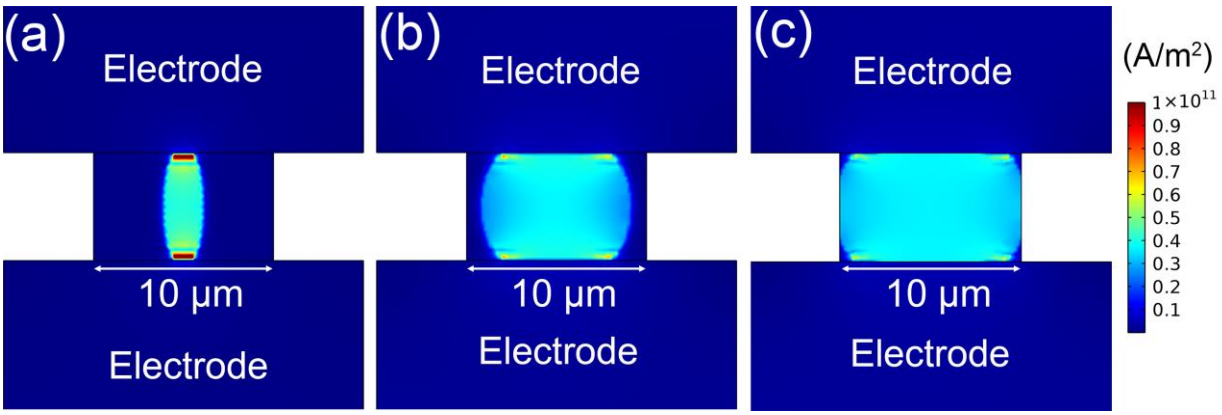

Figure 2.9 The current density profile of the device during ON-state, corresponding to (a) point at the beginning of the ON-state (point B in Figure 2.8), (b) point at the current of 2.4 mA (point E in Figure 2.8) and (c) point at which the slope of *I-V* in the ON-state changes to positive (G in Figure 2.8).

Figure 2.10 illustrates the temperature distribution corresponding to points A, B and G in Figure 2.8. The temperature distribution along the width the VO_2 strip right before the threshold (point A in Figure 2.8) is shown as a black continuous line. The x-axis indicates the position across the 10 μm wide VO_2 channel. The temperature increase ranges from 7 K at the edges of the VO_2 to 12 K in the center. The Joule heat generated in the channel is transported straight down towards the heat sink below the substrate but also laterally resulting in somewhat higher temperature (and conductivity) in the center of the VO_2 channel than at the periphery.

At the lowest point in the ON-state (point B), represented by blue dashed line in Figure 2.10, the temperature exceeds 272 K in a 4 μm wide region in the center of the VO_2 channel. The temperature change between the edge of this region and the center is only 11 K but the

corresponding change of conductivity is about two orders of magnitude. This creates a well-defined conducting filament connecting the two electrodes (Figure 2.9a). Also, it is worth noting that the temperature of the VO_2 outside the filament is lower than at threshold voltage (black curve in Figure 2.10) with a corresponding lower current density. This is due to the lower voltage across the device in the ON-state compared to that at threshold. When the filament fills the entire device, the highest temperature in the VO_2 channel is only about 30 K above the stage temperature (10 K higher than IMT transition region).

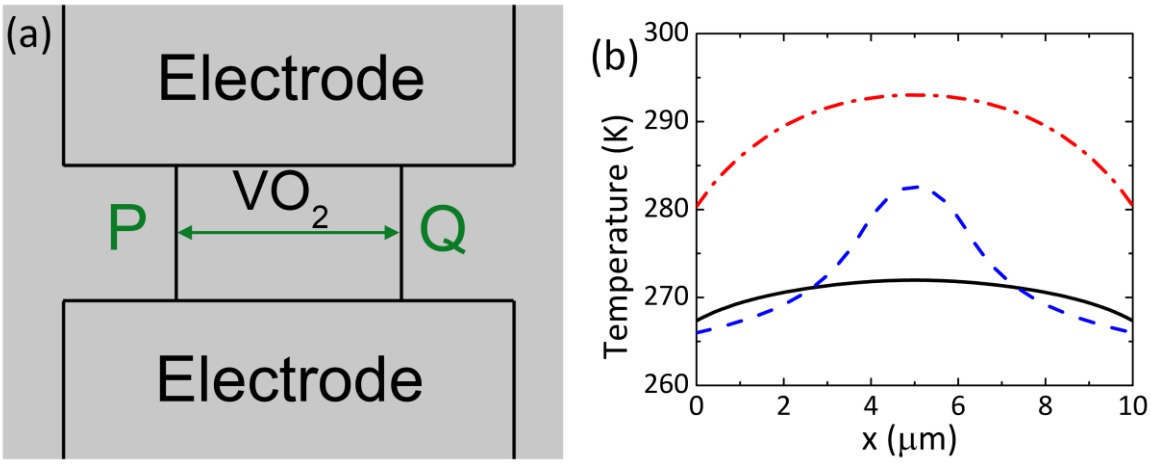

Figure 2.10 (a) The top view of the device structure, with the 6 μm by 10 μm VO_2 channel between two metal electrodes. (b) The temperature distribution along the center of the VO_2 channel (P-Q line with arrows showed in (a)) corresponding to point right before the threshold switching (black line, point A in Figure 2.8), point at the beginning of the ON-state (blue dashed line, point B in Figure 2.8) and the point at the entire VO_2 channel transitioned to metallic phase (red dash-dot line, point G in Figure 2.8), respectively.

2.6 Summary

In this Chapter, I report the results of threshold switching induced by DC and pulse bias applied to the lateral two-terminal VO_2 devices. The mechanism of the switching was investigated through electrothermal finite element simulation. A Joule-heating-based electrothermal model was developed to explain the entire quasi-static *I–V* characteristic, including the OFF-state, the NDR region, and the ON-state of VO_2-based threshold switches. The good agreement between the experimentally measured incubation time and the simulated values at various pulse amplitudes and stage temperatures indicates that the Joule-heating alone can account for the threshold switching without any contribution from carrier injection or electric-field effects. This helps in unifying the DC and short-pulse data using the same thermal formalism and suggests that the discrepancy in the previous works arises partly because a slower time constant (that is greater than the primary thermal time constant ~ 4 μs) associated with substrate heating, leading to an underestimation of temperature in a purely thermal model. Inclusion of a full geometry (that utilizes the actual substrate thickness) in simulation clearly demonstrates an excellent agreement of both transient and steady-state incubation time across 6 orders of magnitude, from 100 ns to 100 ms. The model also describes the formation and evolution of the conductive filament which changes both size and conductivity (temperature) along the ON-state in VO_2-based devices. The temperature of the filament exceeds the IMT temperature only by about 20 K when the entire device is in metallic phase. Since the electrothermal model only uses the device geometry and material properties without any *ad hoc* assumptions, it can be applied to any selector device with thermally induced switching mechanism and can serve as a useful tool to explore both the electric and thermal behavior of threshold switching devices.

3 Scanning probe thermometry of TaO_x-based threshold switching devices

The experimental measurements in this Chapter were completed at National Institute of Standards and Technology with the collaboration of Dr. Andrea Centrone and Dr. Georg Ramer in Nanoscale Imaging and Spectroscopy Group and Dr. Brian Hoskins in Electron Physics Group.

3.1 Introduction

The extreme *I–V* nonlinearity of threshold switches based on VO_2,[69] TaO_x,[133] NbO_2,[134] or chalcogenides[135] makes them the most promising candidates for selectors devices. The mechanism responsible for the rapid increase of the conductivity in these devices, however, is not well understood. Several models have been proposed to explain the switching mechanism, including: electric field induced carrier heating,[84] avalanching,[80] nucleation of a second conducting phase[85] and Joule-heating-induced thermal runaway,[90-93] which is explained in Section 1.4.3. Although these models are based on entirely different physical processes, they all can reproduce the observed *I-V* characteristics and the switching dynamics. Additional experimental observations, for example measurements of the device temperature distribution at different *I-V* points, are needed to discriminate which of the proposed mechanisms is correct. Additionally, knowledge of the device temperature distribution is important since diffusion/chemical reaction rates are typically thermally activated and the failure of selector devices is likely to be a function of the device temperature during switching[136,137] (i.e., the higher the temperature, the faster the device endurance degradation). To date, most of the temperature distributions in selector devices have been derived

from numerical simulations rather than from experiments because in-situ thermometry measurements at the nanoscale are challenging.[138]

Recently, Kumar *et al.* used the thermoreflectance technique to measure *in operando* the temperature of 2 µm × 2.5 µm NbO_2-based threshold switching devices fabricated on a suspended 150 nm-thick silicon nitride membrane with very high thermal resistance.[139] The thin silicon nitride membrane was used to fit the measurement setup, which led to a much higher device temperature than for typical selector devices fabricated on Si wafer under the same bias.[140] Yalon *et al.* used Raman thermometry and SThM to characterize HfO_2, TiO_2 and $Ge_2Se_2Te_5$ planar resistor structures,[141] but neither has shown a threshold switching behavior. Therefore, such measurements cannot provide much information about the temperatures during the switching process.

In this Chapter, the electrothermal model described in Chapter 2 is applied to TaO_x-based threshold switches to reproduce the device *I-V* characteristic. The temperature profile of vertical TiN/TaO_x/TiN threshold switching devices are investigated with nanoscale thermometry using a combination of Scanning Thermal Microscopy (SThM)[142,143] and Scanning Joule Expansion Microscopy (SJEM).[144] The SThM thermocouple probe enables measurement of the top electrode temperature which, in combination with the otherwise qualitative SJEM maps of the thermal expansion, is used to assess the temperature distribution in the device volume with the support of finite element simulations.

The change of functional layer of the devices used in this Chapter is because VO_2 has a low transition temperature (67°C) which limits its application in the real circuits where the local operation temperature is usually above that. While for NbO_2-based devices, Kumar *et al.* has reported the temperature measurement using thermoreflectance technique and the results indicated the Joule heating induced thermal runaway as the mechanism of threshold switching. The TaO_x-based devices exhibit a threshold switching behavior without any phase transition, which is a different material property from both NbO_2 and VO_2, and the switching mechanism has not been well understood. Therefore, it is of interest to experimentally measure the temperature distribution of TaO_x-based devices to provide another piece of information to investigate whether the thermal runaway is the mechanism of the threshold switching behavior.

3.2 Fabrication of TaO_x-based devices

The devices used in this work consist of a 20 nm TiN (bottom electrode)/60 nm TaO_x/20 nm TiN (top electrode)/7 nm HfO_2 (passivation layer) stack, as illustrated by the cross-section schematic in Figure 3.1a. All the device fabrication was completed in CMU nanofabrication facility and the fabrication steps are described here. (1) The 20 nm bottom electrode was first patterned by optical lithography, followed by sputter deposition using TiN target with 150 W RF power at chamber pressure of 3 mTorr in Ar gas atmosphere and lifted off in acetone bath. (2) Second, the 20 nm SiO_2 insulation layer was patterned by optical lithography, followed by sputter deposition from SiO_2 target with 100 W RF power at chamber pressure of 1 mTorr in 5 sccm O_2 and 55 sccm Ar gas atmosphere and lifted off in acetone bath. (3) The third step was to define the active device area (2 μm × 2 μm) using the Elionix e-beam lithography system and a 400 nm thick poly (methyl

methacrylate) (PMMA) resist was used in this step. The PMMA was developed using methyl isobutyl ketone (MIBK) developer after the e-beam exposure to open the 2 μm × 2 μm window of the device area in PMMA layer. (4) Forth, the SiO_2 insulation layer was etched through to expose the active device area with PMMA layer as the soft mask using CHF_3 (22 sccm) and O_2 (3 sccm) gas under 100 W RF power at chamber pressure of 100 mTorr. After this step, the bottom electrode was exposed on the top surface only within the 2 μm × 2 μm active device area, with the other region still covered by the SiO_2 insulation layer. (5) The fifth step was to pattern and deposit the TaO_x functional layer and TiN top electrode layers together without breaking the vacuum in between. The 60 nm thick TaO_x layer was deposited by reactive sputtering using a Ta target under 50 W DC power with 1.8 sccm O_2 and 58.2 sccm Ar gas at chamber pressure of 3 mTorr. The 20 nm TiN top electrode used the same deposition condition as the bottom electrode. (6) The sixth step was to pattern and deposit the 7 nm thick HfO_2 passivation layer on the top surface. The deposition technique was reactive sputtering using Hf target under 50 W DC power with 10 sccm O_2 and 50 sccm Ar gas at chamber pressure of 3 mTorr. (7) The last step was the patterning and deposition of the Au pads for electric testing and wire bonding during scanning probe measurements. The 20 nm Ti/200 nm Au layer was deposited using e-beam evaporation system with a growth rate of 3 Å/s and 5 Å/s, respectively.

This device structure was chosen because it can function under bias for an extended time without incurring permanent changes to the device characteristics and, presumably, structure. The top HfO_2 layer serves to electrically isolate the conductive SThM thermocouple from the top electrode. The device has a smooth top surface (see Figure 3.1b) with root mean square roughness of ≈ 1 nm

(measured by AFM), which is important to limit thermal resistance variations between the tip and the sample surface during scanning.[145]

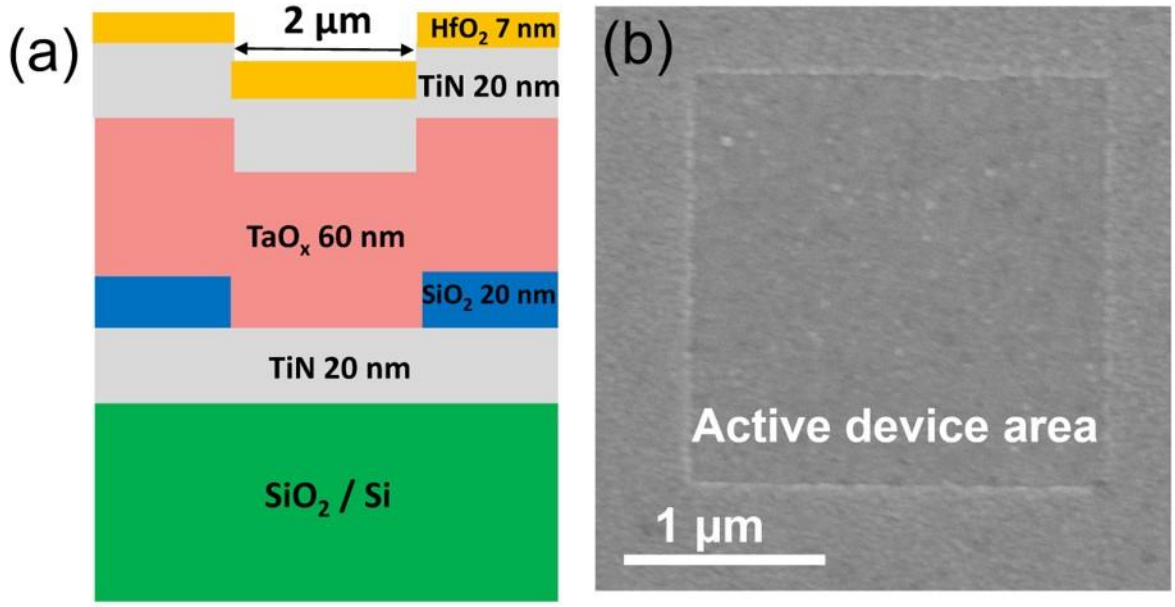

Figure 3.1 (a) Schematic cross-section of the devices used in this work. (Note that the horizontal and vertical scale are different to better highlight the device vertical structure). (b) Scanning Electron Microscopy image (top electrode) of the 2 µm × 2 µm active device area.

Figure 3.2 shows a representative experimental quasi-DC *I-V* characteristic for the TaO_x-based devices (black dots). At low voltages, the device is highly resistive and the current increases linearly with voltage, indicating uniform current conduction in the device. The *I-V* curve shows a super-linear behavior at voltages above 2 V, reaches V_{TH} at 3 V, entering the negative differential resistance (NDR) region. At V_{TH}, if the device is connected to a voltage source and the resistance of the circuit is low, the *I-V* curve would rapidly transition ("snap") along the vertical load line (red dashed line in Figure 3.2) to the value of the current compliance, or upper branch of the device

characteristics. In this experiment, the device was connected to the load resistor (135 kΩ) preventing the snap and allowing for the observation of the entire S-shaped *I-V* curve. Increasing the source voltage further, decreases the device voltage until current reaches ≈ 1 mA, at which point the slope of *I(V)* curve becomes positive again. The NDR region is frequently associated with a nonuniform current flow with the current spontaneously constricting to a narrow thread whose size remains a subject of debate.[146, 147]

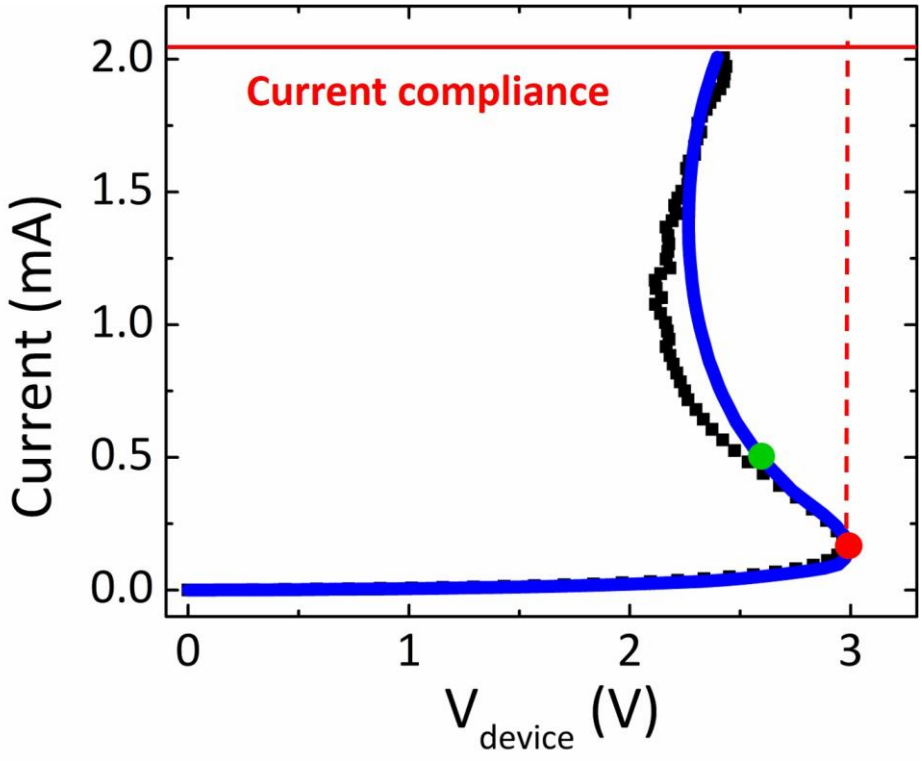

Figure 3.2 Experimentally measured (black dots) and simulated (blue line) threshold switching *I-V* curves of TaO_x-based devices. The red dot corresponding to the current level at 162 µA. The green dot marks the current level at 500 µA. The red dashed line corresponding to the device *I-V* with vertical snap which would occur if the device were connected with a low resistance load.

3.3 Electrothermal simulation of TaO_x-based devices

The electrothermal finite element model was applied to TaO_x-based threshold switches using the Poole-Frenkel (PF) formula to describe the electrical conductivity of TaO_x. The simulation results showed good agreement with measured *I-V* characteristic,[93] which indicated that the threshold switching is due to a thermal runaway mechanism. The Poole-Frenkel formula used here is shown below:

$$\sigma(F,T) = \frac{\sigma_0(T)}{2} + \frac{\sigma_0(T)}{F}\left(\frac{k_B T}{\beta}\right)^2 \left\{1 + \left(\frac{\beta\sqrt{F}}{k_B T} - 1\right)\exp\left(\frac{\beta\sqrt{F}}{k_B T}\right)\right\}, \quad \beta = \left(\frac{q^3}{\pi\varepsilon_0\varepsilon_i}\right)^{\frac{1}{2}} \tag{3.1}$$

$$\sigma_0(T) = q\mu 2\left(\frac{m_e^* k_B T}{2\pi\hbar^2}\right)^{\frac{3}{2}} \exp\left(\frac{E_F(T)}{k_B T}\right) \tag{3.2}$$

where *F* is the electric field, ε_0 is the permittivity of free space, ε_i is the relative dielectric constant of TaO_x, μ is electron mobility in TaO_x (80 cm^2/Vs, fitted by measured low field conductivity), and *q* is the elementary charge, m_e^* is the effective electron mass in TaO_x, $E_F(T)$ is the Fermi energy and k_B is the Boltzmann constant. The Fermi level as a function of temperature was calculated using neutrality equation by fitting the low field electrical conductivity of TaO_x measured up to 500 K, where the calculated Fermi level is 0.32 eV below conduction band at 300 K and dropped to 0.74 eV below at 1000 K. The equation 3.1 was inserted into the electrothermal model as the description of electrical conductivity of TaO_x as a function of temperature and electric field to simulate the device *I-V* characteristic.

Figure 3.3 shows the 2D axisymmetric device structure used in the simulation. It fully reproduced the geometry of fabricated TaO_x-based device with a 2 μm in diameter active device area. The Si substrate is assumed to be 10 μm thick and 20 μm in diameter, which is large enough to mimic the

thermal environment of the real substrate. During the simulation, the bottom surface of the Si substrate was set to stage temperature (298 K) and the material parameters used in the simulation are listed here in Table 3.1. The simulation used the same source voltage amplitude and load resistance value as the experimental measurements. The simulated device *I-V* is shown as the blue line in Figure 3.2 and agrees well with the measured S-shape *I-V* characteristic.

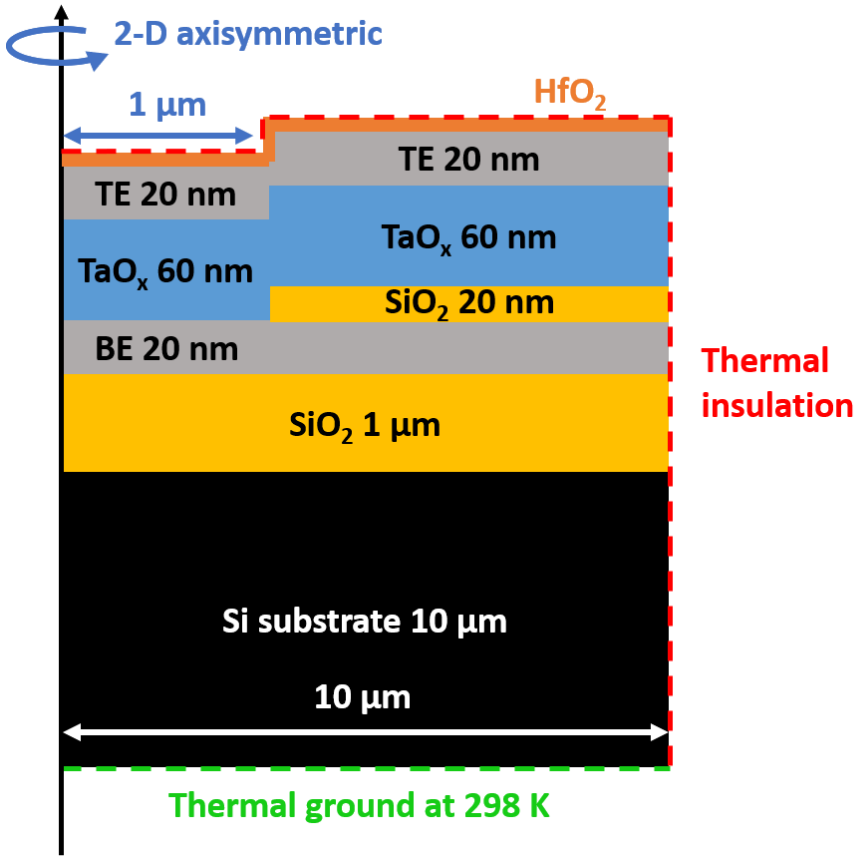

Figure 3.3 The 2D axisymmetric device structure used in the simulation.

Table 3.1 The material properties used in the simulation of TaO_x-based devices.

	Si	SiO_2	TiN[93]	HfO_2	TaO_x[93]	W[148]
Density ($kg \cdot m^{-3}$)	2329	2200	5210	9700	8200	19350
Thermal conductivity ($W \cdot m^{-1} \cdot K^{-1}$)	130	1.4	5	1.1[149]	0.6	$1023 \times T^{-0.312}$
Electrical conductivity ($S \cdot m^{-1}$)	N/A	N/A	4.2×10^5	N/A	User defined	3.5×10^6
Heat capacity ($J \cdot kg^{-1} \cdot K^{-1}$)	700	730	545	120	174	132
Relative permittivity	N/A	N/A	4	25	22	5
Thermal expansion coefficient (1/K)	2.6×10^{-6}	0.5×10^{-6}	1.0×10^{-5} [150]	5.8×10^{-6} [151]	5.0×10^{-6} [152]	N/A
Poisson's Ratio	0.28	0.17	0.25[150]	0.2[151]	0.27[152]	N/A

Figure 3.4 shows the simulated device temperature map at the knee of the *I-V* characteristic (162 μA, red dot in Figure 3.2) and at 500 μA in the NDR region (green dot in Figure 3.2). The color scale represents the temperature increase over ambient temperature (298 K). The device temperature at 162 μA is lower than at 500 μA, with the maximum temperature increase of ≈ 80 K at 162 μA and ≈ 300 K at 500 μA. At 162 μA (at the threshold voltage), the device has an almost uniform current density that reflects the mostly uniform temperature distribution characterized by a full-width-half-maximum of the ΔT profile, FWHM(ΔT) ≈ 1.9 μm. The FWHM(ΔT) is close to the device diameter with the temperature drop at the periphery due to the lateral heat transport which is consistent with typical predictions of the electrothermal model at the knee of the *I-V* characteristics in threshold switching devices.[92,93] As the device current is increased in the simulation, the FWHM(ΔT) decreases slightly to ≈ 1.7 μm at 500 μA.

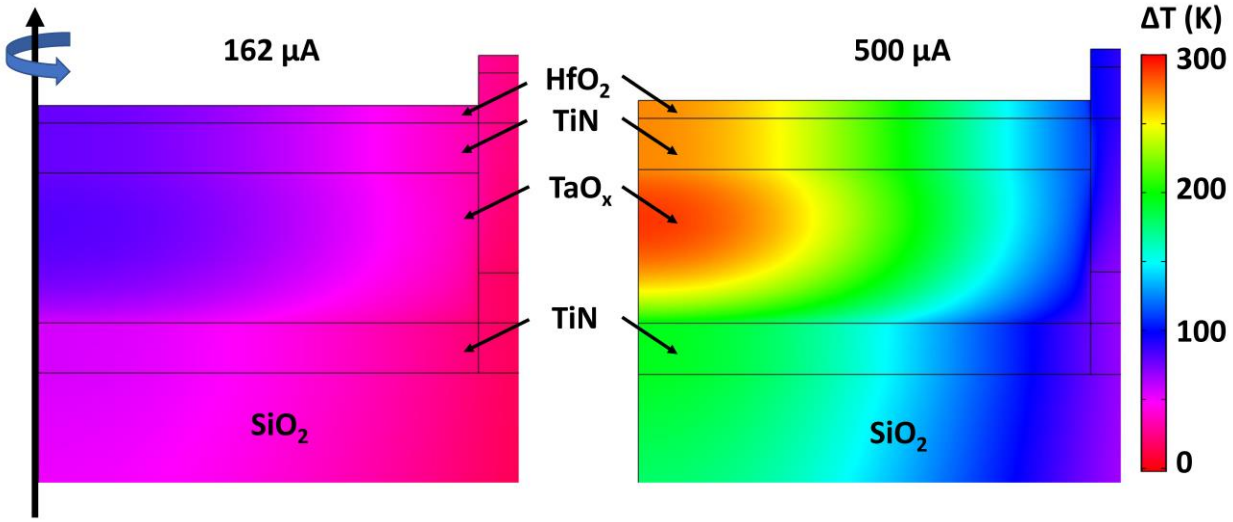

Figure 3.4 Cross-section of the simulated device temperature distributions at 162 µA (left) and 500 µA (right). Note that the horizontal scales in the cross-section plots were shrunk (0.3 : 1) compared to the vertical ones to better highlight temperature variations in the vertical direction. The color scale represents the temperature increase with respect to the ambient temperature at 298 K.

3.4 Scanning probe thermometry measurements setup and calibration

The scanning probe thermometry setups are located in NIST and the measurements were performed with the help from my collaborators, Dr. Georg Ramer, Dr. Andrea Centrone and Dr. Brian Hoskins.

3.4.1 SThM measurement setup and calibration

SThM[142, 153] is a variant of atomic force microscopy (AFM) that leverages a thermal sensor, typically a thermistor or a thermocouple, integrated within the AFM probe to provide topographic

and thermal maps with nanoscale resolution. Most commonly, the SThM probe measures the sample temperature or its thermal conductivity[155]; however, occasionally it has been employed for nanoscale chemical imaging.[154] Here, SThM probes with integrated thermocouple were used to measure the temperature on the surface of TaO_x threshold switching devices under DC bias.

Figure 3.5 shows the SThM measurement setup. The system used is the "VertiSense" SThM module and VTP-200 thermal probe from APPNano, Mt. View, CA, USA. The thermoelectric voltage signal is generated from the thermocouple in the SThM probes and directly transmitted out through a 1000 × amplifier to generate the voltage map. The VTP-200 SThM probes have an integrated thermocouple at the tip. The probes consist of a hollow silicon tip integrated with a vertically oriented thermocouple at the apex which is connected to the sample by a metallic nanowire.[155] The probes were nominally 200 µm long, 50 µm wide and 3.5 µm thick. The cantilever is characterized by a nominal spring constant of 9.9 N/m and resonance frequency of 107 kHz. During the scan (0.5 Hz), the probe was in contact with the sample top surface. The pixel size was 5 nm and 12.5 nm in the x and y directions, respectively. The dwell time per pixel was 2 ms.

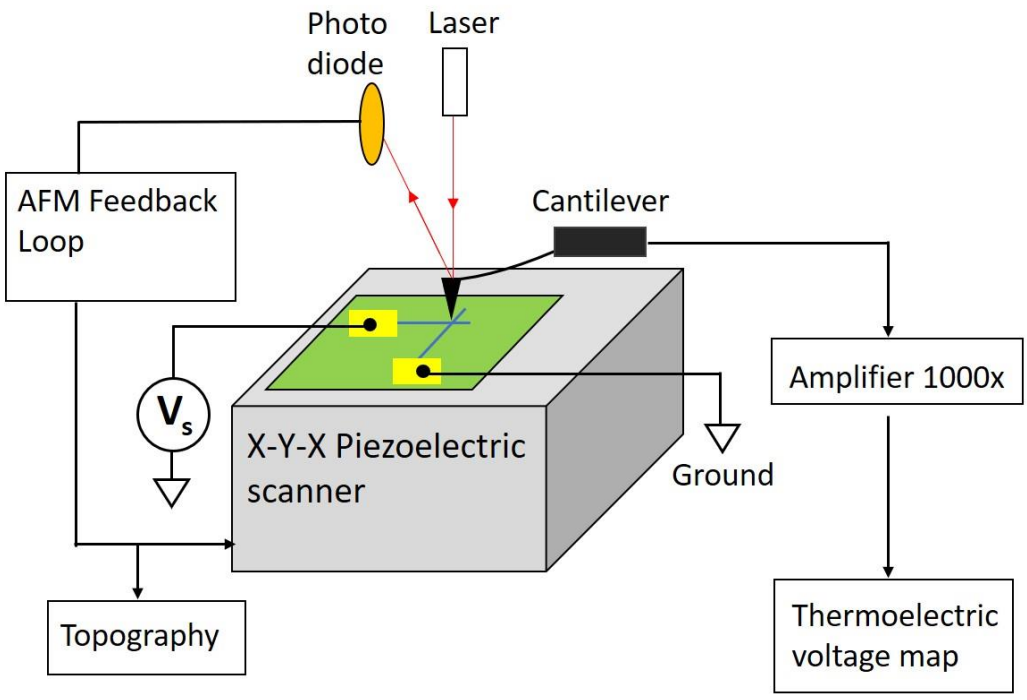

Figure 3.5 Scanning thermal microscopy measurement setup.

The scanning thermal microscopy measurements were performed in air. Because of the typically large tip-sample thermal resistance and because of the contribution to the SThM signal due to heat transfer through air, estimates of the local sample temperature require suitable calibration procedures. In this experiment, I fabricated a calibration chip with a resistive heater structure made of tungsten deposited on the same SiO_2/Si substrate as the TaO_x selector devices. The calibration structure of the heater is shown in Figure 3.6a. The 50 nm thick W layer has a 3 µm × 5 µm constriction located in the middle of the dashed black box. This area is covered by the 7 nm HfO_2 passivation layer to reproduce the exact thermal contact conditions of the TaO_x-based devices. The temperature distribution in the heater structure has been simulated using the electrothermal finite

element model (the material properties are listed in Table 3.1) with the results shown in Figure 3.6b.

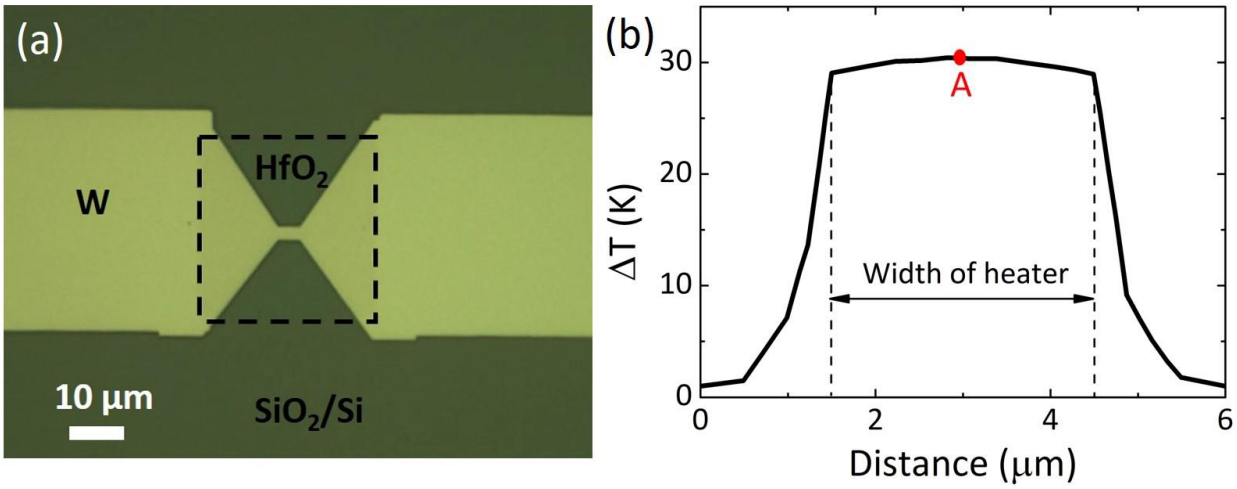

Figure 3.6 (a) The optical image of tungsten heater structure. The heater has a size of 3 µm × 5 µm, located in the middle of the dashed black line. The area within the dashed black line is covered by the HfO_2 passivation layer. (b) Simulated temperature increase profile of the heater structure under DC current at 15 mA.

The heater structure was scanned using the same SThM probe used to measure the TaO_x devices to minimize the contribution of the thermal resistance variation between the probe and the sample. A calibration factor (γ = 22 K/mV ± 2 K/mV) was calculated by comparing the measured signal at the center of the heater (point A in Figure 3.6b) with the corresponding temperature increase obtained from the simulation. The uncertainty of γ represents a single standard deviation of the calibration procedure based on the uncertainty of tungsten's thermal conductivity (assumed to be 10%) and film thickness (assumed to be 5 %) used in the simulations. The uncertainties in the

tungsten material parameters resulted in a calculated temperature uncertainty of ± 3 K. The γ calibration factor was used to estimate the temperature increase of the TaO_x selector devices.

3.4.2 SJEM measurement setup

Figure 3.7 shows the experimental setup of the SJEM measurement. The probes used for the SJEM experiments were contact mode NIR2 probes (Model: PR-EX-nIR2, Anasys Instruments), which had a nominal resonance frequency of 13 kHz ± 4 kHz in air, a spring constant in the range from 0.07 N/m and 0.4 N/m and a contact resonance frequency of ≈ 54 kHz when in contact with the samples. SJEM maps were obtained with 0.2 Hz scan rate resulting in a dwell time of 5 ms/pixel. The pixel size was 5 nm and 12.5 nm in the x and y direction respectively.

80 kHz square voltage wave with 50 % duty cycle and amplitude of source voltage (V_s) was applied to the device during the scan. The applied voltage results in periodic expansion of the entire device structure due to the Joule heating. The AFM cantilever in contact with the sample surface is deflected accordingly and is monitored by the detector. The lock-in amplifier was synchronized to the frequency of the applied voltage. To avoid influence of the tip-sample mechanical contact on the measurement, care was taken to select a voltage modulation with a frequency sufficiently far from the cantilever contact resonance frequency (≈ 54 kHz).

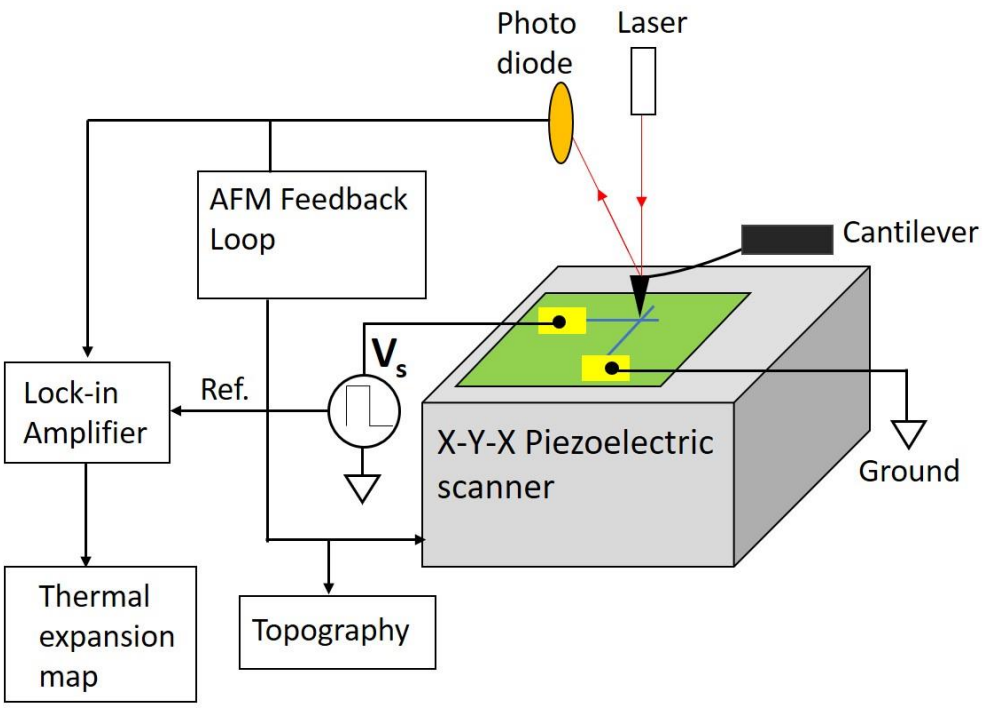

Figure 3.7 Scanning joule expansion microscopy measurement setup.

3.5 SThM and SJEM measurement results

Figure 3.4 shows that the temperature of the top electrode and passivation layers is within 10 % of the temperature increase of the TaO_x functional layer. This is due to the relatively low thermal conductivities of TiN (5 W/m·K) and HfO_2 (1.1 W/m·K) which limit the lateral heat spreading. Such observation suggests that the temperature on the top surface, probed by SThM, well represents the device internal temperature.

For a device current of 162 µA (red dot in Figure 3.2), the SThM temperature map obtained on the top of the passivation layer (Figure 3.8a) shows that the device area heats up almost uniformly.

The temperature increase in the device center is $\Delta T = 79\ K \pm 4\ K$ and $\approx 60\ K$ at the device edge due to the lateral heat transport. The temperature uncertainties throughout this chapter represent a single standard deviation in nominally equivalent temperature measurements obtained within ± 100 nm of the device center due to a combination of measurement noise and point-to-point variation of the tip-sample thermal resistance. Figure 3.8b shows the temperature line profiles for several values of current. The maximum temperature is always in the center of the device and its measured values match well with the simulation results. The ΔT increases with the applied bias from 64 K ± 4 K at 125 µA to 113 K ± 6 K at 200 µA. However, as shown in Figure 3.8b, the experiments show flatter temperature profiles than the simulations. This discrepancy is attributed to the heat transfer contribution from the hot sample to the SThM tip through air, rather than by direct conduction through the tip, an effect that commonly reduces the SThM spatial resolution in air.[153, 156]

The measurements shown here are qualitatively similar but quantitatively different ($\Delta T \approx 80\ K$) than that reported by Goodwill *et al.* for a 5 µm × 5 µm TaO_x device,[93] which predicted $\Delta T = 50\ K$ at the threshold voltage due to the lower resistivity and lower activation energy of conductivity of my TaO_x layer (0.48V ± 0.05 eV) with respect to the one of Goodwill *et al.* (0.70 V). The activation energy was extracted from the slope of the linear fit of the low field TaO_x electrical conductivity as a function of the T^{-1}, from ambient temperature up to 500 K.[93] The uncertainty of activation energy represents a single standard deviation, determined mainly by the fitting procedure. The lower activation energy in these devices corresponds to a less steep increase of the conductivity with temperature, which, in turn, requires a higher temperature to trigger the thermal

runaway. Therefore, the results described in this Chapter are in good agreement with the findings of Goodwill *et al*.[93]

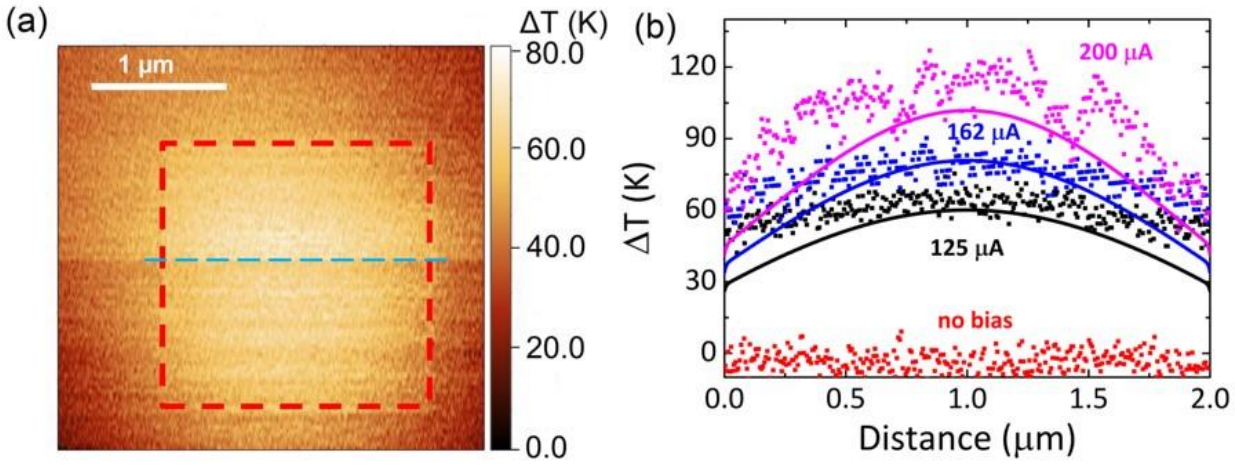

Figure 3.8 (a) SThM temperature map of a TaO_x switching device under bias at 162 µA. The red dashed box highlights the device active area. The blue dashed line marks the position of the measured temperature profiles. (b) Measured (dots) and simulated (lines) temperature line profiles across the TaO_x device at different current levels.

To capture the device temperature profiles with better spatial resolution I resorted to SJEM, which can achieve sub-50 nm resolution in air. In SJEM,[144, 157] a passive AFM probe mechanically transduces the sample thermal expansion resulting from the Joule heating that accompanies the application of short electrical pulses to the device. In general, the SJEM signal is proportional to the sample expansion but does not give an absolute measurement of the expansion. In this work, SJEM measurements were performed by applying a square voltage wave with 50% duty cycle. In response to each voltage pulse, the device thermally expands deflecting the AFM cantilever whose

motion is monitored by the AFM detector (deflection signal). A lock-in amplifier synchronized with the square wave was used to demodulate the AFM deflection signal amplitude. An 80 kHz modulation frequency was used corresponding to 6.25 μs long voltage pulses that exceed the device thermal time constant (≈ 2 μs) to ensure that a steady-state temperature distribution was reached during each pulse. The modulation frequency (80 kHz) was also chosen to be well above the cantilever contact resonance frequency (≈ 54 kHz) to minimize the effect of the local sample-tip mechanical coupling on the signal intensity. The amplitude of thermal expansion measured on the top surface is related to temperature increase of the entire device structure through the following equation[158]:

$$\Delta L = \sum_i \frac{1+\upsilon_i}{1-\upsilon_i} \int_{z_i^0}^{z_i^t} \alpha_i (T(z) - T_0) dz \tag{3.3}$$

with α_i the coefficient of linear expansion, υ_i the Poisson's ratio, z_i^0 and z_i^t refers to the bottom and top surface of each layer, respectively, $T(z)$ the steady state temperature at each position and T_0 the stage temperature (298 K). The thermal expansion of the device structure was calculated using equation (3.3) with the bottom of the sample thermally grounded and fixed in position. The sample was free to expand in the vertical direction. The simulation used the same frequency and amplitude of the applied bias during SJEM measurement.

The SJEM map of a TaO_x device obtained at 22 μA (Figure 3.9a) resembles the SThM map in Figure 3.8a and shows a circular area with a strong signal (i.e. high temperature and high expansion) in the device center. Notably, the region outside the device active area shows nearly zero signal indicating that SJEM can achieve in air a higher spatial resolution than SThM, thus avoiding the challenges due the heat transfer through air. The simulated thermal expansion line

profiles (black lines) and the experimental SJEM line profiles (blue dots) show good correlation, see Figure 3.9b. The vertical scales in Figure 3.9b were set to match the values obtained from the simulation and the experiment at the center of the device at 22 μA.

The SJEM signal shown in Figure 3.9b is proportional to the thermal expansion of the entire device structure, Figure 3.9c shows the simulated contribution for each of the layers. The thermal expansion magnitude from any layer, the TaO_x for example, is given by the difference between two bounding lines representing the interfaces of the layer (blue and magenta lines for TaO_x). The major part of the expansion signal is attributed to the active layers of the device structure rather than the substrate, with the greatest contributions from TaO_x and top electrode layers, due to their higher ΔT. Although the ΔT of the SiO_2 substrate was much lower than for the TaO_x and top electrode layers, the SiO_2 layer contributed a non-negligible thermal expansion due to its large thickness (1 μm) in comparison with the active layers. The good agreement between simulation, SThM and SJEM data is a strong evidence in support of the thermal runaway model for threshold switching in TaO_x devices.[93]

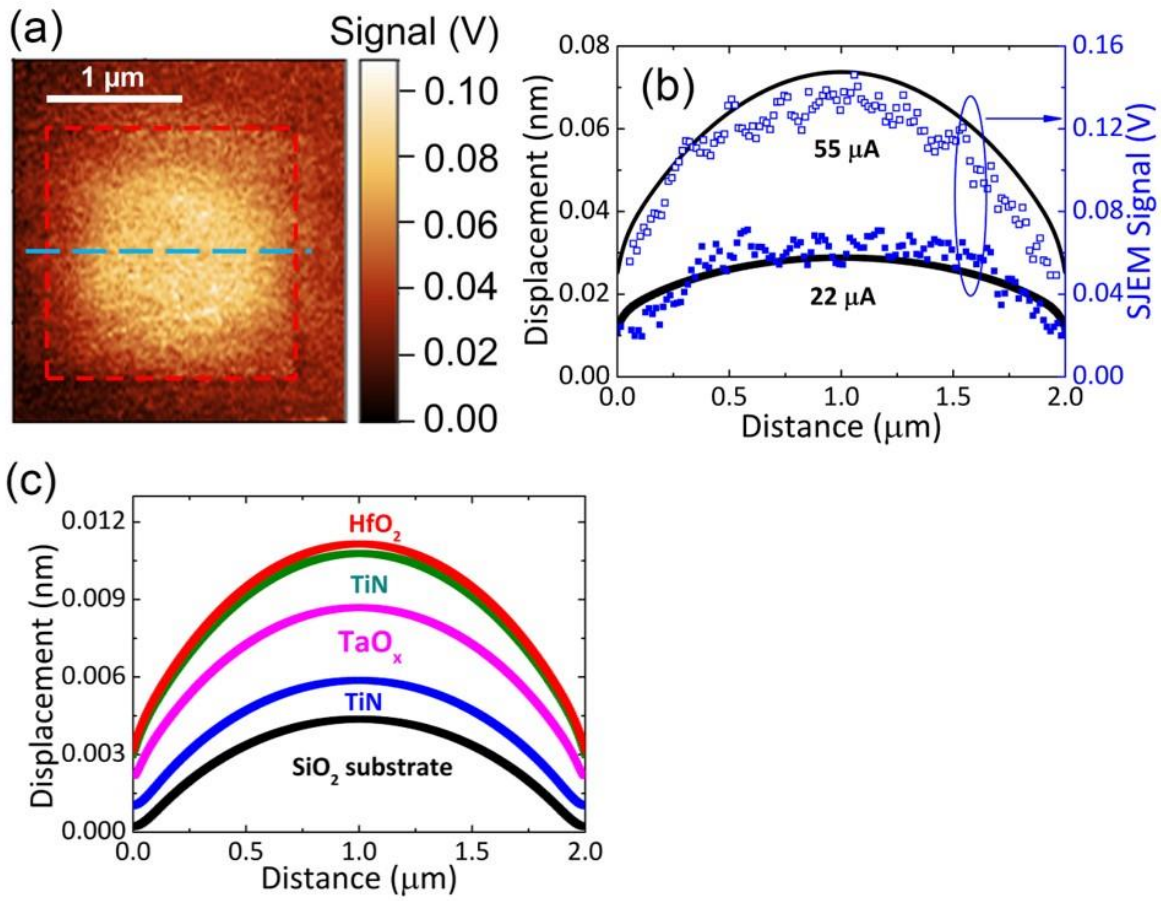

Figure 3.9 (a) SJEM mapping of the active device area at current of 22 μA. The red dashed box highlights the device active area. The blue dashed line marks the position of the measured SJEM profiles. (b) The simulated thermal expansion line profiles on the device top surface (black lines) are compared to the SJEM data (blue dots) obtained at 22 μA and 55 μA. (c) Simulated thermal expansion on top of each layer at 22 μA. The difference between two lines in the plot is the expansion value of the layer that is higher in the device stack (see Figure 3.1a for reference).

One of the competing switching mechanisms, the nucleation model, predicts the formation of a small elongated inclusion (< 1 nm diameter) of a conducting phase.[85] However, such a small

filament would create a much narrower ΔT profile on the device top surface, compared to the temperature profiles measured in this work.[159] The temperature line profile of the TaO_x-based devices assuming nucleation model as the switching mechanism was predicted using the electrothermal simulation. Figure 3.10a shows the device structure used in the simulation including a nucleus of the conducting phase within the oxide layer. The nucleus is a region with electrical conductivity of pure Ta and has a radius of 1 nm, predicted by Sharma *et al.*[88] The length of the nucleus was assumed to be 20 nm at the beginning[85] and could grow vertically with increasing dissipated power until it fully connects the two electrodes (60 nm). The black line in Figure 3.10b shows the temperature line profile on the top surface a 20 nm long nucleus in the middle of the oxide layer, and the dissipated power is 480 μW, the same power as the TaO_x device at threshold switching point shown in Figure 3.2. Although the temperature distribution is very similar to the profile shown in blue line in Figure 3.8b, which is due to the fact that the nucleus is still small and located in the middle of the oxide not connecting the two electrodes. Therefore, the current conduction from top electrode to bottom electrode is not constricted to only the nucleus region. However, the electrical properties of the TaO_x device shows a significant difference from the experimental measured *I-V* characteristic (Figure 3.2). The predicted device voltage is only 0.73 V and the device current is at 660 μA based on the nucleation model compared to 3 V and 162 μA from the measured *I-V*, which is clearly a large disagreement from the experimental data that cannot be explained by the uncertainty coming from the electrothermal model. If the nucleus grows vertically in size with increasing dissipated power and connects the two electrodes formed a filament, the current conduction is then limited to the filament region and the temperature profile on the top surface shows a small hot region as shown in the blue line in Figure 3.10b. In this case, the highest temperature increase is about 300 K in the filament region with the FWHM value of

only 300 nm in diameter, a much small and high temperature spot than the measured data from SThM (Figure 3.8b). Therefore, the scanning probe thermometry results showed here disagree with the prediction based on the nucleation model in both the device *I-V* characteristic and the temperature distribution on the top surface.

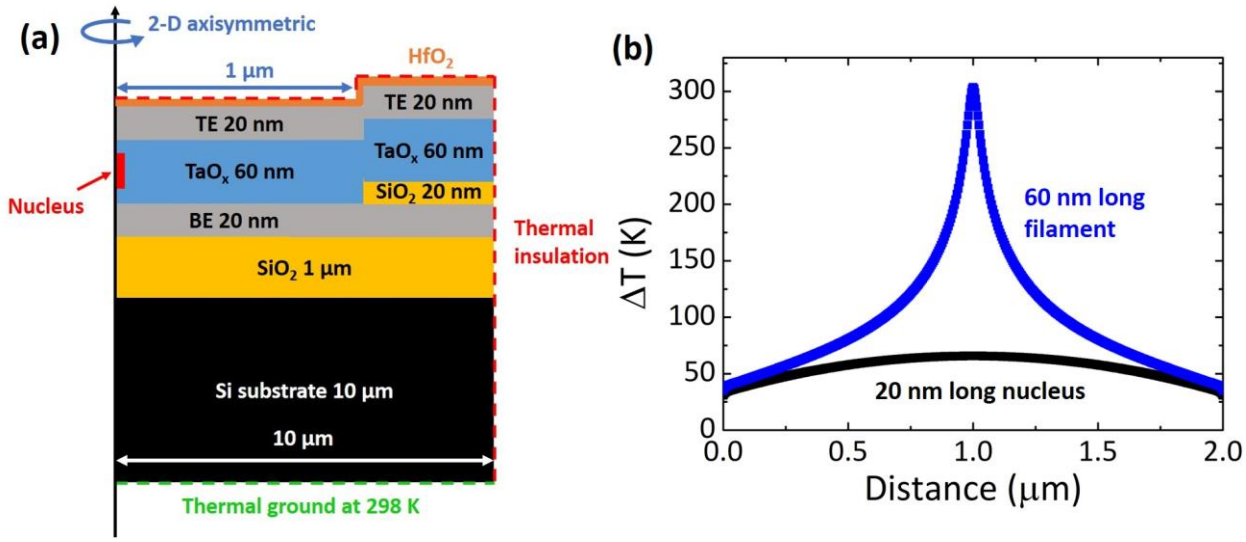

Figure 3.10 (a) The device structure used in the electrothermal simulation with a nucleation of conducting phase within the oxide layer. (b) The temperature distribution on the top surface of the device when the nucleus is 20 nm long (black line) and 60 nm long (blue line).

Below 200 µA, the devices used in this study were stable (exhibited no permanent changes) for more than 10 min, which is sufficient to complete the SThM or SJEM measurements. At higher currents and dissipated power, a permanent filament formed in the devices which was accompanied by changes of the top electrode topography after a much shorter time (about 2 min at 350 µA) thus preventing *in operando* measurements deeper in the NDR region. Further studies

on the failure mechanism of these devices are needed in order to improve the device reliability and map the device temperature distribution in the ON-state.

3.6 Discussion

Based on the results showed in Chapter 2 and Chapter 3, both the electrothermal simulation and experimental measurement results support that the VO_2 and TaO_x-based threshold switches can be interpreted by the thermal-induced switching mechanism. The most relevant material to those two metal oxides is NbO_2 which undergoes an insulator-to-metal transition at 1080 K.[160] The *I-V* characteristics of NbO_2 devices exhibit the NDR region and switch between OFF- and ON-states as well. The early reports associated the threshold switching in this material with the IMT.[161, 162] Three recent papers,[90-92] however, reported the temperature at the threshold voltage in NbO_2 to be much lower than the IMT temperature. Accordingly, it is not clear if the layers exhibited the IMT. The switching was interpreted as the result of thermal runaway due to positive feedback between temperature and conductivity increases in the material with strong dependence of conductivity on temperature as I described in Section 3.3. It should be pointed out that while from the electrical conductivity point of view the ON-state in TaO_x-, NbO_x-, and VO_2-based devices is essentially identical (conductivity increasing with temperature), from structural point of view, VO_2 is different. The structure of the material remains the same in the OFF- and ON-states in TaO_x and NbO_x but changes from insulating monoclinic to conducting rutile in VO_2. This structural change has clear consequences as, such as, the hysteresis in the switching characteristics.

While the operating mechanism in all of the above mentioned devices is the same, their quantitative

characteristics are quite different depending on the temperature dependence of the conductivity ($\sigma(T)$). In devices with the resistance dominated by the thermally activated conductivity of the functional layer, this temperature increase in the device due to Joule heating is related to the activation energy: the higher the activation energy, the larger $\partial\sigma/\partial T$ and the smaller the temperature rise that will result in the runaway. It is also worth noting that the runaway in TaO_x or NbO_x can occur at very different temperatures in the same device depending on the stage temperature. As interpreted by Goodwill *et al*,[93] the runaway occurs when self-heating produces a reduction in the resistance by a factor of two, rather than at a specific conductivity or temperature value. In devices with the IMT-type functional layer at stage temperatures not much below the IMT, the temperature corresponding to halving the initial resistance is likely to fall within the transition range, which is the case of VO_2-based devices. The runaway in such case occurs at almost constant temperature independent of stage temperature.

In previous reports, the device temperature at the beginning of the ON-state was simulated to reach 880 K (~500 K increase from the temperature at threshold switching point) in the TaO_x devices[93] and about 550 K (~250 K increase from the temperature at threshold) in NbO_x devices (with the stage temperature of 300 K).[92] This is more than two orders of magnitude higher than the corresponding temperature rise in the VO_2-based devices. As the blue dashed line shown in Figure 2.10b indicates, the highest temperature obtained in simulation of the VO_2 was only 20 K above the stage temperature and less than 10 K above the temperature at threshold. The different temperature increase from threshold to the beginning of the ON-state in these two types of devices is due to the different $\partial\sigma/\partial T$ at the temperature of threshold switching point. For VO_2, the conductivity increases about 2 orders of magnitude over the temperature range of 10 K at threshold

switching, for TaO_x on the other hand, the temperature needs to change by 400 K for the same two orders of magnitude change in conductivity. Clearly, the larger $\partial\sigma/\partial T$ results in a smaller temperature increase at threshold switching.

The behavior of the filament in these types of devices with increasing current in the ON-state is also different. In VO_2, the temperature of the filament stays almost constant while the lateral size of the filament is increasing. In TaO_x, the filament size (defined as full width at half maximum of current density distribution) increases very slowly while the temperature at the center increases quite rapidly. These differences are also the consequence of different dependence of conductivity $\sigma(V,T)$ on temperature. The value of current at a given voltage in a device with temperature dependent conductivity can be represented by a sum of a series. The first two terms can be written as follows:

$$I(V,T) = V\sigma(V,T_o) + V\frac{\partial\sigma}{\partial T}\Delta T + \cdots$$

$$= V\sigma(V,T_o) + V\sigma(V,T_o)\left[V^2 R_{TH}\frac{\partial\sigma}{\partial T}\Big|_{T=T_o}\right] + \cdots \quad (3.4)$$

This expression assumes a constant thermal resistance of the device (R_{TH}), and T_o denotes the stage temperature. The common factor in the series corresponding to the gain of the feedback loop is shown in the square bracket. The series diverges and the device goes into runaway whenever the value of the gain exceeds unity, which happens at V_{TH}. The gain, however, is a function of temperature. With increasing temperature of the device, the $\partial\sigma/\partial T$ in VO_2 decreases rapidly to zero and changes sign as the material becomes metallic. In parallel, the gain drops and the runaway stops at temperatures not much above the IMT. In TaO_x and NbO_2, the $\partial\sigma/\partial T$ is high and positive and conductivity saturates only at very high temperatures at which chemical reactions or melting

can take place. As a consequence, such devices are likely to be destroyed by the runaway. Only limiting the current by using the appropriate load can allow for observation of the ON-state in DC or pulse modes of operation.[93,163]

3.7 Summary

In conclusion, the TiN/TaO_x/TiN vertical selector devices exhibited S-type *I*-*V* characteristics. The electrothermal model developed in Chapter 2 was applied to TaO_x-based devices with the Poole-Frenkel formula as the description of electrical conductivity and it successfully reproduced the measured S-shape *I*-*V* characteristic. These devices were then measured directly and with nanoscale resolution of the temperature distribution up to the switching point using the combination of SThM and SJEM techniques. The measurements revealed that, at the threshold voltage, the device temperature increases only by about 80 K. The experimental temperature distribution and device *I*-*V* agree well with the electrothermal simulation results. The measurements strongly support that the Joule-heating-induced thermal runaway is the mechanism underlying the threshold switching behavior in TaO_x-based devices. In addition, the results given in this Chapter generally highlight the nanoscale thermometry capabilities of SThM and SJEM techniques for characterizing threshold switching device structures. Finally, NbO_2-based threshold switching devices were discussed and according to previous reports, the switching mechanism of NbO_2-based devices is due to the thermal runaway as well. Therefore, the switching mechanism of VO_2, TaO_x and NbO_2-based devices can be unified to the same Joule heating-induced thermal runaway model and the electrothermal model developed in Chapter 2 is capable of reproducing the device behavior.

4 Scaling behavior of thermal-induced threshold switching devices

4.1 Introduction

In the past few years, several circuit level simulations concerning the requirements for the selector in crossbar arrays have been reported.[44,164-168] In general, to achieve a large array size, the selector needs to have low leakage current at READ voltages, high ON current to allow for switching the memory element, and a threshold voltage compatible with the SET, RESET and READ operations of the memory element. The exact requirements for selectors depend on the parameters of the memory element with which they are connected. In any case, a low leakage current (< 100 pA) and the ability to drive high ON current (> 50 μA) are universally desired.

Most of the studies cited above focused on micron size devices and very few studies explored the scaling behavior at diameters below a micron.[71,169] The most comprehensive work was that of Cha *et al*. who investigated devices between 200 and 30 nm diameters using amorphous NbO_x as a functional layer.[71] The devices used in that study required to be electroformed before they could exhibit stable threshold switching characteristics. According to the authors, electroforming led to local changes in composition and crystallinity which depend on the forming process, neither of which is known. As such, the study could not address the scaling limits of threshold switches.

In this chapter, I report the results using the electrothermal model discussed in Chapter 2 to simulate the threshold switching characteristic as a function of device lateral size and oxide layer

thickness using three different functional layers sharing the same operating mechanism (TaO_x, VO_2 and NbO_2). The device characteristics, such as threshold voltage, leakage current, and maximum temperature in the ON-state at 50 μA were extracted and compared between devices with different dimensions and different materials. The benchmark of 1S1R cell using scaled devices with a set of parameters of a generic memory element was also evaluated.

4.2 Device structure and computation setup

The devices in a crossbar array have square shape cells determined by the intersections of word and bit lines with certain thickness, width and pitch.[170] The electrodes and oxide are typically deposited on a 500 μm thick oxidized Si substrate. In the simulation I use a simplified structure shown in Figure 4.1. The axisymmetric 2D geometry consists of a vertical metal/oxide/metal sandwich deposited on 1 μm thick SiO_2 layer and 5 μm thick silicon substrate. The sandwich is surrounded by SiO_2 on all sides. The 5 μm thick silicon in the model greatly shortens the model conversion and was verified to effectively mimic the heat sink of the 500 μm thick substrate, producing an almost identical temperature distribution. The heat sinking is also dependent on the lateral size of the entire structure. The 5 μm radius was chosen based on simulation results showed this size is appropriate to provide adequate heat sink. The lateral size of the actual device structure ranged from 10 nm to 200 nm in diameter. In the following, the device with, for example, 10 nm diameter will be referred to as 10 nm device. In the sandwich structure, the bottom electrode (BE) is 40 nm thick, and top electrode (TE) is 30 nm thick. Both BE and TE are Au for VO_2 selectors, and TiN for TaO_x and NbO_2 devices. These metals are known to form ohmic contact at the metal/insulator interface.[171] The oxide layer thickness is always larger than 10 nm in all

simulations. Below this value, other conductivity mechanisms than the ones described below can dominate the overall current conduction. During the simulation, the temperature of the bottom surface is set to 300 K (unless specifically noted otherwise) while the top and side surfaces of the structure are thermally insulated. Electrically, the bottom surface of BE is at electrical ground, and the top surface of TE is connected to an outside circuit with a load resistor and voltage source. The load resistance is 400 kΩ corresponding to the High Resistance State (HRS) of the assumed memory element.[44] In the simulation, a source voltage was increased linearly with time over 1 s, followed by an identical linear decrease. The amplitude of the sweep was adjusted to drive the current to 50 µA.

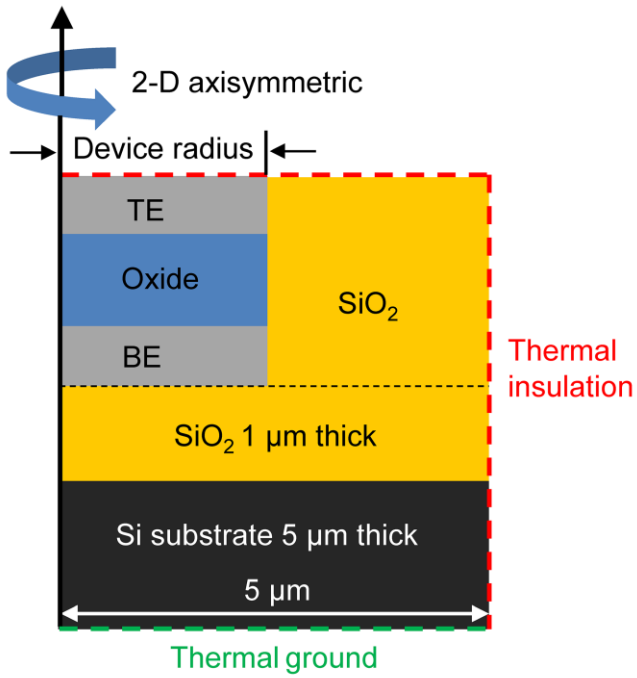

Figure 4.1 Schematic diagram of a selector structure used in the simulations (note: drawing is not to scale). TE and BE corresponding to top electrode and bottom electrode, respectively.

Figure 4.2 shows the electrical conductivity used in the simulation of the three oxides as a function of temperature. Both VO_2 and NbO_2 undergo IMT at their transition temperatures, 340 K for VO_2 and 1080 K for NbO_2, with the metallic state having an almost constant electrical conductivity. There is no IMT in TaO_x and the conductivity increases exponentially with temperature in the entire temperature range. The electrical conductivity of VO_2 as a function of temperature was adopted from a report by Radu *et al.*[106] The thermal conductivity of VO_2 changed across the IMT with $k_{insulator}$=3.5 $Wm^{-1}K^{-1}$ and k_{metal}= 6 $Wm^{-1}K^{-1}$.[125] The VO_2 switches cannot operate if the sink temperature is above the transition temperature essentially eliminating VO_2 from practical applications. It is, however, possible that doping could increase the transition temperature and it was interesting to see the trends in scaling characteristics for a material with low transition temperature.

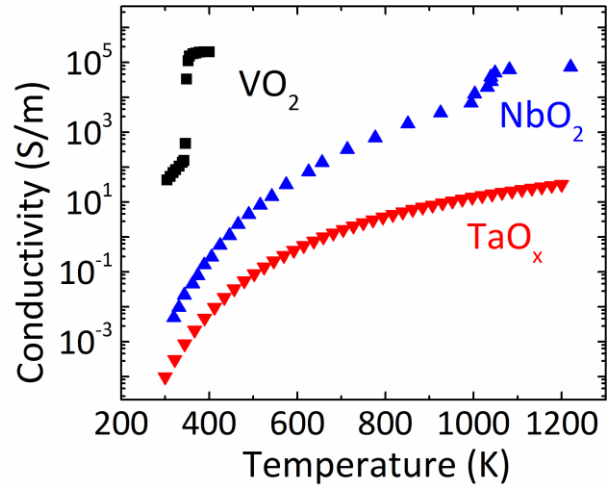

Figure 4.2 Low field electrical conductivity of VO_2, NbO_2, and TaO_x as a function of temperature used in this simulation.

The electrical conductivity used for niobium oxide-based devices is that of crystalline NbO_2. In

the insulating phase, the conductivity follows Poole-Frenkel formula used by Funck *et al.*[92]:

$$\sigma = \sigma_0 exp\left(-\frac{\Delta W_A - \beta\sqrt{E}}{k_B T}\right), \ \beta = \left(\frac{q^3}{\pi\varepsilon_0\varepsilon_i}\right)^{\frac{1}{2}} \quad (4.1)$$

where the pre-factor σ_0 = 9.99 × 10^6 S/m, carrier activation energy ΔW_A = 0.67 eV, k_B is the Boltzmann constant, q is the electron charge, ε_0 is the permittivity of free space, ε_i is the relative dielectric constant of NbO_2 (9.5), E is the electric field (device voltage/oxide thickness), and T is the temperature. The electrical conductivity of metallic phase NbO_2 is assumed to have a constant value of 8 × 10^4 S/m.[172] The thermal conductivities of NbO_2 $k_{insulator}$ = 0.12 $Wm^{-1}K^{-1}$ and k_{metal} = 2.0 $Wm^{-1}K^{-1}$ were adopted from Nandi *et al.*[173]

The electrical conductivity of TaO_x was adopted from Goodwill *et al.*'s work:[93]

$$\sigma_{PF}(E,T) = \frac{\sigma_0(T)}{E}\left(\frac{k_B T}{\beta}\right)^2 \left\{1 + \left(\frac{\beta\sqrt{E}}{k_B T} - 1\right)\exp\left(\frac{\beta\sqrt{E}}{k_B T}\right)\right\} + \frac{\sigma_0(T)}{2} \quad (4.2)$$

where

$$\sigma_0(T) = q\mu N_c\left(\frac{N_d}{N_t}\right)^2 exp\left(-\frac{E_d + E_t}{2k_B T}\right) \qquad \beta = \left(\frac{q^3}{\pi\varepsilon_0\varepsilon_i}\right)^{\frac{1}{2}} \quad (4.3)$$

N_c is the effective density of states in the conduction band, N_d, E_d, N_t and E_t correspond to the densities and ionization energies of donors and traps, respectively, $\sigma_0(T)$ is the low field conductivity, and μ is the electron mobility. The equation (4.2) includes the electron emission in 3D which makes it a little different from equation (4.1) used for NbO_2 and both of the two equations have been reported to successfully reproduce the experimental *I-V* characteristic of NbO_2-[92] and TaO_x-based[93] threshold switching devices. The range of activation energies in (4.3) varies widely with the oxygen content of TaO_x films. Typically, the energies are low (<0.3 eV) for oxygen deficient films and can exceed 1 eV for fully oxidized ones. Accordingly, the

conductivities vary by many orders of magnitude. Here in this study, I used the value of the activation energy that represents a compromise between low leakage current and the high temperature of the functional layer in the ON-state. The values of activation energy and pre-exponential factor used in this simulation were 0.44 eV and 2240 S/m and corresponded to values found experimentally in film with highest oxygen content reported in Goodwill *et al.*'s work.[93] The other material parameters used in the simulation are listed below in Table 4.1.

Table 4.1 The material properties used in the simulation of device scaling behavior.

Material	Density ($kg \cdot m^{-3}$)	Thermal conductivity ($W \cdot m^{-1} \cdot K^{-1}$)	Electrical conductivity ($S \cdot m^{-1}$)	Heat capacity ($J \cdot kg^{-1} \cdot K^{-1}$)	Relative permittivity
Si	2329	130	N/A	700	N/A
SiO_2	2200	1.4	N/A	730	N/A
Au	19300	317	4.56×10^7	129	6.9
TiN[93]	5210	5	4×10^5	545	4
VO_2	4340	Insulating phase: 3.5 Metallic phase: 6.0[125]	User defined	690	36[126]
TaO_x[93]	8200	0.6	User defined	174	22
NbO_2[92]	5800	Insulating phase: 0.12 Metallic phase: 2.0[173]	User defined	459.2	9.5

4.3 Scaling trends of *I-V* characteristic

The simulated *I-V* characteristics of the three types of devices as a function of device diameter are shown in Figure 4.3. All devices discussed in this section had a 10 nm thick oxide layer which was selected to reduce the value of the threshold voltage. The leakage current is defined as the current value when the device is under bias at half of the threshold voltage. TaO_x devices do not show the snapback along load line in the *I-V* because the load line corresponding to the 400 kΩ of memory element HRS has a lower slope than the intrinsic selector characteristics. One should also note that

the ON-state voltage is similar to the threshold voltage (85% for 10 nm diameter device). Using the 10 nm selector *I-V* as an example, at the point where the device current reaches about 40 μA, the filament fills the entire device and the slope of *I(V)* becomes positive. As a consequence, in order for the selector to source 50 μA, the device voltage would have to be larger than threshold voltage for small device sizes (< 10 nm diameter). The VO_2 and NbO_2 devices have similar *I-V* characteristics (plotted in Figure 4.3b and Figure 4.3c). The *I-V's* show a snapback due to the large increase of electrical conductivity. For VO_2 devices the increase is about 3 orders of magnitude over the range of 10 degrees. NbO_2 has the similar conductivity increase between the V_{TH} and the beginning of the ON-state. For devices based on these two materials, the device voltage continuously decreases with increasing current in the ON-state up to 50 μA.

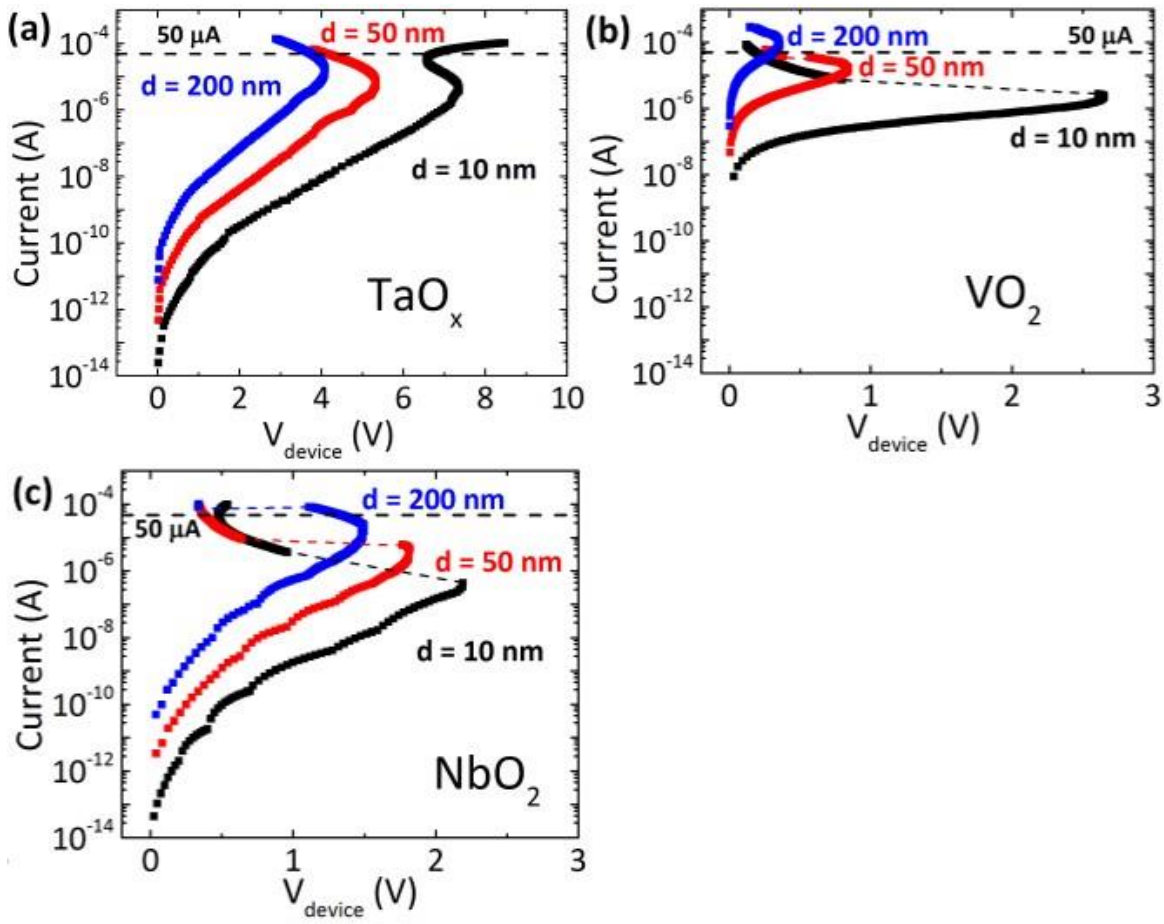

Figure 4.3 *I-V* characteristics of (a) TaO_x (b) VO_2 and (c) NbO_2-based selector devices with 10 nm thick functional oxide as a function of device diameter (from 10 nm to 200 nm).

The scaling trend of threshold voltage is apparent in the *I-V* plots. At a given voltage in HRS, the current density is almost independent of the device size and this would give the same temperature increase at runaway and the same threshold voltage in devices with size comparable to SiO_2 thickness. This clearly is not the case in devices considered here and from simulation results, all the three selector devices show increase of threshold voltage and temperature at threshold with decreasing device diameter. It is noticeable that TaO_x devices have much larger threshold voltages

than that predicted for the other two materials because of the lower electrical conductivity. This could be changed by engineering higher oxygen deficiency in the TaO_x but only at the expense of the increased leakage current.

The scaling trend of leakage current is also apparent in *I-V* characteristics: the leakage current decreases in inverse proportion to the device area as at low fields, the *I-V* is almost linear. For 10 nm devices, NbO_2 device has the lowest leakage current (2 nA), while VO_2 device has the highest value of 420 nA. The leakage current of even smallest VO_2 devices considered here (420 nA) is unacceptably high for most crossbar memory applications. All publications to date reported values of VO_2 conductivity to be in the 10-500 S/m range below IMT and it is not clear whether it can be substantially reduced. For TaO_x and NbO_2 devices, the leakage currents are 5 nA and 2 nA for 10 nm devices. This could be further reduced by increasing the oxide resistance during deposition, by engineering the electrode/oxide interface properties, and introducing additional barrier layers. Recently, several reports have illustrated the reduction of leakage current by using multilayer structure in NbO_2-based devices.[174, 175] Such approach, however, creates an obvious problem of increasing V_{TH} and the resistance of the device in the ON-state. This, in turn, would result in an increase of the device temperature during the SET and RESET operation (discussed below).

4.4 Scaling trend of current density and temperature

Figure 4.4 presents the radial current density profile for the three types of selectors at 50 μA. From these plots one can extract the filament size defined here as diameter of the cylinder where the current density is between maximum density (J_{MAX}) and 0.1 J_{MAX}. In the TaO_x devices (Figure

4.4a), the current density is almost uniform within the device, with a slightly higher density in the center. The weak dependence of current on position is a consequence of small device size compared to the size of the filament forming in large devices. This is also a reason for small different between V_{TH} and the ON voltage and lack of snapback in the *I-V*.

The current density profile for VO_2 (Figure 4.4b) and NbO_2 (Figure 4.4c) 200 nm devices show an almost uniform current density as they are still in the OFF-state (VO_2) or in the NDR before the snap back (NbO_2). In 50 nm devices, the filament is about 7 nm in diameter in VO_2 and 15 nm in NbO_2 devices. The reason for the difference between forming the filament or not is the steeper dependence of conductivity on temperature for NbO_2 and VO_2, as compared to TaO_x resulting in a higher conductivity at high temperatures. As a consequence, the current density is higher at the same filament temperature and the filament is smaller than the device size.

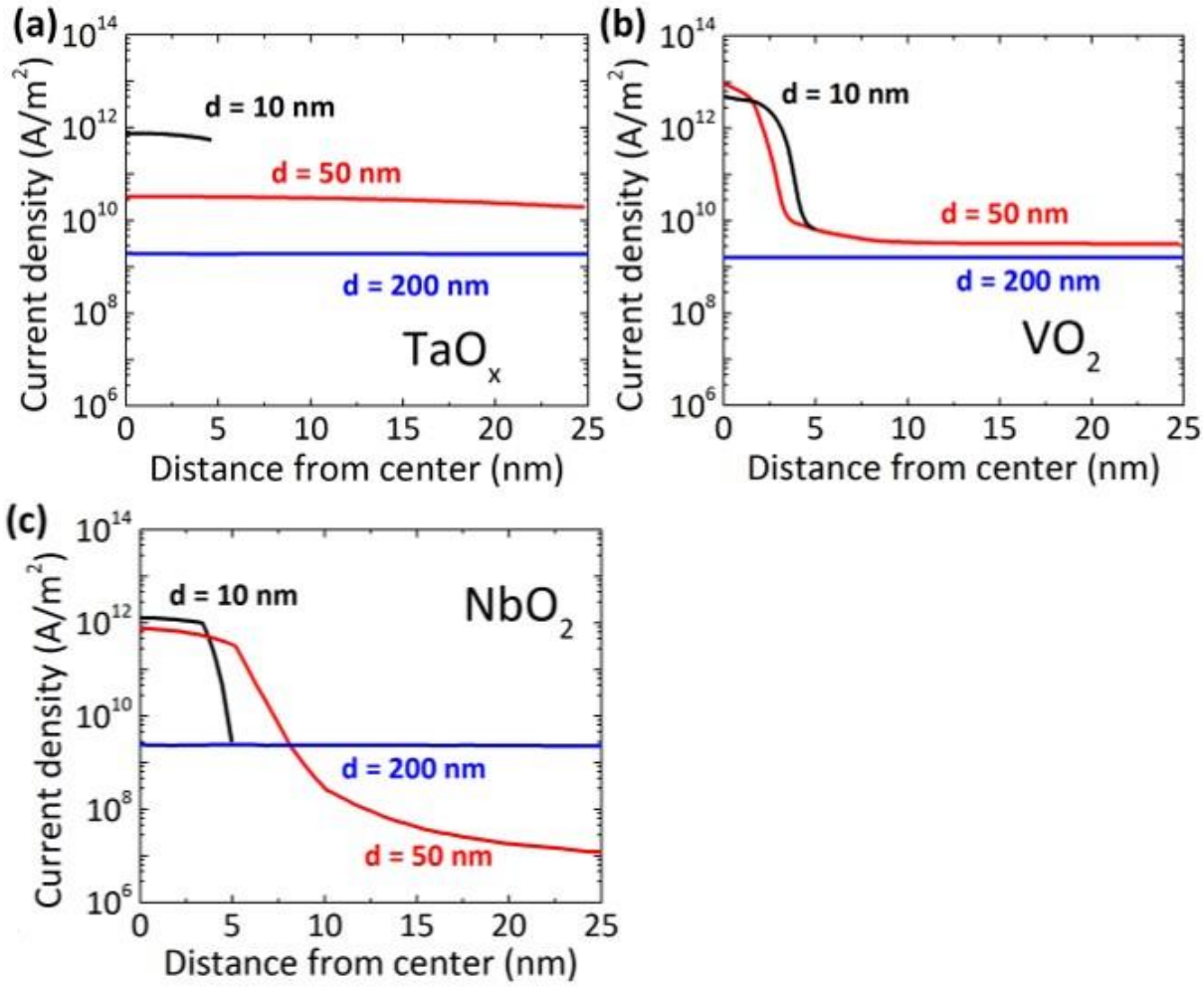

Figure 4.4 Radial current density profile for (a) TaO_x, (b) VO_2 and (c) NbO_2-based selector devices at 50 μA.

One of the challenges faced by the selection devices is the ability of sourcing enough current to switch the memory element. The value of switching current suggested by Narayanan *et al*. is 50 μA.[44] With the current flowing through the small device or filament, the local temperatures can reach values high enough to destroy or permanently affect the device characteristics. Estimating the temperatures should, therefore, be an integral part of a scaling exercise.

The maximum temperature in the center of the functional oxide layer at the total device current of 50 μA is shown in Figure 4.5. In TaO_x devices, the temperature is 510 K for a 200 nm device, and 1300 K for a 50 nm device. This is primarily due to the increase of the device resistance with decreasing size, which results in much higher dissipated power at constant current of 50 μA. An additional factor is the increased thermal resistance in smaller devices. The calculated thermal resistances are about 5.2 K/μW and 1.1 K/μW for 50 nm and 200 nm devices. In structures smaller than 50 nm, the predicted temperature would be even higher. At this point, however, the proposed model can no longer be used as many of the processes not included in the simulation would start taking place. This could include defect generation, diffusion, interfacial reaction, and/or melting. In addition, the thermal and electrical conductivities would likely diverge from the values used in the simulation.

In VO_2 devices, the device temperatures at 50 μA do not change with device diameter and exceed the transition temperature only by 20 K. The small temperature increase is due to high conductivity of the metallic phase and low dissipated power. In case of a 200 nm device at 50 μA, the device has not transitioned to the ON-state, which is the reason for the uniform and lower device temperature than in smaller devices. The NbO_2 devices behave similarly to VO_2 devices. The only difference is larger temperature increase above transition temperature for small devices (80 K for diameters ≤ 100 nm) due to lower thermal and electrical conductivities compared to those of VO_2.

It is apparent that the leakage current in this class of devices is anticorrelated with the temperature increase in the ON state. The lower the leakage current, the higher the temperature at 50 μA. The

more conductive materials have temperature low enough to be stable but have high leakage current. The low leakage ones, could be destroyed by unacceptably high temperatures. This is a difficult trade off that could be alleviated only by using materials with a very rapid increase of electrical conductivity with temperature.

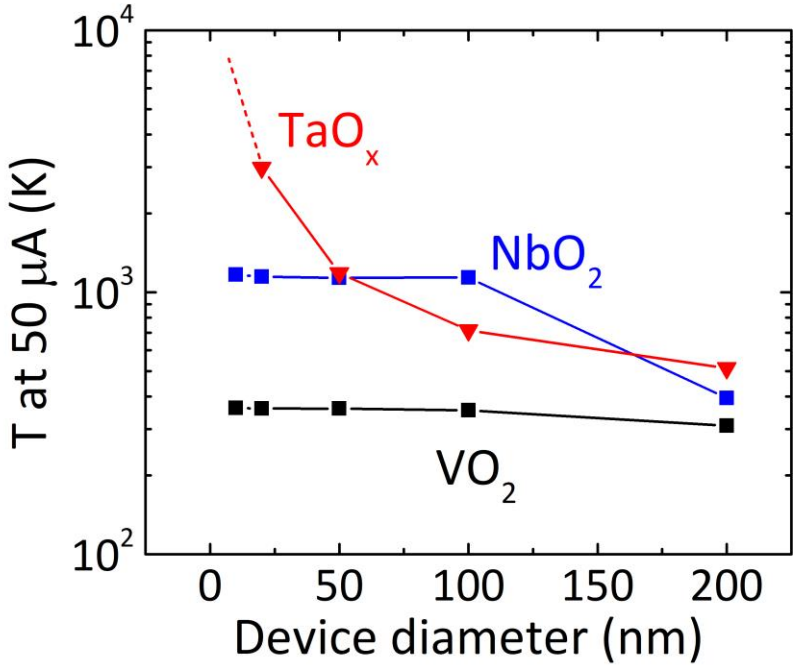

Figure 4.5 The highest temperature within the device at 50 μA.

4.5 Effect of oxide thickness on V_{TH}

Figure 4.6 shows the threshold voltage as a function of oxide layer thickness for 10 nm devices. V_{TH} decreases linearly with decreasing thickness for all three functional materials. The underlying reason for the decrease is an increase of dissipated power at a given voltage with the decrease of thickness. The NbO_2 and TaO_x devices show a higher slope than VO_2 devices, due to the electric field dependence on conductivity (β) in the Poole-Frenkel formula. This trend was also observed

experimentally.[71] Cha *et al*. have reported the scaling behavior of NbO_x-based selector devices with the threshold voltage increasing linearly with oxide thickness. Their devices required forming i.e. formation of a permanent small diameter filament but if one assumes that the filament diameter does not depend on oxide thickness, the results should reflect a true dependence on thickness.

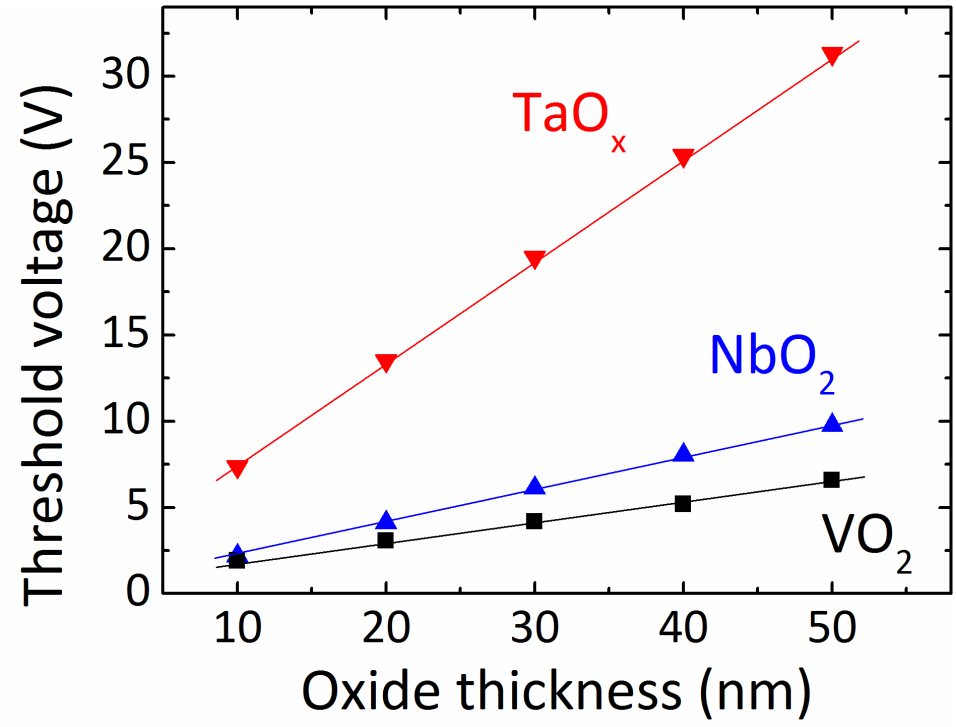

Figure 4.6 Threshold voltage as a function of oxide layer thickness for three types of selector devices.

4.6 Effect of sink temperature on device characteristic

Figure 4.7 presents the threshold voltage and leakage current as a function of sink temperature for 10 nm diameter and 10 nm thick oxide TaO_x and NbO_2 devices. The results of VO_2 devices are not shown because the IMT temperature was only 340 K.[106] As is apparent in Figure 4.7, the

threshold voltage decreases with increasing sink temperature while the leakage current increases for both TaO_x and NbO_2 devices. The leakage current and threshold voltage are obviously connected. Higher current in the OFF-state heats up the device at lower voltages. In NbO_2 devices, within the range of 300 K to 353 K, the threshold voltage dropped from 2.2 V to 1.6 V, 27% reduction, while the leakage current increased from 2.4 nA to 13.5 nA, a 460% increment. For TaO_x devices, the threshold voltage decreased 4% and leakage current increased 81%. This is the result of the higher activation energy for the electrical conductivity of NbO_2 compared to that of TaO_x. Variation of temperature will increase the energy loss in the OFF state of the device and decrease the read margin, which needs to be considered in the circuit level design of the memory array. Similar trends of threshold voltages have been observed in experiments.[91,93]

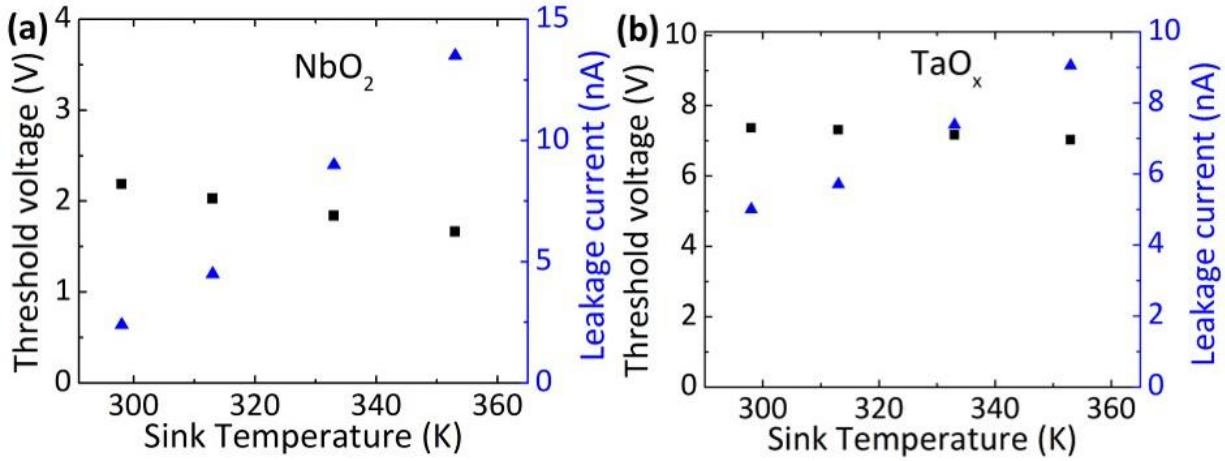

Figure 4.7 The effect of sink temperature on NbO_2 (a) and (b) TaO_x device characteristics. Values of simulated threshold voltage are marked by black squares, that of leakage current by blue triangles.

4.7 Benchmarking of thermal-induced selector devices

The goal of this section is to evaluate whether the scaled threshold switching devices based on the thermal runaway mechanism are suitable for selector device applications using the existing design constraints for 1S1R cell. It also can provide possible directions for the future work.

On the circuit level, I assume V/2 biasing scheme to simplify the design constraints for the selector devices. I also assume an indirect transition strategy between consecutive read/write operations and 0% design margin on all parameters of interest. The detailed discussion of different biasing schemes and transition strategies was covered in previous reports.[166,167] Since selector devices are coupled with the memory element in each 1S1R cell, one needs to specify the parameters of the memory element. Below, I adopt a set of parameters proposed to represent a generic memory element by Narayanan *et al*.[44] The SET voltage and current are 1.2 V and 3 μA with the RESET voltage and current of 0.8 V and 30 μA. The resistances are 400 kΩ and 26.7 kΩ for HRS and LRS. The parameters of interest for 1S1R cell include V_{TH}, ON-state current and V_{WRITE} with memory element in HRS and LRS. Those for a selector device include voltage snapback with memory element in HRS and LRS, leakage current, and the temperature at WRITE_RESET (RESET operations require a higher current than SET and results in higher temperature).

The operations of 1S1R cell are READ, WRITE_SET and WRITE_RESET. During READ operation, the selector device needs to be in the ON-state. This is because the OFF-state resistance of the selector is much higher than HRS of the memory device and the READ current difference between a memory element in HRS and LRS is too small to be detected reliably if the selector

device is in the OFF-state. After the selector device turns on, the voltage across the selector drops while it increases across the memory element. However, if the voltage across the selector drops more than the SET or RESET voltage of the memory element, then the memory element would switch and the READ operation would fail. Therefore, one of the constraints during READ operation is that the voltage drop between the OFF and ON state in selector cannot be higher than SET and RESET voltage for the memory element. For the WRITE_SET and WRITE_RESET operations, the selector device also needs to be in ON state and should be able to deliver 50 µA.

The parameters of the scaled 1S1R cell are extracted from the simulated *I-V* characteristics with two values of load resistance (400 kΩ and 26.7 kΩ corresponding to the HRS and LRS of memory element). All simulations have been performed assuming 10 nm diameter with 10 nm thick functional layer. The simulated *I-V*'s are shown in Figure 4.8. As can be seen, both VO_2 and NbO_2 devices exhibit snapback, but TaO_x device does not. The threshold voltages of the selector devices are the same when the memory element is in either HRS or LRS. The values of each parameter of interest are listed in Table 4.2.

All three selectors have higher threshold voltages than SET and RESET voltage of the memory element, which requires the snapback voltage to be smaller than SET and RESET voltages to allow for the READ operation. This condition is met only by TaO_x selector. For VO_2 and NbO_2 selectors, the voltage snapback with memory element in HRS (LRS) is higher than the SET (RESET) voltage of the memory element. This implies that memory element will switch when the selector device turns on. However, the threshold voltage for TaO_x devices are higher than 7 V, which will lead to undesired high power consumption during operations.

For the ON-state current, all three selectors can drive enough current through the memory element for both WRITE_SET and WRITE_RESET operations at the required WRITE and SET voltage. The leakage current is another important device parameter for the crossbar array as discussed above. Clearly, the leakage current of VO_2 device is much higher than the desired value. For TaO_x and NbO_2 devices, the leakage current is close to the target, and the further reduction of the leakage could be done possibly through the engineering of the metal/oxide interface properties. In addition, the very small value of leakage current is a requirement for large array size used as main memory, the smaller size embedded memory application could accept higher values.

One of the new insights in this simulation is the temperature of the selector device in the ON state, since the temperature is related to the endurance and retention failure of the oxide-based devices. [136,137] The temperature of VO_2 device is lower than 400 K, due to the low transition temperature and small temperature increase in the ON state. The temperature for NbO_2 device (1100 K) is possibly acceptable as long as it shows desirable endurance. But, the temperature of TaO_x device (>2000 K) is unacceptable.

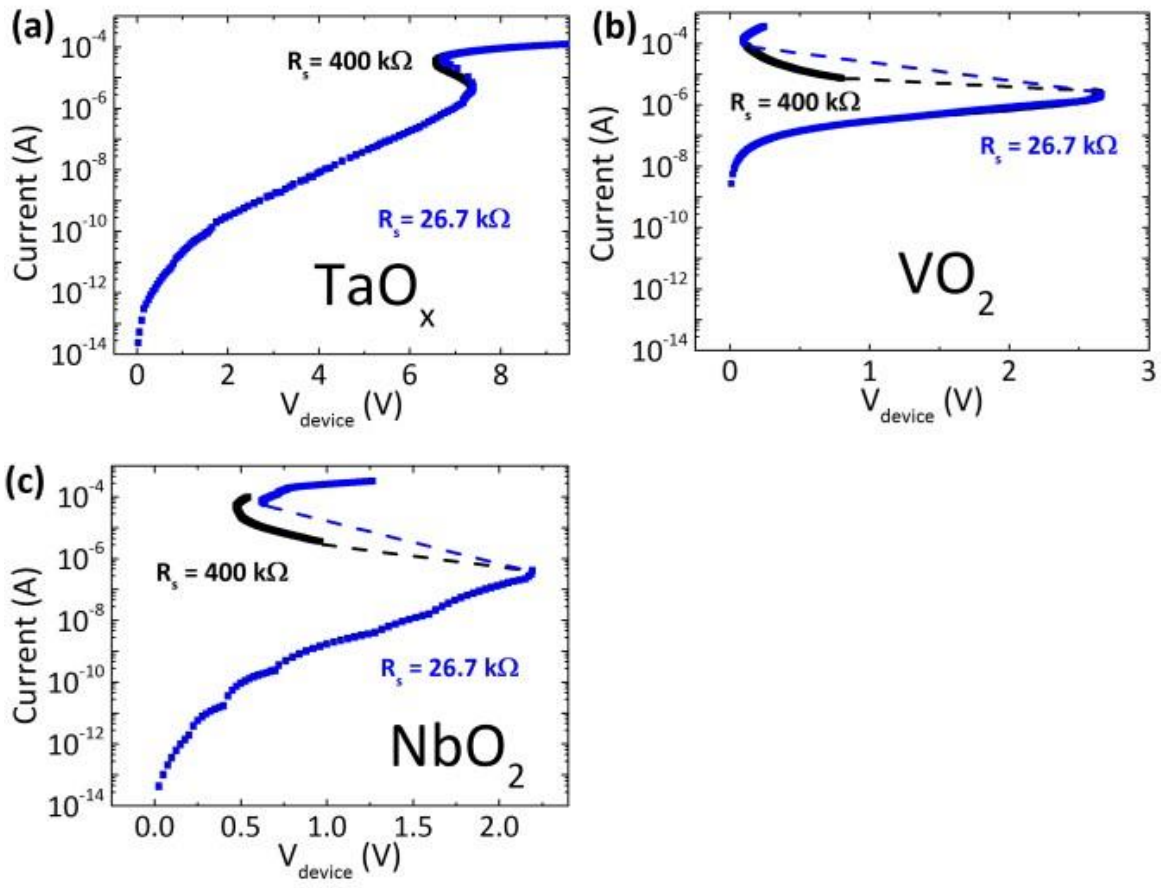

Figure 4.8 *I-V* characteristics of TaO_x (a), VO_2 (b) and NbO_2 (c) selector devices with load resistance of 400 kΩ and 26.7 kΩ.

Table 4.2 List of parameters of interest for 1S1R cell and selector devices for device benchmarking analysis.

	VO_2 device	TaO_x device	NbO_2 device
Threshold voltage (V)	2.6	7.4	2.2
Voltage snapback with NVM in HRS (V)	1.8	0	1.2
Voltage snapback with NVM in LRS (V)	2.5	0	1.6
ON state current with NVM in HRS (μA)	7.4	>3	3.6
ON state current with NVM in LRS (μA)	84.8	>30	63.5
V_{WRITE} with NVM in HRS (V)	3.8	8.5	2.4
V_{WRITE} with NVM in LRS (V)	2.8	7.6	2.2
Leakage current per device (nA)	420	5	2
Temperature of selection device at WRITE_RESET (K)	360	>2000	1100

4.8 Discussion

The specific target values of selector device performance strongly depend on the characteristic of the paired memory cell and the size of the crossbar memory array. But in general, the selector device should have a leakage current about 100 pA, a threshold voltage between 2 V and 4 V, and an ON state current of 100 μA. These general figures of merit came from the collaboration with our industrial sponsors. The temperature budget of the selector device, however, has not been discussed since the material system and device structure have not been decided. While, from the temperature analysis from Choi *et al.* on the 28 nm technology node FinFET transistors,[176] the junction temperature of one transistor could easily reach 400 K during normal operation at 1 GHz.

Therefore, I could assume the selector device should also have a similar temperature budget in order to be efficiently cooled down by the packaging solutions.

With the target values for selector device defined, the VO_2, NbO_2 and TaO_x-devices could be evaluated using the simulated benchmarking results discussed above.

(1) Threshold voltage. Both VO_2 and NbO_2 device have V_{TH} in the range of 2 V to 4 V, but the TaO_x device has a V_{TH} that is too large due to the low electrical conductivity.

(2) Leakage current. The target value is 100 pA, and none of these three devices can reach this value even at 10 nm device diameter, with NbO_2 and TaO_x devices showing leakage current 1 order of magnitude higher than the target. Therefore, additional layer could be inserted to the device structure to increase the device resistance in the OFF state or the materials themselves could be engineered to achieve a lower conductivity.

(3) ON state current. All of the three devices could achieve a ON state current of 100 μA if enough bias is applied to these devices.

(4) Device temperature in the ON state. The temperature budget is about 400 K, and only VO_2 device can meet this target due to a relatively low IMT transition temperature. Both NbO_2 and TaO_x devices reach a much higher temperature in the ON state, due to high IMT transition temperature and low electrical conductivity, respectively.

From the above evaluation, currently, none of these three metal-oxide based devices can meet all the figures of merit for selector application. The preferred material properties could be calculated from the target values assuming a 10 nm × 10 nm square crossbar device with 10 nm thick functional layer. Assume the threshold voltage is 2 V, and the device voltage is 1 V at the leakage

current (100 pA), therefore the electrical conductivity of the functional layer should be 0.01 S/m in the OFF state. When the device turns on, if there is no load resistor connected in series, the device voltage stays the same as the threshold voltage. Since the filamentary behavior is not desired in the ON state, due to the snapback after the threshold point which could lead to undesired switching of the memory cell, a bulk current conduction is assumed in the ON state. Therefore, the 2 V and 100 μA gives an electrical conductivity of 5000 S/m for the functional material. As a result, the material should have a conductivity increase over 10^5 from OFF state to ON state. The temperature induced phase transition is not desired since it always leads to the filamentary behavior in the ON state because the temperature in the device is not uniform due to the lateral heat dissipation. However, the electrical conductivity change of the material could still be due to a phase transition, but induced by an electronic effect, and the entire device region should transition into the high conductivity phase eliminating the localized filament.

4.9 Summary

In summary, the scaling trends of three oxide based electrothermal selector devices (TaO_x, VO_2 and NbO_2) were simulated using finite element simulation. The device characteristics including threshold voltage, leakage current, filament size and temperature in the ON-state were extracted and compared between the three types of selectors. With decreasing the device diameter, the threshold voltage increases and the leakage current decreases, respectively. Both VO_2 and NbO_2 devices show the filamentary behavior in the ON state due to insulator to metal transition which lead to a snapback in device voltage during threshold switching. The ON state temperature of VO_2 and NbO_2 device is slightly above their transition temperatures, while TaO_x device shows a much higher temperature (> 2000 K) due to the low electrical conductivity. Further, the 1S1R cell

benchmarking of these selector devices with 10 nm diameter was performed assuming generic memory element parameters. TaO_x device has a large threshold voltage (> 4 V), which is not favorable for selectors, and the leakage current is about one order of magnitude higher than the target value. Also, the tradeoff between leakage current and ON-state temperature seems too restrictive to allow an acceptable compromise. The NbO_2 device shows a suitable threshold voltage, but the leakage current is one order of magnitude higher than the target value and the temperature in the ON state (1100 K) due to the IMT transition is out of the temperature budget. VO_2 device has a transition temperature (340 K) that is too low for the real application and the leakage current is also three orders of magnitude higher than the target value. Therefore, currently, none of these three metal oxide based devices is suitable for selector application. The preferred material properties for selector device based on the figures of merit were calculated assuming a 10 nm × 10 nm square device with 10 nm thick functional layer, resulting in that the electrical conductivity should increase from 0.01 S/m in the OFF state to 5000 S/m in the ON state, which I think should be preferable due to an electronic effect.

5 Summary and Future work

5.1 Conclusion

In this Ph.D. study, I have addressed: (a) an electrothermal finite element model based on Joule heating that can reproduce the devices' electrical and thermal characteristics of thermal-induced threshold switching devices; (b) experimental measurement of the temperature distribution on the top surface of TaO_x-based threshold switches using scanning thermal microscopy and scanning Joule expansion microscopy; and (c) the simulation of scaling behavior down to 10 nm in diameter of VO_2, NbO_2 and TaO_x-based thermal-induced threshold switches for selector applications.

Chapter 2 reported on the understanding of the switching mechanism of VO_2-based threshold switching devices by comparing the experimentally measured device characteristics and the finite element simulation results. The devices were measured at various stage temperatures to obtain the *I-V* and transient responses during switching. The electrothermal finite element model was developed based on the Joule heating effect and the device performance was simulated using the same testing conditions as the experiments. The good agreement between experimental data and simulation results strongly indicated that the threshold switching in VO_2- based devices is purely thermally induced without the need to invoke electronic effects. In addition, the results suggested that the electrothermal model I have developed is capable of reproducing the device characteristic of thermal-induced threshold switches and the model should be able to be applied to any material system and device structure of thermal-induced switches.

Publications contributing to this chapter:

1. **Li, D.**; Sharma, A.A.; Gala, D.K.; Shukla, N.; Paik, H.; Datta, S.; Schlom, D.G.; Bain, J.A.; Skowronski, M. Joule Heating-Induced Metal–Insulator Transition in Epitaxial VO2/TiO2 Devices. *ACS Appl, Mater. Interfaces*, 2016, **8**, 12908.
2. **Li, D.**; Sharma, A.A.; Shukla, N.; Paik, H.; Goodwill, J.M.; Datta, S.; Schlom, D.G.; Bain, J.A.; Skowronski, M. ON-state evolution in lateral and vertical VO2 threshold switching devices. *Nanotechnology*, 2017, **28**, 405201.

Chapter 3 described the experimental measurements of the temperature distribution on the top surface of TaO_x-based threshold switching devices using scanning thermal microscopy and scanning Joule expansion microscopy. The TaO_x devices have also shown threshold switching behavior based on thermal-induced mechanism and the *I-V* characteristic was successfully reproduced by the electrothermal model. The scanning thermal microscopy measured the absolute temperature on the top surface of the device using the integrated thermocouple at the tip of the specially made AFM probes. Scanning Joule expansion microscopy measured the thermal expansion signal on the top surface of the device due to Joule heating effect, which had a better spatial resolution than scanning thermal microscopy. The TaO_x-based devices were measured by these two scanning probe techniques at several current levels up to the threshold switching point along the device *I-V*, and both the temperature profiles and the thermal expansion values matched with the electrothermal simulation results. The measurement results showed in this chapter supported the argument of thermal-induced switching as the mechanism of threshold switching of TaO_x-based devices, excluding the other proposed mechanisms, such as the nucleation model.

Publication contributing to this chapter:

1. **Li, D.**; Ramer, G.; Yeoh, P.; Hoskins, B.; Ma, Y.; Bain, J.A.; Centrone, A.; Skowronski, M. Scanning Probe Thermometry of TaO_x-based Threshold Switching Devices for Selector Applications. Submitted.

Chapter 4 reported the simulation results on the scaling behavior of VO_2, TaO_x and NbO_2-based threshold switching devices. The previous two chapters showed evidence of thermal-induced threshold switching in TaO_x and VO_2-based devices and that the electrothermal model I developed could reproduce the device behavior. Recent papers also reported the NbO_2-based devices as thermal-induced threshold switches. Therefore, all the three metal oxides share the same mechanism as threshold switches and can be simulated by the electrothermal model. The scaling behavior of these three devices were simulated using a crossbar device structure with the device diameter from 200 nm down to 10 nm. The device characteristics, such as *I-V* behavior, leakage current, and temperature in the ON-state were extracted from the simulation results and compared among the three devices. The results suggested that the device performance highly depends on the properties of paired memory cell and the thermal-induced selector devices suffer from a tradeoff between the leakage current and ON-state temperature. Currently, none of these three threshold switching devices can meet all the figures of merit for selector device application. The preferred material properties for selector application were calculated based on the target values of the device performance and an electrical conductivity change over 10^5 should be achieved between OFF state and ON state.

Publication contributing to this chapter:

1. **Li, D.**; Goodwill, J.M.; Bain, J.A.; Skowronski, M. Scaling behavior of oxide-based electrothermal threshold switching devices. *Nanoscale*, 2017, **9**, 14139.

5.2 Future work

The successful device temperature measurement using scanning probe thermometry shown in Chapter 3 opens a wide range of possible future work. First of all, the measurements in this study were only conducted in the OFF-state and up to the threshold switching point of the TaO_x devices due to the device failure at higher bias. The future work could modify the device structure, for example using planarized bottom electrodes, to improve the stability of the devices and measure the temperature profiles in the deep NDR region or in the ON-state region to capture the current constriction and extract the size of the conductive filament. Secondly, the thermometry measurements can be applied to memory switching devices as well, where there is a permanent conductive filament after electroforming, and the temperature profile on the top surface should show a clear small hot spot related to the size of the filament. As the properties of the filament in memory switching devices is still an open question, the temperature profile on the top surface is capable of providing the information of the filament size and the evolution with device current. Thirdly, in memory arrays with nanometer scaled devices, the devices are close to each other in physical locations and during the operation of each single device, the temperature spreading could increase the temperature of nearby unselected devices and increase the leakage current or degrade the devices. Therefore, one can measure the temperature profile in a memory array to investigate how large is the heated zone around one device and what is the absolute temperature.

In terms of simulation, the future work can focus on improving the accuracy of the electrothermal model. The current model only assumes the electrical conductivity as a function of temperature and electric field, however, the conductivity depends on the local composition of the oxide film as well. The model could include the atomic motion under field and thermal gradient, which leads to local composition changes and related to the local electrical conductivity. This modification can be applied to the simulation of the conductive filament formation and evolution in the ON-state. In addition, the simulation results shown in this study were based on the existing device structure, however, the current device configuration may not be the best option. As the devices studied here are thermal-runaway-induced threshold switches, the thermal environment of the device can greatly affect the device performance. The future research could try to change the device geometry, such as the substrate material, the substrate thickness, and the material of insulation layer, to engineer and improve the device performance. For example, the power needed to reach thermal away can be reduced by increasing the thermal resistance of the device to enable the low-power operation.

Appendix A. Electrical testing setup

The electrical testing setup used in this study is described below. The quasi-DC testing were performed in the work shown in Chapter 2 and Chapter 3 on VO_2-based planar devices and TaO_x-based devices. The testing setup is shown in Figure A.1 using a Karl Suss PM6 probe station. Agilent 4155C semiconductor parameter analyzer was used as the voltage source with the ramping rate of 4 V/s. The load resistor (R_L) was connected in series with the source and the device under testing to act as a current limiter in the circuit. The R_L was an external resistor for the testing on VO_2 devices showed in Chapter 2, while it was an integrated on-chip resistor for the testing on TaO_x devices used in Chapter 3. In Chapter 2, the VO_2 devices were tested at various stage temperatures using a Lakeshore Model CRX-VF cryogenic probe station. The VO_2 devices were inside the vacuum chamber of the probe station, and the voltage source and load resistor were outside.

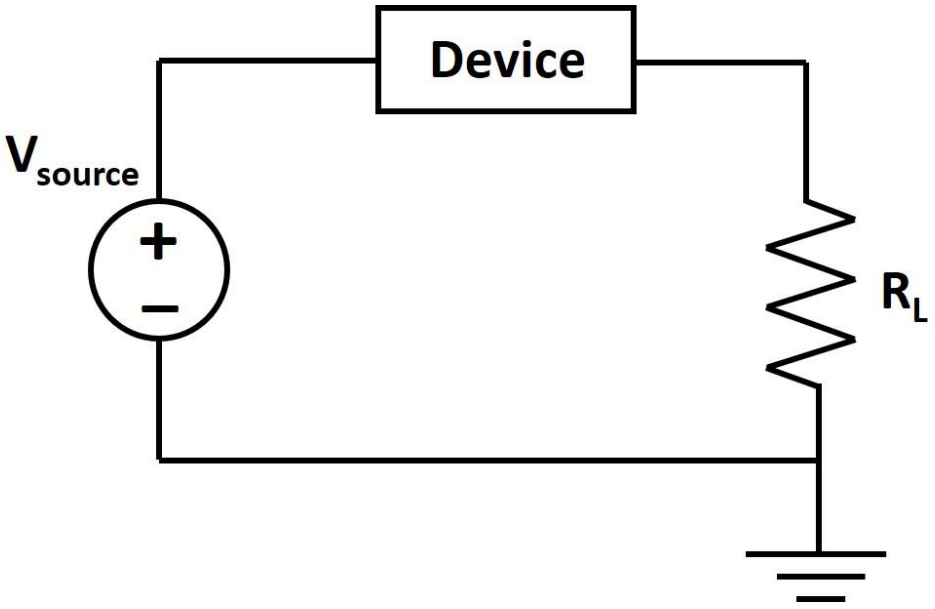

Figure A.1 Circuit scheme of DC testing setup used in this study.

In Chapter 2, I also tested transient response of the VO_2 devices to measure the incubation time before threshold switching event and the testing setup is shown in Figure A.2. The Agilent B1110A pulse generator was used as the voltage source with a built in 50 Ω resistor. The applied voltage pulses were with 2 ns ramp up and ramp down time, and the pulse length and amplitude were varied. An Agilent DSO6104 oscilloscope was connected in series with the pulse generator, VO_2 device and the load resistor. The oscilloscope was set to with 50 Ω resistance and monitored the voltage over that resistance. Therefore, the current that flowed through the circuit could be calculated accordingly (V_{scope}/50). And the device voltage was calculated by $V_d = V_{source} - V_{scope} - I \times R_L$.

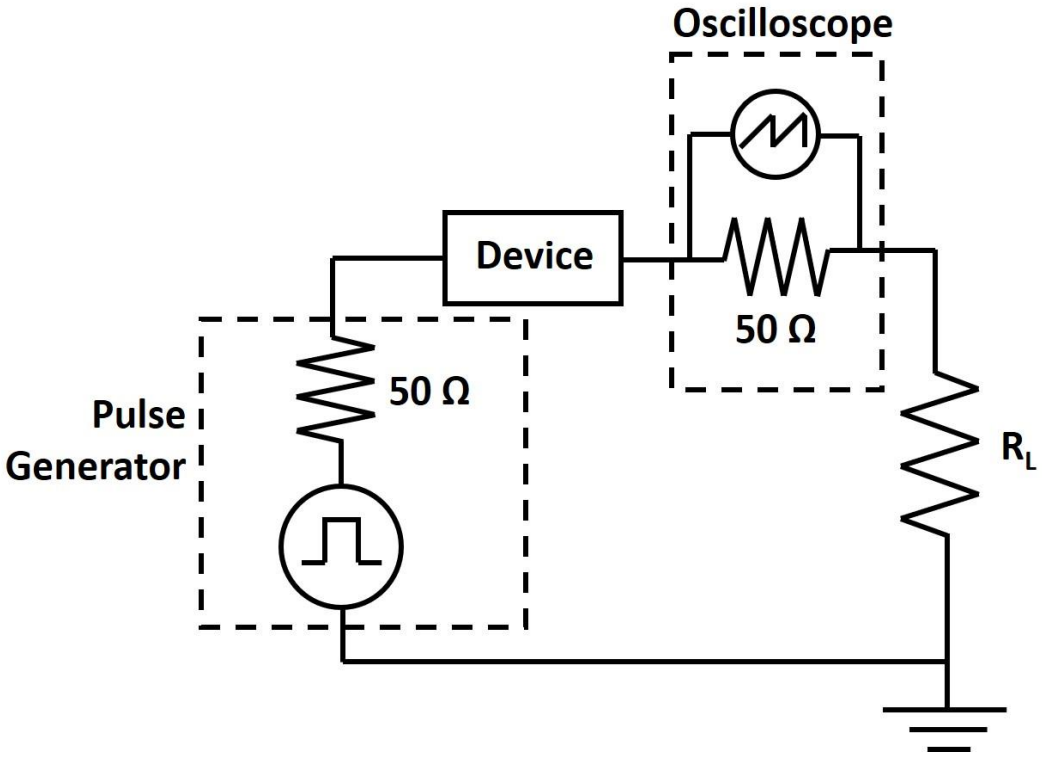

Figure A.2 Circuit scheme of transient measurements testing setup.

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