HIGH EFFICIENCY CLASS-D RF AMPLIFIERS
AND
MOBILE NMR SYSTEMS

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ABSTRACT

This thesis details the development of a hand held mobile NMR system. The new system addressed the drawbacks on most of the existing NMR systems of being physically large and heavy with poor power inefficiency. In order to achieve the goal of producing a compact and power efficient NMR system, several high efficiency Class D RF amplifiers were developed which showed efficiencies of over 80%. The single cycle controlled PWM amplifier working at 2 MHz was a novel design and no other PWM Class D amplifiers has been reported to operate at high frequency with output power greater than 100 W. Development of the 20 MHz amplifier with 100 W constant amplitude output showed that the Class D amplifiers are suitable for NMR applications even at high frequency and further development of this amplifier to work at 17 MHz with amplitude modulation was successful. It paved the way for the development of a full mobile system with the newly available 17 MHz Mini-MOUSE sensor. The fully integrated mobile system was developed using SoC FPGA technologies. The use of a 400 Msps DDS device for RF pulse generation results in a broadband system. A duplexer was developed to enable sensor tuning and matching with the receiver amplifiers on the duplexer output stage provided 72 dB gain. The web based control program running on an iPad has shown great portability and it allows the system to be operated outdoors, even in remote areas. Experiments on industrial applications has shown successful T_{2eff} measurements on polymer composites and rubber samples and showed the potential for such a system to be used in industrial applications. The fully integrated system prototype fits in a case measuring 140x120x100 mm (LxWxH) and weighs 800 grams and fulfil all the requirements for a mobile NMR system.

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List of Acronyms and Names

Auto Phase	Automatically phase the data for symmetrical real and imaginary components
CPMG	Carr, Purcell, Meiboom, Gill, refers to a pulse sequence developed by them
CPMG_Int	Integral of echo data from CPMG experiment to obtain a T_2 decay curve
DDS	Direct Digital Synthesizer
FID	Free Induction Decay
FPGA	Field-Programmable Gate Array
KEA	A spectrometer for bench top NMR systems
LapSpec	A portable NMR spectrometer
MicroZed	A development board for Xilinx 7000 SoC system
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOUSE	Mobile Universal Surface Explorer, a hand held size sensor
MRI	Magnetic Resonance Imaging
NMR	Nuclear Magnetic Resonance
Phase Cycling	NMR experiment technique to improved signal
Prospa	A software program for controlling the KEA spectrometer system
RCA	Rock Core Analyzer
SNR	Signal to Noise Ratio
SoC	System-on-Chip
Wobble	An experiment for tuning and matching probe/sensor

Chapter 1. Introduction

Nuclear Magnetic Resonance (NMR) systems have become very popular due to their non-invasive nature and are used extensively in chemical analysis [1,2], well logging [3,4,5], and medical diagnostic applications [6,7,8,9]. Oil and gas exploration uses NMR systems to measure porosity of rock core samples to check the oil content and the possibility of extraction. Heritage preservation uses NMR systems to measure moisture content and their distribution on paintings to adjust the storage environment. The quality control of polymer products uses NMR systems to monitor and measure the cross linking of the molecules to determine quality and aging. Those are just some of the industrial applications of NMR systems. More details of the NMR process will be provided in Chapter 2.

Presently most NMR systems are only operational in laboratory environments due to the high power requirements, large electronic consoles and heavy superconducting or permanent magnets needed for these systems. It has long been the goal of NMR application engineers to have portable or mobile NMR systems, allowing the NMR technology to be used outdoors and in remote areas. Most of the mobile NMR systems in the market are bench top systems (a list shown in section 2.2), consisting of a computer, a spectrometer and a sensor. While the bench top systems are mobile, in that they can be easily moved from one laboratory to another, it is not easy to move outdoors for doing *in-situ* measurements as the weight of a full system is typically in the range of 30 to 100 kg. A truly mobile system should be able to be carried by the user to any area and operated without much extra physical effort. The goal of a mobile NMR system is then to bring the system to the sample instead of bringing the sample to the system. For example, a mobile system would allow the monitoring of tyre rubber degradation on high performance cars at the race track in real time. It also makes it possible to monitor the aging of plastic piping in remote areas such as oil fields. However, the design of a mobile system places demanding hardware and power requirements, as it is most likely to be battery powered. In order to be mobile, considerable size and weight reduction on all electronic components and sensors are required. NMR systems are expensive in general, even a low cost bench top system cost approximately 20,000 USD. The design of a new mobile system will aim to reduce the system cost.

A full NMR system can be seen as having three functional blocks as shown in Figure 1.1. The user interface provides system control, while the electronics consist of both digital and analogue RF electronics, which determines the capability of the system. The sensor detects the NMR signals from samples as determined by the applications of the system.

Figure 1.1 The three functional blocks of a full NMR system

One of the most important requirements in producing a successful mobile NMR system is a compact RF amplifier. This amplifier also has to be efficient to conserve power and needs to have a broad frequency range to enable multiple applications. Classical RF amplifiers are not suitable as they have low efficiencies, while higher efficiency class D audio amplifiers are also not suitable because of their low frequency of operation range. Mobile NMR applications such as well logging and rock core sample analysis requires the amplifier to have a fast response time and a ring down time shorter than one microsecond. Amplifiers that have all of the above requirements are not currently available on the market.

With advances in MOSFET technology [10,11,12], the new power MOSFETs currently available are more efficient and can be switched at frequencies of tens of MHz. They are also available in small packages and gives the possibility of building high efficiency Class D amplifiers that can operate outside of the audio frequency and into the MHz frequency range. This will be a totally new operating range for Class D amplifiers. Small devices also mean the amplifier can be compact, which is ideal for a mobile system.

For a full NMR system, a computer is always needed for user control and data acquisition and processing. In the last few years, developments in small digital electronics have produced some unique FPGA devices that now include powerful processors. These are System-on-Chip (SoC) devices that essentially combine a processor and FPGA logic fabric onto a single chip. An example of such a SoC is the Zynq-7000 from Xilinx [13], which will be capable of processing NMR data in real time. With some suitable supporting hardware, a SoC system

can be used to replace the computer and lots of the digital electronics normally needed in a NMR system, greatly increasing the mobility of a NMR system.

Looking at all of the above positive possibilities, the construction of a full mobile NMR system is very possible and it is the ambition and motivation of this research to develop such a system. The bulk of the work is the development of compact electronics to minimize system size. A compact Class D RF amplifier reduces the overall size of the electronics. The SoC FPGA system can handle data processing and provides a host system for the user interface. Integration with a hand held sensor gives a full mobile NMR system.

The overall objective of the work was the development of a truly mobile NMR spectrometer system and the integration of this spectrometer with a commercially available NMR MOUSE sensor. In order to achieve this the following goals had to be met:

- First is the development of high frequency Class D amplifiers. While the target sensor operates at 17 MHz, the amplifier design can start at a lower frequency to see if Class D amplifiers are actually suitable for NMR applications. Device selection is important and research will be done to find the suitable MOSFETs and gate drivers to use on the design. After the construction of the amplifiers, pulse sequences will then be developed to test the amplifiers in a 2 MHz NMR system. Different switching techniques such as Single Cycle Control PWM can be explored to see if the rise time and ring down of the amplifiers can be improved. Higher frequency amplifiers can then be developed to see the switching capability of the market available MOSFETs. Finally a 17 MHz amplifier can be developed to work with the MOUSE sensor.
- The second goal is the development of digital electronics for the new mobile system. It can make use of the new SoC FPGA technology, having a powerful processor in a compact package for processing the NMR data and generation of the pulse sequences. High speed ADC and DDS devices can be used for interfacing the analog and digital parts of the design. High gain and low noise amplifiers are also needed and will be designed to the requirements of the input lines to the ADC and capturing the NMR signal from the sensor.
- The third goal is the development of a user interface and control for the mobile system. The new SoC FPGA device can host a Linux operating system and allows the running

of a web server. This capability allows the use of a webpage as a user interface to run the full system. With a working user interface, the customised NMR pulse sequences to use on the MOUSE can then be developed.

- The fourth goal is the integration and testing of the full system. With the development of all the required hardware and software, the fully integrated system can be tested on samples with known properties, and compare results to the existing commercial KEA spectrometer system.
- The fifth and final goal is a demonstration of the mobile system performing industrial applications such as measuring T_2 (or T_{2eff}) of plastics and polymers.

This thesis first gives a brief introduction to NMR, followed by an overview of the hardware requirements for building mobile NMR systems and presents some examples of the smallest NMR systems available commercially (Chapter 2). Development work was first done on building some Class D amplifiers operating in the MHz frequency range and testing them on a 2 MHz bench top NMR system (Chapter 3). The tests performed using the bench top system proved that the Class D amplifiers are suitable for NMR applications. Then with the compact feature in mind, amplifiers that would work at even higher frequencies of 17 MHz and 20 MHz were built and tested with NMR MOUSE sensors (Chapter 4). The successful implementation of a 17 MHz amplifier with amplitude modulation capability together with a Xilinx SoC module allowed the development of a full mobile NMR system (Chapter 5). The software and hardware integration of the new system is given in detail and works with a recently developed handheld Mini-MOUSE sensor. A web based program running on an iPad was developed to run the full system. The final chapter discusses the results from all the development work and conclusions were made (Chapter 6).

The prototype system was tested on industrial applications such as polymer quality and reaction monitoring. The NMR test results are presented and they showed the full system is functional and stable. The successful construction of the full system proved that Class D amplifiers and SoC FPGA technologies can be used in mobile NMR system design and this work paves the way for future development of even smaller mobile NMR systems.

Chapter 2. NMR Theory and Hardware

This chapter gives some background information on Nuclear Magnetic Resonance (NMR) and the physics behind the phenomenon. A brief overview of NMR systems is presented, followed by some examples of NMR systems available on the market.

2.1. NMR Theory

2.1.1. Introduction to NMR

NMR was first reported in late 1945 on analysing bulk materials [14]. Due to the non-invasive and non-destructive nature of NMR, it has become a major tool in analytical chemistry and medical treatment nowadays. The mathematics behind NMR has been described in the works from Purcell and Bloch, etc [14,15,16]. Instead of repeating the mathematical details, here is a basic introduction to NMR using simple mechanics concepts.

The structure of an atom is well known, it consists of three particles: electrons, protons, and neutrons. Protons have positive charge and neutrons have no charge, together they form the nucleus of the atom. Electrons have negative charge and they orbit around the outside of the nucleus. Atomic number is the number of protons in the nucleus and it is a way of differentiating elements. The nucleus in the natural state is constantly rotating about an axis as illustrated in Figure 2.1.

Figure 2.1 Spinning nucleus

Nuclei with odd atomic numbers in their natural state will generate a small angular momentum, known as “nuclear spin, I ”. Nuclei with even atomic numbers have no net angular momentum, ie, $I = 0$, and they are not affected by a magnetic field. Since nuclei are

positively charged, nuclei with non-zero angular momentum will have a net magnetic moment, μ . In the presence of a magnetic field, B_0 , the vector sum of μ gives a net magnetization vector, M . Without the influence of any external magnetic field, nuclei are randomly oriented and $M=0$. When an external magnetic field is applied, the nuclei align with the field in either the same or opposite direction. The two different orientations have different energies according to Zeeman interaction [17,18]. The nuclei pointing at the same direction as B_0 are at lower energy state than the opposite direction, this is the reason for more nuclei pointing at the same direction as B_0 and their vector sum resulting in a non-zero M . Figure 2.2.

Figure 2.2 Nuclei orientation, (a) randomly oriented without a magnetic field, $M = 0$. (b) aligned with a magnetic field B_0 , $M \neq 0$.

Figure 2.3 Spin precession at the presence of a magnetic field.

In the presence of a magnetic field B_0 , protons which have magnetic moment begin to precess around the B_0 axis much like a spinning top precesses around the earth's

gravitational field as shown in Figure 2.3. This precession is at a constant frequency and is proportional to the strength of the magnetic field, known as the Larmor frequency (ω_0) and is expressed by the equation:

$$\omega_0 = \gamma B_0 \quad (1)$$

where γ is called the *gyromagnetic ratio* and is nucleus-dependent. For Hydrogen $\gamma = 2.675 \times 10^8 \text{ rad s}^{-1} \text{ T}^{-1}$ or 42.58 MHz T^{-1} .

The hydrogen nucleus ^1H , consisting of a single proton and has a large magnetic moment compared to the other nuclei, it is the most abundant and therefore the most used in NMR experiments. For this reason Hydrogen nuclei are often referred to as protons.

By convention, B_0 and the axis of precession are defined to be oriented along the z-axis of a Cartesian coordinate system. The motion of spin is described as either perpendicular (projected onto the x-y plane) or parallel to the direction of B_0 . Figure 2.4 shows the coordinate system with a non-zero M .

Figure 2.4 Coordinate system showing a non-zero M .

To measure M , a torque needs to be applied to cause it to rotate. This is done by applying an external magnetic field, B_1 at the Larmor frequency. The net effect is the

magnetization vector M rotate towards the x-y plane around the z-axis in a spiral trajectory as illustrated in Figure 2.5(a). Analysis of the magnetization vector M is very complex in the normal laboratory reference frame due to the rotation. A way to simplify that is the use of a rotating reference frame around the z-axis at the same Larmor frequency. The nuclear magnetic moments then appear stationary, i.e. $\omega_0 = 0$ and B_0 disappears because $\omega_0 = \gamma B_0$, therefore the B_1 field is able to apply a torque to the apparently stationary magnetization. If B_1 is also oscillating at the same frequency then it appears as a static vector at right angle to B_0 . This way the whole spiral motion becomes a single angle rotation between the z-axis and the x-y plane. Figure 2.5(b).

Figure 2.5 The effect of B_1 . (a) In laboratory reference frame M rotate towards the x-y plane around the z-axis in a spiral trajectory. (b) using a rotational reference frame for M , the spiral motion becomes a single angle rotation into the x-y plane.

The oscillating B_1 can be produced by driving a radio frequency (RF) transmitter coil with a sinusoidal signal at the Larmor frequency. The RF signal is known as an excitation pulse. If the RF pulse is left on long enough to provide enough energy to make M rotate entirely into the x-y plane as M' in Figure 2.5, this is known as a 90° pulse because it tips M by 90° .

When B_1 is removed by turning off the RF transmitter, the net magnetization M' is in the x-y plane rotating about the z-axis. If a receiver coil is placed perpendicular to the x-y plane, the motion of M' produces an electromotive force (EMF), oscillating at the Larmor frequency. This induces a voltage in the receiver. This is known as the free induction decay (FID). Figure 2.6 shows a FID signal from a water sample as an example. The FID is a time

domain signal and has real and imaginary parts. Quadrature modulation and detection circuits are used in transceivers to capture the NMR signals with both magnitude and phase information. In practice an FID signal often contains multiple frequency components therefore it is often easier to analyze in the frequency domain using Fourier transformation, converting the signal to magnitude and phase components.

Figure 2.6 Example of an FID signal

2.1.2. Relaxation Times T_1 and T_2

In the rotating reference frame as illustrated in Figure 2.5(b) earlier, a 90° RF pulse tips the magnetization vector M into the x-y plane as M' . When the RF pulse is switched off, M' starts to decay to zero and M slowly recovers to the equilibrium position along the z-axis. This recovering process is called longitudinal relaxation and is described by the equation.

$$M_z = M_0 \left(1 - e^{-t/T_1} \right) \quad (2)$$

where T_1 is called the longitudinal relaxation time. T_1 can be used to characterize materials and monitoring chemical changes as it reflects the interaction of nuclei in their molecular environment.

Another process happening after the 90° RF pulse is transverse relaxation. At the end of the RF pulse the protons start to precess in the x-y or transverse plane. The precession is in phase to start with, but due to their difference in magnetic environments, the protons precess at a different speed over time and hence become out of phase as shown in

Figure 2.7(a). After more time elapses they appear to be completely random, resulting in zero net transverse magnetization, Figure 2.7(b).

Figure 2.7 Transverse relaxation; (a) protons precessing out of phase; (b) random transverse components.

The transverse relaxation process is described by the equation

$$M_{xy} = M_0 e^{-t/T_2} \quad (3)$$

where T_2 is called the transverse relaxation time constant. T_2 is sensitive to perturbing magnetic fields and if B_0 is not homogeneous then a new term T_2^* is used to describe the decay rate of the FID, this is different from the actual T_2 of a material. A more accurate method of determining the value of T_2 will be explained later.

2.1.3. The Spin Echo and CPMG experiments

Apart from the FID, another signal that can be produced is an echo. After the application of the 90° RF pulse, a short time later another RF pulse is applied to flip the magnetization components by 180° , known as a 180° pulse. This is known as the Hahn-spin echo experiment [19], Figure 2.8.

Figure 2.8 Spin Echo experiment, the RF pulse sequence and the NMR signals (Top). Dephasing and rephasing of the magnetization (bottom).

The 90° pulse tips the magnetization into the x-y plane, as the spin precess some protons are getting out of phase (dephasing), the 180° pulse flips the magnetization and causes the protons to refocus (rephasing) and induce an echo signal in the receiver coil. After reaching a maximum the protons will start dephasing again.

After the formation of the first echo the protons start to dephase again, one can apply another 180° pulse to force another echo to be formed and this can be repeated to get a series of echoes, known as an echo train. This method is known as the Carr-Purcell-Meiboom-Gill (CPMG) sequence [20, 21], Figure 2.9. The CPMG method provides a one shot measurement of T_2 parameters and is commonly used in situations with inhomogeneous magnetic fields.

Figure 2.9 CPMG spin-echo formations with T_2 decay curve (red line), the CPMG pulse sequence is shown on top.

T_2 is an important parameter in NMR measurements. It is directly related to the molecular environment. In inhomogeneous magnetic field, CPMG produces an echo train made up with the summation of direct Hahn echoes and indirect stimulated echoes. This echo train decays with an effective relaxation time known as T_{2eff} , it is slightly greater than T_2 . Analyses of T_{2eff} data from rock core and soil samples provide information about their porosity, saturation, pore size and permeability [22]. T_{2eff} relaxation data from polymer products such as PE pipes and car tyres is related to the molecular linking and can be used to determine the quality and aging of the materials [23,24].

2.2. NMR Hardware

2.2.1. Introduction to NMR Systems

A full NMR system can be broadly divided into three parts, a computer, a spectrometer, and a sensor as illustrated in Figure 2.10. The purpose of the computer is to provide the user interface to the spectrometer, controlling all the operations and processing the NMR data. The spectrometer consists of a transmitter for RF pulse generation, often having an amplifier to provide higher power signals; and a receiver for capturing RF signals from the probe. The sensor part is made up of a magnet system with RF coils [25]. For imaging systems, a gradient unit is also present together with gradient coils in the sensor.

Figure 2.10 Block diagram of a NMR system.

NMR systems come in many shapes and sizes depending on their primary usage. One of the biggest NMR systems is the medical Magnetic Resonance Imaging (MRI) scanner used in hospitals. MRI is similar to NMR but uses additional magnetic field gradient coils to determine spatial information. MRI is particularly good for detecting brain tumours and other soft tissue injuries as it provides images with better contrast to that of X-ray images. The contrast in MRI is generated by differences in spin density and relaxation and does not require absolutely homogeneous magnetic fields. A full body size scanner capable of creating a 3D image of the inside of a human body is shown in Figure 2.11.

One of the most common types of laboratory based NMR system is the vertically orientated superconducting magnet that provides the strong, stable and very homogeneous fields that are necessary for high resolution spectroscopy. An example is shown in Figure 2.12 with the magnet and the supporting electronics console. High resolution NMR spectroscopy has made a major impact in the field of chemistry [26,27,28], and it is a very important tool for studying the chemical structures of proteins and other molecules.

Figure 2.11 A full body MRI scanner, Toshiba - Vantage Titan 3T [29].

Figure 2.12 A Superconducting magnet NMR system, Bruker. Left is the magnet system and right is the electronics console, both are taller than a metre [30].

2.2.2. Bench top NMR Systems

Bench top NMR systems are available commercially from many manufacturers, some examples of relatively inhomogeneous systems that measure T_2 are the KEA and Rock Core Analyzer (RCA) system by Magritek [31], Figure 2.13, and the MQC analyzer by Oxford

Instruments [32], Figure 2.14. High resolution Bench top NMR systems such as the high field Spinsolve by Magritek have also recently become available, Figure 2.15.

Figure 2.13 RCA system

Figure 2.14 MQC system

Figure 2.15 Spinsolve systems

Bench top systems are mainly used in chemistry labs and have a wide range of applications, such as monitoring chemical reactions, detecting porosity and therefore potential oil content of rock core samples, etc. The MQC system has a built-in computer system for data analysis. The RCA is a 2 MHz NMR system that determines the porosity and pore size distribution of rock core samples by measuring the T_2 values. The main components in this system are the 2 MHz magnet probe, KEA spectrometer and a magnet temperature controller. The rack mounted version of the RCA system can also do diffusion measurements, with the addition of an external high power gradient amplifier.

A summary of the bench top systems available from some of the well known manufacturers is shown in Table 2.1.

Table 2.1 Summary of bench top systems from well known manufacturers.

System	Manufacturer	Description
Minispec, FOURIER x,	Bruker	Using cryogen-free, permanent magnet technology for standard lab benches. Running the standard NMR software TopSpin™ and offering both 1D and 2D NMR capabilities, applications in reaction monitoring, liquid polymers, edible oils, petrochemicals and many other materials.
MagStationLite	Progression	The MagStationLite measures hydrogen, phosphorus, and fluorine using NMR spectrometry with no manual sample preparation required.
Acorn Drop particle analyzer	XIGO Nanotools	Measurement of foam droplet size and distribution. The Acorn Drop does not require sample dilution that is needed with conventional particle sizing techniques such as laser diffraction.
iSpin	SpinCore Technologies	A portable NMR system can serve as a complete system console for Nuclear Magnetic Resonance (NMR) or Nuclear Quadrupolar Resonance (NQR) with spectrometer frequencies from 0 to 100 MHz.

AqualogBenchtopFluorometer	HORIBA Scientific	A bench top fluorometer capable of determining fluorescence Excitation-Emission Matrices (EEMs) and absorbance spectra simultaneously.
Spinsolve,	Magritek	The permanent magnet based low-cost Bench top NMR system for chemistry labs. Spinsolve® can be used for chemistry reaction monitoring.
MQC Analyser	Oxford Instruments	Compact, modular design for Quality Control measurements; upgradeable firmware, and software self-diagnostics to aid servicing. The MQC requires no external PC, a standard Windows™ PC motherboard is built inside, with USB access, Ethernet connection and a hard disc for data storage.
Rock Core Analyzer	Magritek	A 2 MHz permanent magnet based T_2 analyzer for rock core analysis.

2.2.3. Mobile NMR System and Requirements

The sensor or probe is an integral part of the NMR system. The size of the sensor directly affects the overall size of the complete system and its portability. The Bench top systems listed earlier all required samples to be prepared and put inside the sensor to be examined. This is not ideal as not all samples can be put inside the sensor, such as car tires and cultural heritage paintings. To have a truly portable system, the sensor has to be small. For on-site measurements, the sensor needs to come to the sample instead of preparing a sample to bring to the sensor. One truly portable sensor that fits all those requirements is the Mobile Universal Surface Explorer (MOUSE) developed by a group in Aachen University of Technology, RWTH [33,34].

The MOUSE sensor was initially developed for analysing the rubber of car tyres, but has since been used in various applications such as detecting moisture contents in historic documents and buildings; quality control of elastomers and polymer materials [35,36,37]. It is based on the principles of “inside-out” NMR where the region of interest is outside the sensor. The MOUSE is a surface sensor that can only be used to obtain data from samples that are located within a few millimetres of the sensor surface. The object to be examined should only be placed close to the surface of the sensor, therefore it is not necessary to prepare a sample and there is no limit on the maximum size of the object being tested.

A schematic view of the construction of the MOUSE is shown in Figure 2.16. Two rectangular permanent magnets line up in opposite direction and are placed on top of an iron yoke. A solenoid surface coil is used to interact with samples on the surface. A picture of a newly developed Mini-MOUSE is shown in Figure 2.17. This Mini-MOUSE sensor typically resonates at 17 MHz, uses an excitation power level of 30 Watts RMS, a 90° pulse time of 4 μ s and produces a Spin Echo signal with an amplitude of approximately 5 μ V and duration of 10 μ s.

Figure 2.16 NMR-MOUSE construction using permanent magnets [32]

Figure 2.17 Hand held 17MHz Mini-MOUSE, 70x50x50 mm [38]

Figure 2.18 Hand held 20 MHz NMR MOUSE [33]

An alternative construction of the MOUSE is the single cylindrical bar magnet mouse shown in Figure 2.18, also produced by the same group in RWTH. Here a B1 coil is placed directly on the surface of a magnet. Again only samples within a few millimetres from the surface can be measured. The MOUSE sensor typically resonates at 20 MHz, uses an excitation power level of 100 Watts RMS, a 90° pulse time of 4 μ s and produces a Spin Echo signal with an amplitude of under 10 μ V and duration of 10 μ s.

The NMR systems mentioned in section 2.2.2 before are bench top systems. This is mainly due to the size of the instrument and the power supply needed to run the instrument. There might be very different definitions of a mobile system; in this report it refers to a system that can be hand carried and operated at the same time. The smallest mobile NMR system in the market today is the LapSpec produced by Magritek, Figure 2.19. It uses a NMR MOUSE sensor to examine properties of plastic pipes, rubbers, etc.

Figure 2.19 LapSpec Mobile NMR Spectrometer by Magritek

While the LapSpec system is good in size for its mobility, there are some drawbacks in the hardware. As all mobile devices do, they use battery to run; the RF transmitter in the LapSpec uses a Class A amplifier for generating the high power RF pulses. The output of the amplifier can produce pulses of 100 Watt RMS power but it has an efficiency of only 25%, which is not ideal for battery powered devices. The LapSpec is also based on early DSP and FPGA technologies so the system is rather bulky. It weighs 3.6 kg and runs for up to 4 hours on rechargeable batteries. A computer is needed to run the LapSpec system software.

Chapter 3. Class D RF Amplifiers for Mobile NMR Applications

This chapter first gives some background information on the operations of Class D amplifiers. Starting with the basic switching circuit then followed by more advanced switching techniques to produce pulse width controlled amplifiers. The switching characteristics of MOSFET and gate drivers are also discussed. Then the development of some Class D amplifiers working at 2 MHz is presented and the test results shown.

3.1. Class D Amplifier Theory

Class D amplifiers convert the input signal to a sequence of higher voltage pulses first, and then reconstruct a smoother sinewave signal using a passive filter on the output. The main advantage of a Class D amplifier is power efficiency. Because the switching transistors (usually MOSFETs, more details given in the next section) are switched either completely on or completely off, power dissipation is low as MOSFETs have very low on-resistances, $R_{DS(on)}$. Class D amplifiers can achieve efficiencies of 80% or higher. More detail on the operation of the Class D amplifier is given next.

3.1.1. The Basic Class D Amplifier Circuit

A simplified Class D circuit with a tuned network output is shown in Figure 3.1. It shows the basic structure of Class D amplifiers. There are two transistors or MOSFET switches, the one on the top, Q1, usually referred to as the "high side", and the other, Q2, referred to as the "low side". The outputs from the two switches are driving a tank network; the load is part of this network. This tank network converts the rectangular voltage pulses to a smooth sine wave output.

Figure 3.1 Simplified Class D circuit

The figure shown is a voltage switching amplifier where the tuned circuit LCR elements are in series. In the case of a current switching amplifier, the LCR elements are connected in parallel. The operation of both voltage switching and current switching Class D circuit is the same, the difference being in the current source supply and the type of tuned circuit in the output [39,40,41]. In practice, the voltage switching type is preferred due to the lower current rating requirements of the MOSFETs, as high voltage MOSFETs are readily available in the market. There is also a report that the voltage switching type has a slightly higher efficiency at high power when operating at high frequency [42]. The voltage switching amplifier will be the focus of this research.

3.1.2. Class D Amplifier Operations

The general operation of the voltage switching Class D amplifier is explained with reference to Figures 3.2 and 3.3, showing the voltages and currents at different parts of the circuit. The gate driving signals V_{GS1} and V_{GS2} have 50% duty cycle and are out of phase, so that the two MOSFETs are always in opposite states.

When V_{GS1} is high, Q1 is on, at the same time V_{GS2} is low and Q2 is off, the switching node connects the LCR tuned circuit to the power supply V_d via Q1, and current starts to flow. This gives the positive half cycle at the output. When V_{GS2} is high and V_{GS1} low, Q2 is on and Q1 is off, the switching node connects the LCR tune circuit to the ground via Q2, and current starts to flow. This gives the negative half cycle at the output. The operation waveforms are shown in Figure 3.3.

Figure 3.2 Class D circuit operation

Figure 3.3 Operation waveforms of a Class D Amplifier.

It is very important that the two MOSFETs are on only one at a time. If both of them are on at the same time, the power supply will be shorted to ground through the MOSFETs, resulting in very high current flow in the devices and damage. This is known as Shoot Through. To avoid this and protect the devices from damage, a small delay is used between the switching off time of Q1 and the switching on time Q2, to make sure that Q1 is totally off before Q2 is turned on. Similarly in the other operating cycle, make sure that Q2 is totally off before Q1 is turned on. This delay time is referred to as the “dead-time” as illustrated in Figure 3.4. The dead-time has direct impact on the efficiency of the amplifier, it is to be well adjusted to be as short as possible but avoiding shoot through [40,43].

Figure 3.4 Dead time of Class D circuit

3.1.3. Transformer Coupled Voltage Switching Class D Amplifier

A variation of the Class D circuit is having a transformer at the output. This type of transformer coupled Class D amplifier has the advantage of higher power output from the same power supply voltage. This is achieved through the use of a step up transformer with turn's ratio "m" as shown in Figure 3.5.

Figure 3.5 Transformer Coupled Voltage Switching Class D Amplifier

The switching operation of this amplifier is the same as the basic Class D, the higher output power from the same power supply means that the currents flowing in the MOSFETs are higher, therefore the devices require higher power ratings.

3.1.4. Pulse Width Modulated Class D Amplifier

The PWM Class D amplifier is a broadband amplifier. It uses a low pass filter on the output instead of a tuned circuit to reproduce a sine wave. The gate control signals are also variable width compared to the fixed 50% duty cycle of the basic Class D circuit. This method is commonly used in high power and high efficiency audio amplifier designs. The operation of PWM Class D can be explained using an audio amplifier as an example [44,45,46]. A block diagram of this operation process is shown in Figure 3.6.

Figure 3.6 Operations of Class D audio amplifier (waveform drawings are not to scale)

Starting with an assumption that the input audio signal is a standard sinusoidal signal, this signal is compared with a high frequency triangle or saw-tooth waveform to create the PWM signal for switching the MOSFETs. The output of the comparator goes high when the sine wave is higher than the saw-tooth waveform. This PWM signal is then used to drive the power stage, creating the amplified digital signal, and finally a low pass filter is applied to the signal to filter out the PWM carrier and reproduce the sinusoidal audio signal. The LPF for audio amplifier is a broadband filter because the audio signals are at different frequencies.

The PWM Class D method not only works for audio frequency signals, reports of this method working for 500 KHz signals has been published [47]. However, it is a modulation of a single pulse for every half cycle, therefore a tuned circuit on the output is still needed, resulting in a narrowband amplifier.

3.1.5. PWM Using Delta-Sigma and Single Cycle Controls

The PWM signal generation method described in the previous section works fine in audio amplifiers. The same method does not work for some high precision applications because there is no feedback from the output for controlling the PWM signal. The PWM signal is generated by the input and the reference signal, regardless of what happens to the amplifier output. Amplifiers of this type does not have good linearity performance.

Another way of generating a PWM signal from an analogue input is Delta Sigma Modulation [48,49,50,51]. This method has been successfully used in audio amplifiers [52,53]. Figure 3.7 shows a block diagram of a first order Delta Sigma Modulator.

Figure 3.7 First Order Delta Sigma Modulator

The main components in this first order circuit are the Integrator, comparator and data latch. The difference between the input and the feedback signal is first integrated, then compared to a reference signal, usually ground. The output from the comparator is then latched to the output by a clock. The output goes high on the high cycle of the clock whenever the comparator output is high. The output waveforms at different stages of the circuit are shown in Figure 3.8 [54]. The PWM output can be used as switching logic signals to control the MOSFET switches in power converters or Class D amplifiers.

Figure 3.8 Waveforms of a 1st Order Delta Sigma Modulator [54]

From the operation principles of the Delta Sigma Modulator, researchers have come up with the Single Cycle Control method for use in power converters [55,56,57]. The Single Cycle Controller is very similar to the Delta Sigma Modulator. It also has an integrator, a comparator and a clock controlled SR latch. The general layout of a Single Cycle Control circuit is shown in Figure 3.9.

Figure 3.9 General layout of a Single Cycle Control circuit

The operation of the circuit is as follows. When there is a "high" signal from the SR latch, the switch is turned on, the integrator output starts to ramp up, this output is compared with the control reference in real time. Once the integrator output reaches the reference level, the comparator output goes high and triggers the RS latch to output a "low" signal to the switch, and the switch changes state to off; at the same time the integrator resets to zero for the next cycle. It is very clear that the Integrator is the heart of the system.

3.1.6. Unipolar and Bipolar Switching Systems

There are two types of PWM switching systems - unipolar and bipolar. Unipolar systems switch between the positive DC voltage to ground, and negative DC voltage to ground. An output waveform from such a system is as shown in Figure 3.10. They are referred to as unipolar because of the single common reference.

Figure 3.10 Unipolar PWM waveform.

Figure 3.11 Bipolar PWM waveform.

Bipolar systems switch only between the positive and negative DC voltages; an output from such a system is shown in Figure 3.11. In either of those switching systems, a low pass filter is needed at the output to recover the sinusoidal signal. In a half-bridge switching system, only one MOSFET is switching to produce the half cycle of the sinewave. In the bipolar system both MOSFETs have to be switching. This is one of the advantages of a unipolar system.

3.1.7. Proposed PWM Class D Circuit

As explained earlier, the heart of the Delta Sigma Modulator circuit and the Single Cycle Controller circuit is the integrator. Usually high precision components such as OpAmps and high stability capacitors are needed for this part of the circuit. The following section proposes a simplified PWM method for a class D amplifier that does not use the OpAmp integrator circuit, but still operates on the same principles of Delta Sigma and Single Cycle methods.

A block diagram of the proposed PWM Class D circuit is shown in Figure 3.12. The logic circuit for controlling the gate drivers to each of the MOSFETs are very similar, consisting of a comparator and a D Flip Flop operating at a chosen frequency. The unipolar PWM method is used in this circuit because this way only one power MOSFET is switched at a time on each half cycle. This minimises the switching losses compared to the use of a bipolar switching method, because both power MOSFETs need to be switched for bipolar. There is a "cycle selection and dead time control" function block in the circuit. The purpose is to make sure the correct half cycles are used for generating the PWM signals for driving the MOSFETs. It also provides control for the dead time. During the positive half cycle, only the top half of the circuit is operational, which means Q2 is off. Similarly only the bottom half of the circuit is operational during the negative cycle and Q1 is off. A feedback signal is formed by integrating the PWM signals from the output of the two D flip flops. A simple LC low pass filter can be used instead of an OpAmp integrator.

Figure 3.12 Block diagram of a proposed PWM Class D circuit and operation waveforms. Cycle selection signals are shown pink, the input signal is black, blue is the feedback signal and green is the Q output of the flip flop.

The circuit operates as follows. On the positive half cycle of the input, assuming the feedback signal (blue) is lower than the input (black), then the comparator output is high and this feeds into the Data port of the D flip flop. On the rising edges of the clock, the "high" data bit is transferred to the Q output (green) and stays "high" for the duration of the clock; this switches the Q1 MOSFET on, resulting in a high power output from the LC filter network. If the output is high enough and the feedback signal is higher than the input, then the comparator output is low, the Q output of the D flip flop also stays low and Q1 turns off and no more power is delivered to the output. This process repeats until the negative cycle of the input comes. The same operation happens on the negative cycle of the input for the bottom half of the circuit, the only difference is the two inputs to the comparator have been swapped due to the negative polarity of the signals. Physical construction of this circuit and test results are shown in the later sections of this report.

Component selection is very important for achieving high efficiency in amplifier design. The two major components in a Class D circuit are the MOSFETs and their gate drivers. The next section will discuss those in more details.

3.2. Power MOSFETs

Power MOSFETs are divided into two categories, enhancement-mode and depletion-mode. Each category is then sub-divided into two types; N-channel and P-channel [40,58]. N-channel MOSFETs are commonly used in electronic switching devices due to the lower on resistances compared to P-channel MOSFETs. Lower on resistances results in lower power losses and higher output efficiency. The main difference between depletion-mode and enhancement-mode is that enhancement-mode MOSFET turns off at 0 V Gate-Source voltage (V_{gs}) but depletion-mode stays on and requires a negative V_{gs} to turn off. The negative V_{gs} requirement of depletion-mode devices makes the gate driving circuit very complex and has led to N-channel enhancement-mode MOSFETs becoming more popular for circuit designers to use. Figure 3.13 shows the physical structure of an N-channel enhancement-mode MOSFET and the equivalent circuit symbol. Note that the Gate metal contact is on top of the SiO_2 layer and there is no direct connection to the n or p materials, hence the high input impedance on the Gate.

Figure 3.13 N-channel MOSFET and circuit symbol.

MOSFET is a voltage controlled device. When a gate voltage, V_{gs} , is applied to the Gate terminal and is higher than the gate threshold voltage, $V_{gs(Th)}$, a conduction channel is formed under the SiO_2 layer between the Drain and the Source terminals. That is the on state of the MOSFET. If V_{gs} is less than $V_{gs(Th)}$ then there is no conduction path formed and the device is in the off state. The p-type material on the body of device forms a p-n junction with the n-type material on the Drain, it is called the “body diode” and it functions exactly like a normal diode with reverse recovery characteristics [58].

The dynamic switching behaviour of a MOSFET is affected by the parasitic capacitance between the terminals. They are the gate-to-source capacitance, C_{gs} , gate-to-drain capacitance, C_{gd} , and drain-to-source capacitance, C_{ds} , as shown in Figure 3.14.

Figure 3.14 The parasitic capacitances [58].

Manufacturer datasheets normally give three parameters that are related to the parasitic capacitances. They are the small-signal input capacitance, C_{iss} , small-signal output capacitance, C_{oss} , and small-signal reverse transfer capacitance, C_{rss} . They are related to the three parasitic capacitance parameters via the following equations [38]:

$$C_{gd} = C_{rss} \quad (4)$$

$$C_{gs} = C_{iss} - C_{rss} \quad (5)$$

$$C_{ds} = C_{oss} - C_{rss} \quad (6)$$

To turn the MOSFET on, C_{gs} and C_{gd} must be charged and similarly they must be discharged at turn off. That is the function of a gate driver. The lower the values of C_{gs} and C_{gd} the faster the MOSFET can be switched on and off. Another parameter related to the switching speed and given in datasheets is the gate charge, Q_g . It is the amount of charge that is required during turn on and to be removed during turn off at the gate terminal, again those are the functions of the gate driver.

While those capacitance parameters can affect the switching time, the actual switching time parameters of a device is usually given in the manufacturer datasheets. Those parameters are often the deciding factors in choosing a device. The parameters are: rise time, t_r , falling time, t_f , turn-on time delay, t_{D_on} , turn-off time delay, t_{D_off} , and body diode reverse recovery time, t_{rr} . The switching times are illustrated in Figure 3.15 for a typical pulse input. For fast switching MOSFETs that are operating in the MHz frequency ranges, those parameters are defined in nano-seconds.

In response to a gate driving pulse input (top), output “high” means the MOSFET is turned on, however this happens only after a time delay, t_{D_on} . The state transition from off to on also takes a finite time, t_r . Similarly at turn off, this happens after a delay of t_{D_off} , and the process takes a time of t_f .

Figure 3.15 Switching diagram showing all the timing parameters

A MOSFET also has a breakdown voltage level which limits the maximum voltage across the Drain and Source. The current handling capability is also an important factor on selecting a device. Table 3.1 shows a selection of some of the fastest switching MOSFETs available in the market with their relevant parameters. An ideal MOSFET would have the lowest parameter values for parasitic capacitances, gate charge, diode recovery time, and equal timing parameters for the rising and falling edges of the pulse with similar propagation delays, i.e. a symmetrical pulse. With the selection criteria of small footprint, fast switching and capable of handling 100 W of power from a 24 V power supply, the most suitable device is the CSD17313Q2. This device has low gate capacitance (260 pF) and charge (2.1 nC), high pulsed drain current (20 A) and a switching time of 4 ns with delay time of under 4 ns. The maximum Drain-Source voltage is 30 V. The reverse recovery time of the body diode is under 13 ns. The size of the device is 2x2 mm. The maximum gate drive voltage can be up to 10 V.

Table 3.1 Selection of high speed switching power MOSFETs

Parameters MOSFETs	Tr (ns)	Tf (ns)	Td_on (ns)	Td_off (ns)	Trr (ns)	Id_ct. (A)	Id_pl (A)	Vds (V)	Ciss (pF)	Coss (pF)	Crss (pF)	Qg (nC)	Vgs (V)	Vgs_th (V)	Rds_on (ohm)	Package/ Footprint
BSP030	10	20	8	24	120	10	40	30	770	265	180	24	+20 / -20	2	0.03	SOT223
CSD17313Q2	2.8	1.3	3.9	4.2	12.9	5	20	30	260	140	13	2.1	+10 / -8	1.3	0.024	SON2x2
CSD17507Q5	5.2	2.3	4.7	5.7	16	13	85	30	410	270	23	2.8	+20 / -20	1.6	0.009	SON5x6
DE275-201N25A	5	8	5	8	300	25	150	200	2500	265	42	81	+20 / -20	3	0.13	DE275
FDD6612A	5	4	9	24	20	10	60	30	660	170	90	6.7	+20 / -20	2	0.02	TO-252
RFD14N05	26	17	14	45	125	14	55	50	570	185	50	25	+20 / -20	2	0.1	TO-252
SI4128DY	12	10	15	13	15	4	30	30	435	95	42	3.8	+20 / -20	2.5	0.03	SO-8
SUD06N10-225L	8	9	8	8	35	6.5	8	100	240	42	17	2.7	+20 / -20	1	0.2	TO-252
ZXMN4A06K	3.8	10.9	3.2	23.3	16	10	35.3	40	827	133	84	17.1	+20 / -20	1	0.05	TO-252

Table 3.2 Selection of high speed gate driver ICs (Parameters given for driving 1nF load or under)

Parameters Driver ICs	Io (A)	Vout (V)	Td_on (ns)	Td_off (ns)	Tr (ns)	Tf (ns)	P.W_min (ns)	Package/ Footprint
AUIRS21915	3.5	10 ~ 20	90	90	15	15	25	SOIC16
DEIC420	20	10 ~ 30	38	35	3	3	8	DE420
ISL55110	3.5	5 ~ 12	12	12	4	4	6	QFN16 / TSSOP8
LM5114	1.3	5 ~ 12	12	12	8	3.2	na	SOT23-6 / LLP6
TPS28225D	4	4.5 ~ 8.8	14	14	10	10	30	SOIC8 / DFN8
ZXGD3002E6	9	10 ~ 20	1.25	1.6	8.3	10.8	na	SOT23-6

3.3. Gate Driver

A gate driver is a very important part of the Class D circuit. An efficient gate driver can switch the output MOSFETs on and off quickly, greatly reducing the switching losses in them. For that, the driver needs to charge and discharge the gate and parasitic capacitors of the MOSFET quickly, which means that the driver has to supply high current pulses to the gate at the operating frequency. A gate driver IC is a device that can be connected directly to the Gate of a MOSFET and controls the switching by a logic level input. Using a driver IC will simplify a design and use fewer components. There are many gate driver IC devices available in the market. In practice, a driver IC is chosen according to the switching speed, output voltage and current as required by the MOSFET device. A gate driver IC has the same timing parameters as a MOSFET in response to a control logic input. Table 3.2 lists some of the suitable gate driver ICs available in the market.

While the MOSFET is a voltage controlled device, the gate driver still needs to supply enough output current at the gate voltage level to charge and discharge the gate and parasitic capacitances. This output current requirement is estimated from the device datasheet using equations 7 and 8:

$$i = C \frac{dV}{dt} \quad \text{and} \quad (7)$$

$$Q = CV \quad (8)$$

where i is current (A);

C is capacitance (F);

Q is charge (C);

V is gate voltage (V).

From the datasheet for the MOSFET CSD17313Q2, $Q_g=2.25$ nC with gate voltage of 5 V, the gate capacitance is calculated to be 0.45 nF. The current value is frequency dependent as it is determined by the $\frac{dV}{dt}$ term. The higher the switching frequency the higher the current needed. The datasheet gives the turn-on rise time of the CSD17313Q2 as 2.8 ns and the turn-off fall time as 1.3 ns. The gate driver has to supply enough current and the shorter turn-off

time of 1.3 ns is use in here for the current calculation. For a gate drive voltage of 5 V to switch within 1.3 ns, the required current is:

$$i = C \frac{dV}{dt} = (0.45 * 10^{-9}) * \frac{5}{1.3 * 10^{-9}} = 1.73 \text{ A.}$$

Looking back at Table 3.2, most of the gate driver ICs listed can be used to drive the CSD17313Q2 MOSFET, apart from LM5114 which has an output current of 1.3 A. Another parameter to check on choosing the driver IC is the “minimum pulse width”. It is the shortest output pulse the driver IC can produce; any input that is shorter than this length will not enable an output from the driver. The next step is to check this requirement against the CSD17313Q2 MOSFET operating at 20 MHz.

Using the timing parameters from the datasheet and Figure 3.15 as a reference, a more detailed timing diagram for two MOSFETs in a Class D setup is produced and shown in Figure 3.16. The dead-time needed for the Class D setup is the body diode recovery time, t_{rr} , in the diagram.

Figure 3.16 Timing diagram of Class D setup with two MOSFETs, time unit in ns.

The period of a 20 MHz signal is 50 ns and therefore each half cycle is 25ns. The total length of the fixed timing parameter on each half cycle is $(t_r + t_f + t_{rr}) = 17$ ns. This leaves the useful portion of the output signal as 8 ns. Minus the timing due to asymmetric on and off

delays, $(4.2-3.9)=0.3$ ns, the minimum pulse length is therefore 7.7 ns. Checking with values on Table 3.2, the only gate driver IC that can have a pulse length of fewer than 7.7 ns is ISL55110 with a minimum pulse length of 6 ns. Note that this analysis used the maximum diode recovery time t_{rr} of 12.9 ns. In a high frequency switching setup, the on time of the device is short and t_{rr} will be shorter due to the reduced charge on the body diode, therefore it is possible to operate the MOSFET at higher than 20 MHz with a shorter dead-time using the same gate driver IC. For this project that operation is not required.

The physical size of the chosen MOSFET and gate driver IC are small, 2x2 mm and 3x6.4 mm respectively, ideal for compact and small size design and will be used in this project. A test board was made to test the switching speeds of the gate driver IC and MOSFET combination in a Class D setup. A schematic capture showing the driver ICs and the output MOSFETs is shown in Figure 3.17.

Figure 3.17 Part of a test circuit for the Gate driver IC and MOSFET combination. S1 and S2 are the switching logic signals, U14 and U15 are the driver ICs and Q1 and Q2 are the MOSFETs.

A pair of 20 MHz pulse logic signals from a Tektronix AFG3102 signal generator were used as inputs to the driver ICs. The dead-time between the half cycles was set to 13 ns. A screen capture is shown in Figure 3.18. The driver IC has an output range of 5 V to 12 V. The

device was first tested on the 5 V output. This was done by using a 5 V supply on the VH pin. The corresponding driver output signals on the gates of the MOSFETs were measured and shown in Figure 3.19. The turn-off delay is clearly shown as the dead-time is now less than 13 ns, approximately 10 ns.

Figure 3.18 A pair of 20 MHz logic signals used as driver input

Figure 3.19 Gate driver outputs at 20 MHz

The driver IC at higher output voltage was also tested. While the driver is capable of up to 12 V output, the MOSFET gate has a maximum rating of only 10 V. A 9 V supply was used for testing as it is just under the maximum rating of the device. The same pair of logic signals were used and the corresponding driver outputs are shown in Figure 3.20.

Figure 3.20 Gate driver logic and outputs at 20 MHz. (blue and orange are gate logic signals, green and purple are corresponding driver outputs on the MOSFET gates).

One observation on Figure 3.20 is the gate driver output signals (green and purple) are not square shape, which is due to the effect of the MOSFET gate capacitance. Higher gate drive voltage can result in more gate charges therefore increased the turn-on and turn-off times. However it is clear that the driver output is matching the logic input which means the devices are capable of operating up to 20 MHz. The 5 V driver output is preferred because it has better turn-on and turn-off time and is well within the maximum rating of the MOSFET gate voltage.

3.4. Development of Class D RF Amplifiers for 2 MHz Operation

This section describes the developments of three types of Class D amplifiers that are suitable for mobile NMR applications. To be able to test each design, they were all designed to work at 2 MHz and tested using the Rock Core Analyzer system. Some specifications for the Class D amplifier design is shown in Table 3.3.

Table 3.3 Specifications for the Class D amplifiers.

Performance Parameters	Values
Operating frequency	2 MHz
Power (RMS) into 50 ohm load	100 W
Rise and ring down times	< 3 μ s
Efficiency	> 80%

3.4.1. The Amplifier Control Lines

NMR spectrometers normally provide some form of control lines for operating the RF amplifiers, either as TTL lines or RF signals. For the KEA spectrometer in the RCA system, there are two programmable TTL lines. All of the 2MHz Class D amplifiers in this project were designed to use those TTL lines as control signals. The KEA spectrometer uses Euro card size (160x100 mm) PCB modules, therefore the new amplifiers were laid out on Euro card size PCBs so they can be plugged into the spectrometer for testing.

Operation of the KEA spectrometer is controlled by a computer program, Prospa [59]. Pulse sequence information such as pulse lengths and amplitudes for the 90 and 180 degrees pulses can be user defined and sent to the KEA via a USB interface. Custom TTL logic lines are also available to the user. The control logic lines and the RF pulses used on a CPMG sequence are shown in Figure 3.21.

Figure 3.21 The Logic lines and RF pulses of a CPMG sequence

Those are the control signals needed for operating the existing Class A amplifier. The Class D amplifier will be using the same. There are two logic lines named “Gate” and “TTL” on the KEA system. The TTL signal turns on the amplifier for the whole duration of the pulse sequence, the Gate signal only turns on to enable the RF input to the amplifier. The pulse sequence can be created using the Pulse Programmer in Prospa.

Knowing the control signals to use for the RF amplifier, the next step is to build the prototype for testing. The transformer coupled Class D circuit as described in Section 3.1.3 earlier was built first.

3.4.2. Class D RF Amplifier with Constant Amplitude Output

The first amplifier built was a basic transformer coupled Class D amplifier operating at 2 MHz as illustrated earlier in Figure 3.5. While the block diagram of this amplifier looks simple and easy to understand, the actual design of the amplifier is a lot more complex as the complete circuit in Appendix I shows.

The first task in the design was to generate two gate driver signals from the input RF signal. The idea here is to have two separate logic signals with opposite phases to control the driver ICs that are driving the two MOSFETs. This was done by using comparator circuits, the principle of which is explained using Figure 3.22 below.

Figure 3.22 Gate driver control signals and Dead-time control

Comparing the positive cycle of the input RF to a positive reference voltage level, any parts of the input RF that is greater than the reference would generate an output and can be used to control the positive side of the gate driver. Similarly, comparing the negative cycle of the input RF to a negative reference voltage would generate a control signal for the negative side of the gate driver. On using a fixed amplitude input RF, the dead-time between the positive and negative cycles can be controlled or set by the magnitude of the two reference signals. A high magnitude reference results in a longer dead-time and a lower magnitude would reduce the dead-time.

The input RF signal coming from the Transceiver of the KEA is a 0 dBm sinusoidal signal, which is equivalent to a 1.5 V_{p-p} signal in terms of voltage. Since the input signal is going to the input of a comparator, an OPA695 amplifier circuit (Figure 3.23) with a gain of 15 dB is used to boost the input to a higher voltage level. This reduces the chance of chatter while crossing through threshold. Amplifying the magnitude of the input RF also speeds up its rise time and improves the response time on the input of the comparator.

Figure 3.23 OPA695 Amplifier circuit for the input RF

The comparator circuit for the positive cycle is shown in Figure 3.24. The same circuit was used also on the negative cycle but with the two inputs swapped and a negative reference voltage. The comparator used is the LT1715 manufactured by Linear Technology. It is a dual comparator setup in a small MSOP package. It operates up to 150 MHz and has a response time of 4 ns, which is a lot faster than what is needed. The reference voltage was set to 0.25 V.

Figure 3.24 Comparator circuit for the positive cycle

With the prototype board built, some circuit measurements were made to check the logic control parts of the design. A 2 MHz, 0 dBm signal was sent to the input of the amplifier from the KEA transceiver output, the output of the OPA695 circuit was measured together with the two outputs from the comparators. A screen shot is shown in Figure 3.25.

Figure 3.25 OPA695 output (blue) and comparator outputs, positive cycle (cyan) and negative cycle (pink).

Figure 3.26 Dead-time of 16 ns between the two cycles (cyan and pink)

The OPA695 output (Blue trace) has a peak to peak value of close to 8 V, which agrees with the design of 15 dB gain from the OPA695 circuit. The positive cycle output (Cyan) and the negative cycle output (Pink) are all as intended. A closer look at the dead-time is 16 ns as shown in Figure 3.26. This is acceptable as it is slightly longer than the reverse recovery time of 13 ns for the MOSFETs.

The power supply for the output stage is heavily filtered. Low ESR capacitors were used in parallel to provide a good bypass path. Apart from the many bypass capacitors, an RF Choke was also used in series to stop the switching noise from entering the power supply. The RF Choke was constructed from a T105-15 toroid, 27 turns are need for a value of 25uH. This choke will provide enough DC output current and enough impedance (314 ohm at 2 MHz) to block any feedback of 2 MHz noise into the supply line. Using 24V DC supply on the output stage should provide output powers of 100 W, the transformer ratio is calculated to be close to 1:4. This step up transformer will transfer the load impedance of the output LCR network (50 ohms) to about 3 ohms on the MOSFET side. Designing with a Q of 5 and an operating frequency of 2 MHz, the calculated values for the output tank components, L is 20 μ H, and C is 320 pF. The inductor L is constructed using T106-2 material, winding a total of 39 turns. The toroid material is chosen based on the frequency response curve and power rating data supplied by the manufacturer, Amidon [60].

The step up transformer was made with 1:4 ratio using BN-61-002 material. Using this transformer in the circuit, the outputs were measured and are shown in Figure 3.27. The orange waveform is the gate drive pulse for the negative side MOSFET and the blue is the amplifier output into a 50 ohm load. Output power is 104 Watt RMS and efficiency of 90%.

Figure 3.27 Amplifier output (blue) into a 50 ohm load with the gate drive signal shown on top (orange)

The rise time and ring down performances are very important aspects of the amplifier especially when used in NMR systems. Long rise time or long ring down times would limit the amplifier from producing narrow pulses. A 5 μ s pulse output from the amplifier is shown in Figure 3.28. The rise time is under 1 μ s and the ring down time is approximately 3 μ s. Those times are acceptable for the RCA system.

Figure 3.28 Output of a 100 W, 5 μ s pulse on a 50 ohm load (green), orange is the gate control logic signal

Figure 3.29 Output of 20 μ s pulses at 20% duty cycle

Output stability of the amplifier was tested by producing long duration and high duty cycle pulses repeatedly. The continuous output of 20 μs pulses at 20% duty cycle is shown in Figure 3.29. The constant amplitudes suggested that the amplifier is very stable.

To use the new amplifier inside the KEA spectrometer and to do NMR measurements, the controlling pulse sequence had to be modified. Note that on the pulse sequence for a Class A amplifier, the amplitude of the 180 degree pulses are double that of the 90 degree pulses. For this Class D amplifier, modulating the amplitude is not possible, therefore the pulse length of the 180 degree pulses was doubled to provide the equivalent RF power as illustrated in Figure 3.30.

Figure 3.30 CPMG pulse sequence for Class D amplifier

The test sample used in the RCA was a water sample. Based on existing experiment parameters from a Class A amplifier on the same sample, the parameters used for the Class D amplifier are shown in Figure 3.31. The CPMG sequence has 64000 echoes and an echo time of 200 μs . The amplitude settings for both 90 and 180 pulses are the same to have the correct output power from the RF amplifier.

Figure 3.31 Prospra parameters of CPMG for Class D amplifier

The same experiments were performed using the Class A amplifier and the results are shown in Figure 3.32. The results were obtained from the average of four phase cycled scans. The T_{2eff} decay is almost the same in both cases but the phase oscillation of the Class D amplifier is clearly visible on the imaginary data set. This oscillation does not affect the decay rate. It is likely due to imperfect RF pulses (variations in amplitude or phase during start and end of the pulses).

Figure 3.32 CPMG results from Class D amplifier (blue) and Class A amplifier (red). There is oscillation on the imaginary data set of the Class D amplifier.

3.4.3. Class D RF Amplifier with Amplitude Modulation

While the constant amplitude version of the Class D amplifier is working, one advantage of having amplitude modulation capability is that it can use the existing pulse sequences in Prospa from the Class A amplifier without modification. Amplitude modulation also allows the amplifier to output different power levels, in practice the amplifier could be driving different types and sizes of sensors or loads that require very specific power levels. The way of achieving amplitude modulation in here is to control the width of the gate controlling pulses using a PWM modulator. A block diagram of the new design is shown in Figure 3.33.

Figure 3.33 Block diagram of a PWM controlled Class D amplifier

A set of width varying gate control signals are used to control the output MOSFETs; this will result in width varying power pulses on the switching node, which in turn changes the amplitude of the output on the load after the low pass filter. Controlling the width of the switching pulse is equivalent to controlling the dead-time of the two cycles. A narrow gate pulse results in a lower output, same as having a longer dead-time. This process is explained using Figure 3.34.

Figure 3.34 Amplitude modulation by varying width of a single pulse.

Using two fixed reference voltages and varying the amplitude of the input RF signal, a simple pulse width modulation can be achieved. On the positive cycle, the more time that

input is greater than the reference, the wider the output pulse width is. Similarly on the negative cycle, the more time that input is beyond the reference level the wider the pulse output is. If the input signal doesn't go beyond the reference voltages, then there will be no pulse output on the comparator. The same circuit on the previous amplifier can be used for this part.

The output stage of the constant amplitude amplifier used a transformer for impedance matching with the load; however that will not work here as the width of the pulses for lower amplitude outputs are much less than the 50% duty cycle needed for transformer operation. A passive LC low pass matching network was used here, that also makes it a broad band output amplifier. Broad band output has a faster response time than the resonant tank narrow band output. The output stage is shown in Figure 3.35.

Figure 3.35 Output stage of amplifier

A very important point about the positive side (also called “high” side) of the circuit is that its reference point is at the output switching node of the amplifier, which is connected to the input end of the filter inductor; therefore the supply voltage to this part of the circuit has to be a floating power supply. This design uses an isolated voltage regulator (MEE3S1209SC) as it is readily available in the market at an affordable price. The control logic part of the circuit also required isolation. A high frequency digital isolator is chosen for this. The ADUM1100BRZ manufactured by Analog Devices, has a 100 MHz bandwidth and isolation voltage of 560 V. This component is also readily available in the market and comes in a small SOIC8 surface mount package. More detail on this part of the circuit can be found in Appendix II.

Apart from the change of output circuit, the power supply has to be a dual polarity supply as the lower side of the circuit needs to generate the negative cycle as there is not a resonant circuit to do so. Since the DC supply to the KEA system is a fixed 24 V DC supply, a power inverter circuit was used to convert the positive DC supply to a negative rail for the lower side. A positive step-down converter was also used to drop the voltage down to a magnitude that matches the negative rail. A schematic of the converters is shown in Figure 3.36. A switch mode regular, LT1074 was used in the design and it was chosen based on its low noise and high efficiency. An output current rating of 5 A is also sufficient for this design. Due to the maximum voltage rating of 30 V for the MOSFETs used, the maximum supply voltage was chosen to be ± 15 V. The two supply rails were also filtered with low ESR capacitors and RF chokes as in the previous amplifier.

Figure 3.36 Power converters for dual polarity supply

A measurement of the output switching node using a maximum magnitude (0 dBm) RF input signal is shown in Figure 3.37. The duty cycle of the two half cycle gate pulses (orange and cyan) are at maximum width of just under 50%. The switching node voltage is changing between +15 V and -15 V as expected (purple). This shows that the MOSFETs are switching in the correct manner and the new circuits are working so far.

Figure 3.37 Gate signals (cyan and orange) and the corresponding output switching node voltage (purple).

When operating in the amplitude modulation mode, the duty cycle of the switching pulses is much less than 50% and the dead-time between them are longer. During that time the output switching node needs to be grounded otherwise it is an open circuit and the back EMF causes the body diodes of the MOSFETs to conduct. This also changes the impedance presented to the output node. This is true for both positive and negative sides. This will negate the modulation effect and result in a constant output. Another set of MOSFETs was used to do the grounding as shown in Figure 3.38.

Figure 3.38 Output stage of amplifier with grounding path

The two MOSFETs Q3 and Q4 are in series but back to back connected, this ensures their body diodes are not providing a conduction path. The one ohm series resistor acts as a damper for any voltage oscillations happening at switching time. The gate control signals for the grounding MOSFETs Q3 and Q4 are the same, which is obtained by inverting the control signals of Q1 and Q2 as shown in Figure 3.39. The inverted signal cannot be used directly as it does not have a dead-time period between the switching cycles and the grounding MOSFETs. A way of obtaining the new dead-time was by trimming the width of the gate control pulses as shown in Figure 3.40. First the original control signal (A) is delayed by a delay IC with a fixed delay time. The delayed signal (B) is then combined with the original using an AND gate. The output (C) gives the dead-time period that was fixed by the delay IC. The delay IC used here is a DS1135Z-10, which has a delay time of 10 ns. A shorter dead-time is used because the grounding MOSFETs do not carry as high a current as the main switching ones and there is less charge on the reverse recovery body diode, therefore the MOSFET can be switched faster.

Figure 3.39 The gate control signals (dark blue and cyan) and the grounding signal (purple)

Figure 3.40 New dead-time control method

Examining the output voltage oscillations at switching time in Figure 3.37, the voltage magnitude is very close to the MOSFET rating of 30 V. As a precaution, ± 10 V was used during development stage. A low pass matching network with a Q of 5 was used on the output; this reflects the 50 ohm load to 2 ohms for the switching node. Component values are 0.78 μ H for the inductor and 7.8 nF for the capacitor. Multiple capacitors were used in parallel to get the total capacitance value. Those values are not optimised yet at this stage of the design. To see if the modulation technique is working, two different amplitudes of input RF were used and the resulting outputs are shown in Figure 3.41 and Figure 3.42.

The voltage at the switching node (orange) is about 25% duty cycle in Figure 3.41. The output voltage (blue) after the filter and into the 50 ohm load has an amplitude of 50 V. A higher RF input produced a wider pulse at the switching node, about 45% as in Figure 3.42. The output amplitude is about 70 V. This comparison of results shows that the modulation technique does work.

Figure 3.41 Amplitude modulation at low duty cycle, voltage at the switching node (orange) and the output on the load (cyan).

Figure 3.42 Amplitude modulation at high duty cycle, voltage at the switching node (orange) and the output on the load (cyan).

In both of the results, the output is distorted. That is caused by the low Q of the matching network and the voltage spikes on the switching node. The supply voltage is also a factor as the switching voltage shows an increasing trend instead of a flat line. Further modifications were made to address those issues. A bigger capacitor of 2200 μF was installed on each of the supply rails. The Q of the output circuit was increased to 9 by using a 0.43 μH inductor and a 14.4 nF capacitor. Multiple capacitors were again used in parallel. A simple RC snubber circuit was used to compress the voltage spikes on the switching node. A 4.7 nF capacitor in series with a 2.2 ohm resistor was used. A new output from the circuit after those modifications is shown in Figure 3.43.

Figure 3.43 Amplitude modulation output after circuit modification, voltage at the switching node (orange) and the output on the load (cyan).

The figure shows a 35% duty cycle switched voltage (orange); it is clearly flatter and without spikes. The output voltage waveform (cyan) is a lot more sinusoidal compared to earlier results. These results prove that the modulation technique can be used to generate good output waveforms. The next step is to optimise the output stage using a circuit simulator, LTSpice. MOSFET models used in the simulation have the same switching properties as the ones used in the design but alternative MOSFET models were used because the simulator

does not have all the device models for all manufacturers. A schematic from the simulation is shown in Figure 3.44. By adjusting the component values, the optimum output for a fast rise and ring down time with 100 W output was found. The Q of the output network is 12 using a 0.29 μH inductor and 20 nF capacitor. A 20 μs pulse output from the simulation is shown in Figure 3.45.

Figure 3.44 Schematic for circuit simulation

Figure 3.45 Simulation output at the load

The output has a peak to peak voltage value of 216 V into a 50 ohm load. The power output is calculated to be 110 W RMS from a dual power supply of ± 15 V. The components of the actual physical design were modified using the suggested values from the simulator. The power supply rail was set to ± 14 V to avoid the voltage limits of the MOSFETs. A 15 μs pulse from maximum RF input is shown in Figure 3.46. This output shows good agreement with

results from the simulation. The rise time to reach steady state amplitude is about 3 μs and the ring down time is about 1 μs . Output power is calculated to be 100 W RMS.

Figure 3.46 Output of a 15 μs 100 W pulse

Figure 3.47 Amplitude modulated output pulses

To compare the change of amplitude, the input RF pulse was adjusted to -2.6 dB for the 90 degree pulse and 0 dB for the 180 degree pulses. The output is shown in Figure 3.47. The figure clearly shows the amplitude difference of the two pulses. At -2.6 dB input, the output pulse amplitude is half of the maximum output. Note that the amplifier now can operate in either constant amplitude mode or modulated amplitude mode by adjusting the

RF input amplitude. The next step is to test both of the operation modes in the RCA system by doing some NMR measurements.

The RCA system was setup for doing NMR measurements on an oil sample by the Magritek engineers at that time, using their internal Class A amplifiers. The new Class D amplifier was tested in that system on the same sample. Based on existing experiment parameters from the Class A amplifier, the parameters used for the Class D amplifier are shown in Figure 3.48. The CPMG sequence has 17 μs 90 degree pulse length, 5000 echoes and an echo time of 200 μs .

Figure 3.48 Prospra parameters of CPMG for Class D amplifier

Figure 3.49 High power CPMG sequence pulses

The output high power pulse sequence from the Class D amplifier was checked using a 50 ohm load before connecting to the sensor, the result is shown in Figure 3.49. The width of the pulses are in accord with the controlling sequence and with the right amplitude. Maximum output power is about 100 W RMS. The same experiments were performed on both the Class A and Class D amplifiers. Results obtained from the average of eight phase cycled scans are shown in Figure 3.50. Both results are plotted together for easier comparison.

Figure 3.50 CPMG results from both Class D (red) and Class A (blue) amplifiers, oscillations at the start of the imaginary data is much bigger for Class D.

The T_{2eff} decay data from the two amplifiers are the same. There are oscillations at the start of the imaginary data curve for both amplifiers, however the oscillation for the Class D amplifier is much bigger. Again this oscillation does not seem to affect the real component of the decay data.

The constant amplitude mode of the amplifier was also tested on the same sample using the pulse sequence from the previous constant amplitude amplifier. A screen shot of the parameters is shown in Figure 3.51. The output high power pulse sequence was also looked at before connecting to the sensor, the result is shown in Figure 3.52. The difference in pulse width of the 90 and 180 degree pulses is clearly shown.

Figure 3.51 Prospa parameters of CPMG for Class D amplifier

Figure 3.52 High power CPMG pulse sequence from Class D amplifier

Results obtained from the average of eight phase cycled scans are plotted together with the ones from the Class A amplifier as shown in Figure 3.53. The T_{2eff} decay data is still very similar; however the oscillation at the start of the imaginary data curve is greatly reduced on the Class D amplifier. The oscillations can be caused by the imperfect power level of the 90 degree pulse. With the amplitude modulation mode, the width modulation of the single pulse is very sensitive to the amplitude of the input RF. This is because for a narrow switching pulse, only the small area at the top of the sinewave is over the reference voltage (see Figure 3.34 earlier). A small change of magnitude on the input signal results in a big change in the

switching pulse width. There is not enough resolution for generating a precise amplitude low power 90 degree pulse, hence there is a bigger oscillation when operating in this mode. When operating in the constant amplitude mode, the change of power level is controlled by the width of the pulse sequence. This width is set by the timing parameters from the DSP, and has high resolution. Therefore the oscillation in this mode is lower, almost the same as the Class A amplifier.

Figure 3.53 CPMG results from both of the Class D (red) and Class A (blue) amplifiers

Looking into the pulse width modulation technique, if each cycle of the sinewave is made up of multiple smaller switching pulses instead of a single one, changing the amplitude would be a lot more precise. The next amplifier is designed using this technique.

3.4.4. Class D RF Amplifier with Single Cycle PWM Control

As shown in Figure 3.12 earlier, this design used a set of cycle selection signals with dead time control. These signals function the same way as the gate control signals in the previous Class D amplifiers, therefore the same input circuits from before can be used here. The new part needed for the circuit is a single cycle control method to generate multiple switching pulses.

The single cycle control circuit uses higher speed components due to higher frequency switching requirements of the design. The comparator LT1715 can be used again as it fits the requirement and has a dual package for both cycles. The D-flip flop chosen to be used here is

the NC7SZ74 manufactured by Fairchild Semiconductor. It is a high speed flip flop with a 5 ns response time and delay under 2.6 ns. The circuit can be separated into top and bottom sides as they function the same way and control the "high" side and "low" side MOSFETs accordingly.

On the top side of the circuit, the input RF signal is compared to the filtered feedback signal coming from the output of the D-flip flop, a "high" pulse is generated whenever the feedback is lower than the input on the positive input cycle. Similarly a "high" pulse is generated on the negative input cycle by the bottom side of the circuit. The outputs from those comparators are used as Data input to the D-flip flop. The function table of the D-flip flop is shown in Table 3.1. As explained in section 3.1.7 earlier, the proposed method requires the Q output "high" on the rising edge of the clock whenever the Data input is "high", otherwise output "low". This operation has to be controlled by the "high" part of an "enabling" signal. A study of the function table shows that those requirements can be satisfied if the comparator output is connected to the Data port, the "cycle selection" signal connected to the NOT Clear port, and the NOT PR port held "high". The functions used are marked on Table 3.3.

Table 3.3 Function table of a D-flip flop.

Inputs				Outputs		Function
$\overline{\text{CLR}}$	$\overline{\text{PR}}$	D	CK	Q	$\overline{\text{Q}}$	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Q_n	$\overline{Q}_n$	No Change

H = HIGH Logic Level
L = LOW Logic Level
 Q_n = No change in data
Z = High Impedance
X = Immaterial
↑ = Rising Edge
↓ = Falling edge

A circuit schematic with the connections as described is shown in Figure 3.54. The combiner circuit uses the OP695 amplifier as before, configured with two summation inputs and with the negative input side doing the inversion to give the negative cycle from the bottom side PWM signal. The two separated PWM signals are combined this way into one

feedback signal. The D-flip flop requires a Clock input, for this system a clock of 40 MHz or higher is used to generate pulses for a 2 MHz signal with good resolution. The KEA system has two output channels on the transceiver board, however only a sinewave is available on the transceiver output. A sinewave to clock converter is needed and the LT1715 comparator was again used on the design. The circuit was tested at a lower frequency of 500 KHz as slowing down the operation gives more details of the PWM signals. Using 500 KHz and 40 MHz signals from the KEA, and a 2 MHz low pass LR filter at the output of the combiner, PWM signals were observed on both of the D-flip flop outputs.

Figure 3.54 Schematic for the proposed single-cycle PWM controller

Figure 3.55 shows the waveforms at different parts of the circuit during the positive half cycle. The orange trace is the input signal, light blue trace is the output after the LPF which is also the feedback signal to the comparator. The green trace is the output of the comparator. Starting from the two comparator inputs, the input signal (orange) and the feedback signal (light blue), whenever the input is higher than the feedback, the comparator output (green) goes high. This resulting PWM signal goes to the input of the D-flip flop and the output is shown in Figure 3.56. The “high” input data (green) is transferred to the D-flip flop output (light blue) on the rising edge of the clock (purple). It is very clear that the D-flip flop output is clock controlled and the resolution is the period of the 40 MHz clock, 25 ns. The

same operation happens on the bottom side of the circuit for the negative cycle. This result agrees with the theory of single-cycle control.

Figure 3.55 Operation waveforms for the positive half cycle, orange is the input signal, light blue is the output after the LPF, green is the output of the comparator.

Figure 3.56 D-flip flop signals during the positive cycle, green is input data, D-flip flop output high (light blue) on the rising edge of the clock (purple)

The same output stage circuit from the previous amplitude modulation amplifier was used here with the modification of the low pass matching network to operate at 500 KHz. Component values were 3.75 μ H for inductor and 25.2 nF for capacitor. The output switching node is again held to ground after each of the switching pulses. The dead time control circuit is similar to the one earlier. A complete schematic of the new amplifier design is shown in Appendix III.

The gate control logic signals were first examined for the RF input of -6 dB, the output signals are shown in Figure 3.57. The gate signals for both the positive (purple) and negative (green) cycles are shown corresponding to the input RF (orange). The control signal for the grounding MOSFETs (light blue) is occurring only when the other two signals are off. The output into a 50 ohm load is shown in Figure 3.58.

Figure 3.57 The gate signals (purple and green) corresponding to the input RF (orange). Light blue is the control signal for the grounding MOSFETs.

The output into the load (light blue) looks very smooth. A higher power output from a -1 dB input is shown in Figure 3.59. The gate switching pulses are now a lot wider (green and

purple), the high power output (light blue) into the 50 ohm load is also increased, which confirms the modulation circuit is working.

Figure 3.58 The gate signals (purple and green) corresponding to the -6 dB input RF (orange). Light blue is the output on the load.

Figure 3.59 The gate signals (purple and green) corresponding to the -1 dB input RF (orange). Light blue is the output on the load.

The magnitude of the high power output suggested that the power supply of ± 15 V is not enough for getting a 100 W output into the load. However this voltage level is limited by the voltage rating of the MOSFET. A way of solving this issue is using two devices in series, known as a “Stacked FET” setup. This new output stage configuration is shown in Figure 3.60. Having two devices in series effectively doubles the overall voltage rating. To keep the voltage equally divided across the two devices, a capacitor divider was used on each pair of devices. Low value capacitors (10 nF) were used to limit the capacitance effect on the MOSFETs. With this setup, the voltage supply rails can be increased to ± 20 V and be still within the safe operating area of the MOSFETs. The gate control logic signal is the same for each stack therefore no additional circuits are need there. However the additional MOSFETs required their own driver and their reference points are also floating, therefore additional isolated supply modules and digital isolators are needed. The new schematic for this part of the circuit is shown in Appendix IV.

Figure 3.60 Output stage “Stacked FET” setup

The output low pass matching network from the previous amplitude modulation amplifier for 2 MHz was used again in here. Using the same Prospa parameter settings as

before, the amplifier output into a 50 ohm load was examined. Figure 3.61 and Figure 3.62 shows the gate control logic signals for the 90 and 180 degree pulses respectively.

Figure 3.61 RF input (blue) and gate control logic signals (cyan and purple) for 90 degree pulse

Figure 3.62 RF input (blue) and gate control logic signals (cyan and purple) for 180 degree pulse

Figures 3.61 and 3.62 clearly show that there are now more switching pulses for each half cycle and the position of the pulses are at the expected places. The width of the 180 pulses is clearly wider than that of the 90 degree pulses. The voltage level at the switching node for the 90 and 180 degree pulses are shown in Figure 3.63 and Figure 3.64 respectively.

Figure 3.63 The 90 degree high power switching pulses

Figure 3.64 The 180 degree high power switching pulses

The high power switching pulses shown are in agreement with the gate control pulses, this suggested that the Stacked FET output configuration is working. The next step is to have a look at the filtered output into a 50 ohm load. The close up view of the 90 and 180 degree pulse waveforms are shown in Figure 3.65 and Figure 3.66 respectively.

Figure 3.65 The 90 degree pulse waveform

Figure 3.66 The 180 degree pulse waveform

The close up views of the waveforms show smooth sinewaves without any obvious distortions. The amplitude of the 180 degree waveform is about twice that of the 90 degree, which is exactly as intended. The full length of the two individual 17 μ s pulses are shown in Figure 3.67 and Figure 3.68.

Figure 3.67 Output of a 17 us, 2 MHz 90 degree pulse

Figure 3.68 Output of a 17 us, 2 MHz 180 degree pulse

The peak to peak voltage value on the 180 degree pulse is 200 V, this is 100 W RMS power output into the 50 ohm load and is the maximum power output from the new amplifier. The rise and ring down time of this output is very similar to the previous amplifier, this is expected as the output network is the same. This new PWM controlled amplifier was used with the RCA to analyse a rock core sample [61]. The results are shown in Figure 3.69 and compared to the existing results taken by a Magritek engineer [62].

Figure 3.69 CPMG results from the PWM Class D amplifier (blue) and Tomco amplifier (red) for a rock core sample.

The results were obtained from the average of 128 phase cycled scans using a pulse sequence containing 50000 echoes. The T_{2eff} decay and spectrum data are almost identical from the two amplifiers. The oscillation shown earlier on the start of the imaginary data of the T_2 decay curve is now minimized. The existing result was taken using an external TOMCO Class A amplifier which has better temperature stability for doing long pulse sequences, such

as 50000 echoes on this sequence, compared to the internal Class A amplifier. The results show that the improved control over the amplitude and phase results in a reduction of the oscillations in the CPMG decay curves.

A photo of the final amplifier is shown in Figure 3.70 (top). Compared to the internal Class A amplifier (bottom) used in the KEA, one obvious difference is the big heatsink on the Class A amplifier. The Class D amplifier was designed to fit inside the KEA spectrometer therefore used the same euro-card size board as the Class A amplifier and no attempt was made to minimise size. The Class A amplifier has 25% efficiency therefore a big heatsink is needed. The efficiency of the Class D amplifier was measured to be 86%.

Figure 3.70 Picture of the two amplifiers, the new Class D (top) and the existing Class A amplifier (bottom)

3.5. Summary

This chapter has given details on the operation theory and circuit design of three different types of Class D amplifiers. They were transformer coupled voltage switching, simple pulse width controlled, and a proposed Single Cycle PWM controlled amplifier. The operation and properties of MOSFET devices have been discussed and selection of devices for both MOSFETs and drivers were shown. The selected devices were tested and shown to be capable of operating at 20 MHz. Using those devices, three Class D amplifiers were developed and constructed to operate at 2 MHz with output power of 100 W. Different types of CPMG pulse sequences were used to test the amplifiers using the Rock Core Analyzer system. The test results were compared to the ones from the existing Class A amplifier and shows great similarity. However the Class D amplifiers are a lot more superior in efficiency, with over 86% compares to 25% for the Class A.

Chapter 4. High Frequency Class D RF Amplifiers

This chapter focuses on the development of higher frequency Class D amplifiers. The first amplifier being developed is to push the capability of the switching MOSFETs to the limit for the highest switching frequency and output power. The target is to work with the 20 MHz MOUSE with 100 W of power. The second amplifier being developed is intended to work with the recently developed 17 MHz Mini-MOUSE sensor from RWTH, Germany. The requirements for this new amplifier being light weight, small size and output power of 30 Watts RMS; that is equivalent to a “peak to peak” voltage (V_{p-p}) output of 110 V into a 50 ohm load. The new amplifier is to be controlled by a single RF input signal and needs to have amplitude modulation capability for two fixed amplitude outputs of 90 and 180 degree pulses in one sequence. At present, the highest frequency of operation for Class D amplifiers working in NMR systems is reported to be 10 MHz, with output power of 5 W at 61% efficiency [63].

4.1. Development of a 20 MHz Class D RF Amplifier for the NMR MOUSE

The tests performed on the chosen MOSFET devices in Chapter 3 (Figure 3.17) have shown they are capable of operating at 20 MHz. Therefore the same devices and gate driver ICs are used in this design. The requirement of output power 100 W is very high for a Class D amplifier working at 20 MHz, therefore a full bridge configuration is used. The full bridge setup is also known as “H” bridge and it consists of two half-bridge circuits, it has higher output power capability compared to a half bridge [58].

A full bridge switching setup also allows better control of the amplifier at switch on and switch off as the two bottom MOSFETs can ground the output nodes to stop any oscillation. This is very important for NMR systems as it affects the rise time and ring down of the RF pulses being generated. A resonant tank was used to convert the high power pulses into sinusoidal waveforms, and a transformer was used at the output for impedance matching to a 50 ohm load. A simplified schematic diagram of the amplifier is shown in Figure 4.1(a) and a full schematic of the design is shown in Appendix V. The circuit is very similar to a full-bridge resonant LC power converter, the difference is that it does not have the rectifier diodes on the output. Switches S1 and S4 are controlled as one pair of devices to give the positive output cycles, while S2 and S3 give the negative cycle. The resonant tank formed by the LC network was tuned to match the switching frequency of the MOSFETs at 20 MHz.

(a)

(b)

(c)

Figure 4.1 (a) Simplified schematic of a full bridge resonant Class D amplifier. (b) LTSpice simulation circuit of the full bridge circuit at 20 MHz. (c) Simulation output, $V(p-p) = 56$ V, Power = 125 W RMS.

The output transformer was constructed using the same BN-61-002 material as in the previously built 2 MHz transformer coupled design, with a 1:4 ratio. The inductance of the LC tank circuit uses the leakage inductance of the transformer, measured to be 40 nH. The capacitance value of the tank circuit was found, using the LTSpice simulator to be 1.68 nF. The load resistance in the simulation was 3.125 ohms, this is the reflected impedance as seen by the MOSFETs on the primary side of the transformer. In the actual physical circuit board, the capacitance value was made up of three 560 pF capacitors in parallel to reduce ESR and improve performance. The LTSpice simulation circuit is shown in Figure 4.1(b) and the simulation output into the resistive load is shown in Figure 4.1(c). The output voltage at the load has a peak to peak value of 56 V, this is 125 W RMS power into the 3.125 ohm load. It is the power on the primary side of the transformer using ideal components. In reality, there will be power losses in components and the actual power capability would be lower. Even with the transformer losses, it is expected that at least 100 W will be delivered to the secondary side of the transformer to drive the 50 ohm load. The rise and ring down time from the simulation is under 100 ns.

A prototype of the design was built on a 4-layer PCB, this allows the final product to be compact and portable. The new amplifier has three input controls and one output, the same as the earlier 2 MHz amplifier designs. One input provides the RF driver signal. The input power level for maximum output is typically 1 dBm. The second input is a logic level gating signal for controlling the length of the high power output pulse. The third input offers phase control to the amplifier for amplitude modulation purposes when operating in lower frequency. Amplitude modulation was not tested for 20 MHz operation as only constant amplitude output was used with the MOUSE sensor. The finished amplifier weighs just under 120 g and the PCB area is 50 cm².

The output transformer was constructed using the same BN-61-002 material as in the previously built 2 MHz transformer coupled design, with a 1:4 ratio. The inductance of the LC tank circuit uses the leakage inductance of the transformer, measured to be 40 nH. The capacitance used was 1.68 nF, consisting of three 560 pF capacitors in parallel to reduce ESR and improve performance.

The existing Class A amplifier that is used in the KEA spectrometer weighs 480 g with a PCB area of 160 cm² (Figure 3.70). A photo of the new Class D amplifier is shown in Figure 4.2. One big difference between the amplifiers is the heat-sink which with the Class A amplifier is much bigger than that of the Class D unit. This is due to the inefficiency of the Class A amplifier as it loses a high percentage of power as heat which needs to be dissipated into the heat-sink.

Figure 4.2 The 20 MHz, 100 W Class D Amplifier (70x70 mm)

Normally amplifiers with a resonant tank output have the problem of long rise and ring down times and this problem was overcome by using low Q tank circuit and the intelligent switching of the MOSFETs. Low Q reduced the voltage overshoot at switching time therefore reduces ring down. The low side MOSFETs are grounded at turn off. The switching states of the four MOSFETs and the corresponding amplifier output states are summarised in Table 4.1.

Table 4.1 MOSFET switching states and amplifier outputs

S1	S2	S3	S4	Output
On	Off	Off	On	Positive cycle
Off	On	On	Off	Negative cycle
Off	On	Off	On	Off and grounded

The performance of the amplifier was compared to the Class A amplifier. Typical pulse lengths used with the MOUSE are between 2 μs and 10 μs . Figure 4.3 shows the two amplifiers outputting a short 100 W pulse into a 50 Ω load. It can be seen that the rise time of the Class A amplifier is a lot slower. The Class D output pulse reaches the maximum amplitude after the second cycle and stays constant for the duration of the pulse length.

Figure 4.3 The 100 W output pulses from Class A amplifier (top) and Class D amplifier (bottom) into a 50 ohm load

The 180 degree pulse is either doubled the amplitude or doubled the length of the 90 degree pulse. With classical amplifier systems, the double amplitude method is used as it is easy to implement and provides constant excitation bandwidth. However for the Class D amplifiers without amplitude modulation the double pulse length method is easier and used again here. A Spin Echo pulse output from the two amplifiers is shown in Figure 4.4.

Figure 4.4 Spin Echo pulses from the Class A amplifier (top) and Class D amplifier (bottom) into a 50 ohm load

This clearly shows that the 180 degree pulse from the Class A amplifier is still increasing at the end of the pulse, while the Class D pulses show constant amplitude even when doubling the pulse length. The TTL pulse in the same figure shows the turn on and off times of the RF pulse. The CPMG sequence is shown in Figure 4.5, while only the first four of the 180 degree pulses are shown, it is clear that the Class D amplifier output maintains constant amplitude.

Figure 4.5 CPMG pulses from Class A amplifier (top) and Class D amplifier (bottom) into a 50 ohm load

The efficiency of the two amplifiers was compared using their average input and output power over a long CPMG pulse sequence consisting of 128, 180 degree pulses at 10% duty cycle. A current probe was used to measure the current draw from the power supply while the amplifier was running. This was then compared to the steady value when the amplifier is not running. The difference in current allows the calculation of input power. The current probe used a setting of 100 mV/A. The results are shown in Figure 4.6.

Figure 4.6 Power measurement of Class A amplifier (top) and Class D amplifier (bottom) using a 50 ohm load

The DC input voltage was measured to be 23.3 V and the output was into a 50 Ω load, the figures showing the corresponding current measurement for the Class A amplifier is 2.08 A, and 0.6 A for Class D. The output voltage for Class A is 190 Vpp and 202 Vpp for Class D. Based on those values, the efficiency of the Class A amplifier was calculated to be 19% and 73% for Class D. Note that the drop in efficiency of the amplifiers are due to the higher operating frequency compared to the 2 MHz operation earlier. Higher switching losses occur at higher frequencies. A summary of the measurement parameters is shown in Table 4.2.

Table 4.2 Measurement parameters for both amplifiers.

Parameters	Class A	Class D
V_{in} (V)	23.3	23.3
I_{in} (A)	2.08	0.6
$V_{out, Vp-p}$ (V)	190	202
Efficiency	19%	73%

Figure 4.7 Spin Echo results from the Class A amplifier (top) and the Class D amplifier (bottom)

Both amplifiers were used with the 20 MHz MOUSE sensor and performed the same experiments on a rubber sample. Figure 4.7 shows the Spin Echo experiment results. The Spin Echo results were obtained from a phase-cycled data-averaged sequence of 16 scans. The two results being similar is an indication of the two amplifiers outputting the same level of power over the duration of the 16 scans. The higher amplitudes of the Class D data is a result of slightly higher power output by the amplifier as shown by the power measurement results earlier.

The CPMG results were also obtained from the average of 16 phase cycled scans and shown in Figure 4.8. This time the pulse sequence is much longer, with 128 echoes forming in each sequence, this is shown as the Raw CPMG echo data on the left hand side of the figures. The similar decay constants and amplitudes suggest that the stability of the amplifier is close to that of the Class A amplifier.

Figure 4.8 CPMG results from the Class A amplifier (top) and the Class D amplifier (bottom)

The similarity of the NMR test results between the Class A and Class D amplifiers suggests that the latter is capable of producing the output power and pulse sequences necessary for those NMR experiments while doing so in a more efficient way. The compact size and light weight makes the Class D amplifier particularly suitable for use in portable NMR systems. The efficiency of 73% at the operating frequency of 20 MHz with 100 W output power, combining with the fast rise time and short turn off time is a significant improvement when compared with the existing Class A amplifier used with the MOUSE sensor. It is also superior compared to the one that reported operating at 10 MHz, with output power of 5 W and 61% efficiency [63].

The recently developed 17 MHz Mini-MOUSE sensor is smaller and lighter than the 20 MHz MOUSE. It also requires a lower power of 30 W to operate. One of the main targeted applications of the Mini-MOUSE is looking at plastic materials and piping, which has very short NMR signal durations. Note that the CPMG pulse sequence used with the 20 MHz amplifier has the 180 degree pulse with double the length of the 90 degree pulse. Each pulse excites a different region in the inhomogeneous field, i.e. the narrower the pulse the wider the frequency band and hence in inhomogeneous fields the broader the sample region. This is not ideal as it can lead to artefacts. The next section looks to develop a 17 MHz amplifier with amplitude modulation to overcome this drawback.

4.2. Development of a PWM controlled 17 MHz Class D RF Amplifier

The 2 MHz amplifier discussed in section 3.4.3 earlier has the required amplitude modulation capability. Therefore here we will use the same design as a starting point, and tune the output circuit to work at 17 MHz. One of the advantages of operating at a higher frequency is the physical size of the inductor and capacitor in the output filter is reduced, allowing a smaller size PCB layout. Since this amplifier is not designed to be used inside the KEA system and compact size is the goal, a new layout of the amplifier was done. A prototype was built on a 4-layer PCB with an area of just under 40 cm². A picture of the new amplifier prototype is shown in Figure 4.9.

Figure 4.9 Prototype of a 17 MHz, 20 W Class D RF amplifier with amplitude modulation capability, 60x65 mm.

Amplitude modulation was achieved by controlling the width of the gate driver signal on each switching cycle, which in turn is controlled by the amplitude of the input RF signal as explained earlier. Figure 4.10 shows the control signals and RF output for the 90 degree pulses, and Figure 4.11 shows the same for the 180 degree pulses. A dual polarity power supply of ± 10 V was used with those measurements. The output low pass matching network has a Q of 10 with component values of $L=46$ nH and $C=1.8$ nF. The figures clearly show that the amplifier is working as intended; a narrow width control signal produced a lower amplitude output ($26.4V_{p-p}$) for the 90 degree pulses and a full width control signal produced a higher amplitude output ($52 V_{p-p}$) for the 180 degree pulses.

A limitation on this modulation method at 17 MHz is the switching capability of the MOSFETs. While the MOSFET is able to switch at 17 MHz, it also requires a minimum on time of 10 ns, which means that the minimum width of the control signal for the 90 degree pulses cannot be less than 10 ns. That limits the minimum output of the amplifier to a fixed level. There will be no output if the control signal is less than 10 ns as the MOSFET is off. For higher output power, the maximum supply of ± 15 V was used. Figure 4.12 shows a 2 μ s pulse at the maximum power output (180 degree pulse), measured at $90.4 V_{p-p}$, that is 20 W RMS. A close up of the 90 degree pulse is shown in Figure 4.13. It has a peak to peak voltage of 45.2 V, that is half the amplitude of the 180 degree pulse.

Figure 4.10 The control signals (light and darker blue) and RF output (purple) for the 90 degree pulses.

Figure 4.11 The control signals (light and darker blues) and RF output (purple) for the 180 degree pulses.

Figure 4.12 Output of a 2 μ s 180 degree pulse on a 50 ohm load

Figure 4.13 A close up of the 90 degree pulse

4.3. NMR Testing on a 17 MHz Sensor

At the time of designing the amplifier, the intended Mini-MOUSE sensor to be used with was not available, therefore a 17 MHz sensor was built to test the amplifier. It used a 0.5 T permanent magnet and an LC circuit tuned to 17 MHz as shown in Figure 4.14. The sensor was housed inside an aluminium box to reduce noise. It had a Q of 30, the inductor value was $2.14\ \mu\text{H}$, adjustable capacitors were used to tune and matched the probe to 50 ohm at 17 MHz. The sample used was a slice of pencil eraser. A picture of the sensor construction is also shown in Figure 4.14. This simple sensor was built for test purposes only.

Figure 4.14 Construction of a 17 MHz NMR sensor and housing

Figure 4.15 Centre frequency found by Wobble at 17.06 MHz

The new 17 MHz sensor was first used with the Class A amplifier on the KEA, the resonance frequency of the sensor was found using the Wobble experiment in Prospa. Wobble sweeps over a range of frequencies and measures the reflected power from the sensor. When the sensor is tuned to the resonance frequency and matched to 50 ohm, the reflected power is at a minimum, i.e. a dip on the plot. Figure 4.15 shows the result and the frequency is very close to 17 MHz. By adjusting the parameters in Prospa, the optimum pulse length to use was found to be 4.5 μs using 30 W RMS power output from the amplifier. The performance of the Class D amplifier is compared to the Class A amplifier using the same CPMG experiment. Similar pulse sequence parameters were used in Prospa, the only difference being the amplitude of the input RF signal setting as the pulse width is not related to the input amplitude in a linear way. Figure 4.16 shows the Prospa parameters for the Class D amplifier.

Figure 4.16 Prospa parameters for the CPMG experiment on the Class D amplifier

The raw echo data for both of the amplifiers is shown in Figure 4.17. Comparing the raw CPMG echo data, the Class A amplifier has a higher signal level of 4 μV while the Class D amplifier has 2.5 μV . This is because the maximum output power of the Class D amplifier is only 20 W, the Class A amplifier was outputting 30 W, hence a higher signal level. Another way of comparing the two amplifiers was to use the decay curves from the CPMG experiments.

Figure 4.17 Raw CPMG echo data for both amplifiers

The two curves from the average of 256 scans were normalised and shown in Figure 4.18. The two curves are very much on top of each other, this similar decay curve suggests that the stability of the Class D amplifier is close to that of the Class A amplifier. Despite the lower output power, the same decay curve was obtained for the same sample. A curve fit finds the T_{2eff} of the rubber sample to be 4.23 ms, Figure 4.19.

Figure 4.18 Normalised CPMG decay curves

Figure 4.19 Single exponential curve fit finds T_{2eff} at 4.23 ms

4.4. Development of a 17 MHz Class D RF Amplifier with Amplitude Modulation

In order to get a higher output power of 30 W, the Class D amplifier was further developed and used another method of modulating the output amplitude. The idea is using two different levels of supply voltages for generating the 90 and 180 pulses separately. In the earlier designs, both the 90 and 180 degree pulses were generated from the same power supply rail, resulting in using a very low duty cycle switching pulse for generating the 90 degree pulse. If the power supply for the 90 degree pulses is lower, then a higher duty cycle of switching can be used. Furthermore, if the supply is adjusted to a suitable low level then the maximum duty cycle of just under 50% can be used, which is the same duty cycle as for the 180 degree pulses. This means the control logic for the new design is very similar to the constant amplitude design of the 2 MHz amplifier earlier but using the RF input sequences from the amplitude modulation setup, ie, same pulse length on the RF input for the 90 and 180 degree pulses. In a way the new design combines the two variations of the 2 MHz amplifiers in Chapter 3 into one. The amplitude modulation capability is preset by the voltage supply levels of the two supply rails.

A simplified schematic of the new design is shown in Figure 4.20. The full design schematic is shown in Appendix VI. This design uses two fixed levels of DC supply voltages, while the earlier circuit used a single dual polarity supply. The new circuit has an extra MOSFET (Q1), it turns on to connect with the higher supply for outputting the 180 degree pulses only. When Q1 is on, the voltage at the Drain of Q2 is V(High) because V(High) is at a higher potential than V(Low) therefore D1 is reverse biased and not conducting. When Q1 is off D1 is forward biased and the voltage at the Drain of Q2 is V(Low), this is the default connection for 90 degree pulse outputs. A new TTL control line is used to control Q1. The logic control lines and RF pulses of a CPMG sequence for the new design is shown in Figure 4.21.

Figure 4.20 Simplified schematic of a new Class D RF amplifier circuit

Figure 4.21 The logic lines and RF pulses of a CPMG sequence for the new design

It is important to have the higher voltage supply on the MOSFET Q1 and the lower voltage on D1, reversing them will result in a conducting path along D1 and the body diode of Q1, that will damage both the MOSFET and the diode. Q2 and Q3 operate the same way as in the earlier Class D circuit with switching duty cycles of just under 50% with a 10 ns dead time control. However the output has a tank circuit (C1 and L1) in front of the low pass matching network (L1 and C2) as the amplifier operates in a resonant mode. Resonant mode is used because it has to generate the negative cycle on the output from a positive DC supply. The new output circuit was again optimised using LTSpice simulation. Components used in the simulation model were chosen and adjusted to be as close as possible to the real devices used. The simulation circuit is shown in Figure 4.22 and the output is shown in Figure 4.23.

The output circuit was adjusted to have a Q of 10 and output power of 30 W RMS into a 50 ohm load.

Figure 4.22 LTSpice simulation circuit for the output of the new Class D amplifier

Figure 4.23 Simulation output, $V_{p-p} = 111$ V, $Power(RMS) = 30$ W

From a 24V DC input, the simulated output power was 30 W RMS, this is the maximum output and will be used as the 180 degree pulse power. The supply voltage required for generating the suitable 90 degree pulse power was determined experimentally. A prototype board was built and tested. Figure 4.24 shows the measured output into a 50 ohm resistive load, the pulse length was 10 μ s and there were 5000 pulses in the sequence. The measured

output agrees well with the simulated output, with rise and ring down times of under half of a micro second.

Figure 4.24 Output of a 10 us, 180 degree pulse

A close up of the output is shown in Figure 4.25, it is a clean signal with little noise and harmonic distortion. The supply voltage required for generating the 90 degree pulses at half amplitude of the 180 degree pulses was 16V. This was obtained by using a step down regulator on the DC supply of 24 V. An output showing both the 90 and 180 degree pulses is shown in Figure 4.26.

Figure 4.25 A close up of the 180 degree output pulses.

Figure 4.26 The 90 and 180 degree pulses into a 50 ohm load

The performance of the new Class D amplifier is compared to the Class A amplifier using the same CPMG experiment as before. Figure 4.27 shows the Prospa parameter settings

for the new Class D amplifier. The raw echo data for both of the amplifiers are shown in Figure 4.28.

Figure 4.27 Prosipa parameters for the CPMG experiment on the new amplifier

Figure 4.28 Raw CPMG echo data for both Class A and Class D

Comparing the raw CPMG echo data, the maximum signal from the two amplifiers are the same at 4 μV . This suggested that the power output of the two amplifiers is at the same level, 30 W RMS. The decay curves from the CPMG experiments are compared again, the two curves from the average of 256 scans are shown in Figure 4.29. The two curves are very close together, this is a good indication that the new Class D amplifier has the same stability and output power as the Class A amplifier.

Figure 4.29 CPMG decay curves for both amplifiers

Figure 4.30 Single exponential curve fit finds $T_{2\text{eff}}$ at 4.3 ms

A single exponential curve fit on the decay curve finds the T_{2eff} to be 4.3 ms, Figure 4.30, this is very close to the value of 4.23 ms as measured using the previous amplifier. Given the rubber sample on the sensor is the same, a close T_{2eff} value is as expected. The efficiency of the new Class D amplifier was measured using the same average power method as for the 2 MHz amplifier earlier. The efficiency of the new Class D amplifier is 82%, which is very high compared to the 25% from the Class A amplifier.

The 17 MHz Class D amplifier has higher frequency, higher output power and efficiency compared to the ones reported by other researchers [63]. This is an achievement on its own and it also gives the opportunity for developing compact mobile NMR systems.

4.5. Summary

This chapter has shown the development of higher frequency Class D amplifiers. First a 20 MHz full bridge design with 100 W constant output, then a 17 MHz 30 W output with amplitude modulation capability. LTSpice simulation was used on the design to optimise circuit component values. Both of the amplifiers were thoroughly tested using the KEA system on their corresponding frequency sensors. Test results from spin echo and CPMG experiments were compared to the Class A amplifier again and shown to be very similar.

Chapter 5. Mobile NMR System Development and Integration

This chapter details the development of a full Mobile NMR system. New system hardware was built and control software was developed to operate the new system. The goal was to have a compact and portable handheld NMR system working with a 17 MHz Mini-MOUSE sensor. This development is made possible due to the compact and small size of the 17 MHz Class-D RF amplifier and the availability of a new System-on-chip (SoC) module.

Portable NMR systems are often designed for a specific purpose or to work with a sensor at a certain frequency, eg. LapSpec+MOUSE; unlike the bench top systems that are configurable, eg. KEA. It is this specialised operation that allows them to be designed and build with minimal hardware to be compact and portable. A mobile system can be frequency specific for looking at targeted materials. The applications of the MOUSE sensor include looking at polymers, paintings, human skin and tissue [64]. Combining the MOUSE sensor with the compact Class-D RF amplifier and using a digital transceiver, a mobile system with specific application is a real prospect.

5.1. Introduction to the Digital Transceiver

The digital transceiver in a NMR system has the function of generating the RF pulses and control signals on the transmitting side and detecting the NMR signal from the sensor on the receiving side, as illustrated in Figure 5.1. Analogue to digital converter (ADC) and digital to analogue converter (DAC) devices are used to interface between the digital and analogue signals.

Figure 5.1 Digital transceiver connection block diagram

The digital transceiver can be divided into two parts, a transmitter and a receiver. The receiver functions the same way as the ones in many radio systems, i.e. it generates a set of baseband quadrature signals. The major components of a digital receiver are the local oscillator, mixer, and low pass filter as shown in Figure 5.2. The local oscillator generates two digital sinewaves that are phase offset by 90 degrees. The mixer part of the system consists of two digital multipliers. The digital input samples from an ADC are multiplied by the sine and cosine values from the local oscillator. The digital input samples and the local oscillator samples are being generated at the same rate and the two devices share a common clock source. The two outputs from the multipliers are high sample rate baseband In-phase (I), and Quadrature (Q), outputs that contain the amplitude and phase information from the input signal. The mixed outputs are then fed into decimating low pass filters to reduce the sample rate, but maintain the original signal. The digital filter is a complex filter and both real and complex values are available at the output.

Figure 5.2 Block diagram of a digital receiver

There are digital receiver chips available such as the AD6620, which consists of a complex local oscillator, quadrature mixers and Cascaded Integrated Comb (CIC) filters [65]. Another way of implementing a digital receiver is to use a Field Programmable Gate Array (FPGA). FPGAs have built-in hardware multipliers and on-chip memory, the use of Intellectual Property (IP) functional blocks makes designing a receiver a relatively simple process. FPGAs also provide high performance signal processing capability to analyse data on the fly.

The transmitter is a Direct Digital Synthesizer (DDS), it uses a digital phase accumulator and lookup tables to generate precise values to form a digital waveform (sine or cosine), and a DAC is used to convert the digital signal to an analogue form when needed. Many DDS devices available on the market have the DAC build-in as part of the IC. The DDS has amplitude and frequency switching capability via control registers. This allows the frequency to be changed as required which is necessary for the Wobble function. Figure 5.3.

Figure 5.3 Frequency switching with continuous phase on DDS output

Using a FPGA is a good solution for implementing the digital receiver system; however the FPGA requires other supporting components to work, such as a controlling micro-processor and memory chips. A new design using FPGA components requires the development of very complex circuitries and the time needed will be an issue for this project. A new trend in FPGA design is the use of newly available System-on-Chip (SoC) devices and the next section provides more detail.

5.2. The Zynq SoC Systems

In a traditional FGPA design, separate supporting components such as micro-controller and memory chips are needed as illustrated in Figure 5.4. Due to the high number of pins from the components, complex PCB layouts are necessary and sometimes long routing tracks on the PCB is unavoidable. This could introduce noise and skew and therefore lower the system performance. Layout of a complex PCB is also a time consuming process. Having lots of high speed input/output (IO) lines routed also increases power consumption as well as radiated EMI.

Figure 5.4 Block diagram of a traditional FPGA design

The simplest way to see a SoC system is to think of it as a computer system with processor, memory, and user control IO lines - all inside one IC package. The Zynq SoC system simplified the FPGA design by including an onboard processor with some memory [66]. This eliminates the need for PCB routing. The Programmable Logic (PL) part of the system is the equivalent of an FPGA, Figure 5.5.

Figure 5.5 Hard and Soft processors of Zynq SoC [67]

The Zynq SoC processor system (PS) is built around a dual-core ARM Cortex-A9 processor. It is a dedicated and optimised high performance "hard" processor. High speed busses between parts is provided to achieve high data transfer performance. Apart from the "hard" processor, there is an alternative "soft" processor, a MicroBlaze. It is formed by combining elements of the PL. A soft processor has lower performance but it has the advantage of being flexible and configurable for doing dedicated tasks. Multiple MicroBlaze

processors can be implemented within the PL. Having small tasks done in MicroBlazes frees up resources in the PS for performing more calculation intensive tasks for better performance. The PS can boot from a selection of memory devices and PL is configured after the PS is booted.

The Zynq SoC system not only has the high performance processors, but also the associated resources needed for application development. There are peripherals, cache memory and interfaces, etc. A block diagram is shown in Figure 5.6. The IO peripherals available to the user include USB, Ethernet, SPI and UART. There are high speed AXI interfaces for configurable 32 bit or 64 bit operations. Onboard memory controller and interface allows connection to high speed, high capacity external DDR memory.

Figure 5.6 Block diagram of Zynq SoC system [68].

A detailed diagram showing the ARM Cortex-A9 processor as functional blocks and their inter-connections is shown in Figure 5.7. Some highlights of the ARM processor are listed below [13]:

- Dual-core processor
- Self-contained 32KB L1 cache per core
- 512 KB L2 Cache
- Automatic cache coherency between processor cores
- Supports both 16-bit and 32-bit instructions
- Up to 1 GHz operation

Figure 5.7 The ARM processor inside the Zynq SoC [66].

The trend of FPGA evolution is using SoC and the Xilinx' Zynq SoC is one of many available in the market. The Alterra Arria series SoC is the exact equivalent; then there is the A8 series from Apple Inc. Cypress has the PSoC (Programmable System-on-Chip), and Intel has the Quark SoC X1000 Series. While those SoC systems are all suitable to use in this project, the reason for choosing the Xilinx Zynq SoC is that Xilinx supply a complete set of development tools and we have previous experience with it. Our research group have been developing IP functional blocks to use with the Zynq system and those can be used in this project. The next section gives details on the Xilinx development tools available.

5.3. The Xilinx Development Tools

Traditional designs of FPGA systems are challenging as the hardware and software parts of the embedded design are complex projects in themselves. The Xilinx Zynq SoC system offers a solution to simplify the design process by offering an onboard processor and programmable logic on a single chip. Xilinx offers a set of development tools to use with the Zynq SoC system:

- Vivado Design Suite
- Software Development Kit (SDK)
- PetaLinux

5.3.1. Vivado Design Suite

The Vivado Design Suite consists of FPGA synthesis, simulator and IP functional block integrator tools for hardware designing and configuration. This all in one package is the most easy to use application development tools available for FPGA systems. The Vivado *Web PACK™* Edition is available from Xilinx free of charge.

Description	IP Version	IP Type	Status	Processor Support	IP Classification
Analog					
AXI System Monitor/Analog-to-Digital Converter	2.00.a	axi_sysmon_adc	PRE_PROD...	MicroBlaze	PERIPHERAL
AXI XADC	1.00.a	axi_xadc	PRE_PROD...	MicroBlaze	PERIPHERAL
Arithmetic					
APU Floating Point Unit	3.10.a	apu_fpu	PRE_PROD...	PowerPC	PERIPHERAL
V5 APU Floating Point Unit	1.01.a	apu_fpu_virtex5	PRE_PROD...	PowerPC	PERIPHERAL
Bus and Bridge					
Clock, Reset and Interrupt					
Communication High-Speed					
Communication Low-Speed					
DMA and Timer					
Debug					
FPGA Reconfiguration					
FPGA Internal Configuration Memory	2.03.a	axi_hwicap	PRE_PROD...	MicroBlaze	PERIPHERAL
General Purpose IO					
AXI General Purpose IO	1.01.b	axi_gpio	PRE_PROD...	MicroBlaze	PERIPHERAL
LMB I/O Module	1.01.a	iomodule	PRE_PROD...	MicroBlaze	PERIPHERAL
Interprocessor Communication					
Memory and Memory Controller					
AXI 7 Series Memory Controller	1.05.a	axi_7series_ddrx	PRE_PROD...	MicroBlaze	PERIPHERAL
AXI BRAM Controller	1.03.a	axi_bram_ctrl	PRE_PROD...	MicroBlaze	PERIPHERAL
AXI External Memory Controller	1.03.a	axi_emc	PRE_PROD...	MicroBlaze	PERIPHERAL
AXI System ACE Interface	1.01.a	axi_sysace	BETA	MicroBlaze	PERIPHERAL
Block RAM (BRAM) Block	1.00.a	bram_block	PRE_PROD...	PowerPC, MicroBlaze	PERIPHERAL
LMB BRAM Controller	3.10.a	lmb_bram_if_cntlr	PRE_PROD...	MicroBlaze	PERIPHERAL
System Cache	1.01.a	system_cache	PRE_PROD...	MicroBlaze	PERIPHERAL
PCI					
Peripheral Controller					
Processor					
MicroBlaze	8.40.a	microblaze	PRE_PROD...	MicroBlaze	PROCESSOR
Processing System	4.01.a	processing_system7	PRE_PROD...		PROCESSOR

Figure 5.8 Example of IP blocks available

Vivado provides a graphical design environment; it uses functional block components as IP blocks. Users can create a design in Vivado by simply connecting IP blocks together. Xilinx libraries supplies a range of IP blocks, some examples are shown in Figure 5.8. Customised IP blocks can also be created by the user using the IP Integrator (IPI) feature in Vivado. Figure 5.9 shows a system design using IP blocks in Vivado.

The “ZYNQ” processor is itself an IP block but in this case is hard logic. A block diagram of the Zynq SoC is shown in Figure 5.10. It gives a clear view of the system and peripheral IOs available and their configurations.

Figure 5.9 System design using IP blocks in Vivado

Figure 5.10 The Zynq processor system in Vivado

5.3.2. Software Development Kit (SDK)

SDK is the Xilinx Integrated Design Environment for creating embedded applications on Xilinx' devices such as the Zynq-7000 All Programmable SoCs. It also supports multi-processor design and debug. Some highlights of the SDK are listed below and a screenshot of the SDK environment is shown in Figure 5.11.

- Direct interface to Vivado hardware design environment
- Complete software design and debug flows supported
- Editor, compilers, build tools, flash memory management, and JTAG/GDB debug integration
- Custom libraries and device drivers

Figure 5.11 SDK environment

SDK is an integrated development environment complementary to Vivado, it uses C/C++ for embedded software application creation and verification. Other components in the package include:

- Hardware IP for the Xilinx embedded processors
- Drivers and libraries for the embedded software development
- GNU compiler and debugger for C/C++ software development targeting the ARM Cortex-A9MP processors in the Zynq Processing System

The design workflow in SDK can be summarised in three steps and as illustrated in a block diagram in Figure 5.12. Only the “.elf” executable file is transferred to the target device. The design flow sequences are:

1. SDK builds the Board Support Package (BSP) files using Libgen
2. SDK compiles the application software using a platform-specific gcc/g++ compiler.
3. The object files and BSP are linked together to form an executable, elf file.

Figure 5.12 Design workflow in SDK [69].

5.3.3. PetaLinux

The PetaLinux Software Development Kit is a Xilinx development tool that contains everything necessary to build, develop, test and deploy Embedded Linux systems. It provides a complete embedded Linux distribution for Xilinx hardware. It includes pre-configured binary bootable images with Board Support Packages, and Host Development tools, for deploying fully customizable Linux on Xilinx devices. The reference Linux distribution for Xilinx devices includes:

- Boot loader
- CPU-optimized kernel

- Linux applications & libraries
- C & C++ application development
- Debug
- Integrated web server – uweb

An overview of the connections between PetaLinux and Xilinx tools is shown in Figure 5.13. Xilinx open sources components (Linux, U-boot, etc.) is used through a PetaLinux distribution package. PetaLinux compiles the boot files for targeted devices using hardware data from Vivado.

Figure 5.13 Connection between Xilinx Vivado and PetaLinux [70]

5.3.4. Design Process

Vivado is used for system hardware development; it sets the specification of the microprocessor, peripherals, and configures the interconnection between them. The Zynq Processing System can be started and run without anything being programmed inside the

FPGA programmable logics (PL). But to use any soft IP functions or processor system (PS) peripherals, programming of the PL is required and this is done from within SDK.

The Zynq SoC system requires hardware configuration information for both the PS and PL on start up, this is obtained by way of boot image files. The Zynq SoC supports booting from off-chip memories such as Quad SPI flash or SD card. Two files are needed to boot the system: “Boot.bin” and “Image.ub”. The boot image files are compiled in SDK. The “Boot.bin” file contains the following:

- First stage boot loader (FSBL)
- PS/PL configuration bit file
- u-boot.elf

The FSBL is responsible for initializing the PS and configuring the PL with the information provided by the bit files that are generated in Vivado. The “u-boot.elf” file contains information about the Board Support Package (BSP) and starts the kernel for the Linux OS. “Image.ub” contains the kernel and file system of a Linux OS; this is where the web server files are stored for used with an Ethernet connection. The Xilinx tool chain can be summarised in Figure 5.14.

Figure 5.14 Xilinx tool chain

On system power up, the FSBL first configures PS and PL, and then loads the Linux file system image into memory space as a ramdisk. The file system contains a web server and the system is configured to obtain an IP address from a DHCP host once an Ethernet connection is active. The system is accessible through a serial interface or using the IP address. Communication protocols such as ssh, http, telnet, etc, are all supported.

5.3.5. MicroZed Module

The Xilinx Zynq-7000 SoC system is available in a module form called “MicroZed” [71]. Figure 5.15 shows the top and bottom views of the module. The size of the module is 101mm x 57mm, ideal for a compact system. Using the MicroZed module is a good option as it has all the necessary peripherals connected to suitable connectors, eg, USB, Ethernet. The user I/O lines are available through two 50-pin microheaders on the bottom side of the module. The module comes with pre-build PetaLinux boot files and cost 199 USD.

Some technical specifications of the module is listed below:

- Processor: Xilinx XC7Z010-1CLG400C SoC operating at 800 MHz
- Memory:
  - 1 GB DDR3
  - 128 MB QSPI Flash
  - microSD Card extension
- Interfaces:
  - Xilinx PC4 Header for programming: JTAG and Digilent Pmod
  - 10/100/1000 Gb Ethernet
  - USB Host 2.0
  - microSD Card
  - USB 2.0 Full-Speed USB-UART bridge
  - Digilent Pmod compatible interface, connected to PS MIO
  - Two 100-pin MicroHeaders
  - LEDs
- On-board Oscillator: 33.333 MHz

Figure 5.15 The MicroZed module (101x57mm), top and bottom views. The FPGA, memory and other ICs are on topside; user IO connectors are on bottom side.

The connections of the processor system to the interfaces are illustrated in Figure 5.16.

Figure 5.16 The MicroZed module connection diagram [71]

The connections available on the two microheader connectors are listed on Table 5.1. The programmable logic IO lines on Header#1 (49) and Header#2 (50) offers a big range of user control lines.

Table 5.1 Micro header connections [71]

MicroHeader #1				MicroHeader #2				
Signal Name		Source	Pin Count	Signal Name		Source	Pin Count	
PL	Bank 34 I/Os (except for PUDC_B)	Zynq Bank 34	49	PL	Bank 35 I/Os	Zynq Bank 35	50	
JTAG	TMS_0	Zynq Bank 0	5	PS	PS Pmod MIO[0,9-15]	Zynq Bank 500	8	
	TDI_0	Zynq Bank 0		C	Init_B_0	Zynq Bank 0	2	
	TCK_0	Zynq Bank 0			Power	Vccio_EN	Module/Carrier	1
	TDO_0	Zynq Bank 0				PG_MODULE	Module/Carrier	1
	Carrier_SRST#	Carrier				Vin	Carrier	5
Analog	VP_0	Zynq Bank 0	4	GND		Carrier	23	
	VN_0	Zynq Bank 0		VCCO_35		Carrier	3	
	DXP_0	Zynq Bank 0			Bank 13 pins	Bank 13 **	8	
	DXN_0	Zynq Bank 0			Total 100			
	C	PUDC_B / IO		Zynq Bank 34				2
DONE		Zynq Bank 0						
Power	PWR_Enable	Carrier	1					
	Vin	Carrier	4					
	GND	Carrier	23					
	VCCO_34	Carrier	3					
	VBATT	Carrier	1					
	Bank 13 pins	Bank 13 **	8					
TOTAL			100					

5.4. Full System Outline

The XC7Z010 Zynq FPGA processor on the MicroZed board is a Cortex™-A9 MPCore processor, combining with 1 GB of DDR3 Memory onboard, the processing power available on this system is equivalent to many mainstream tablets available on the market today, therefore it is possible to use this system to do the NMR data processing in place of a computer.

Figure 5.17 Outline of the new NMR system.

An outline of the new system hardware is shown in Figure 5.17. It is designed based on the interfaces available on the MicroZed module. The MicroZed module has integrated USB and Ethernet connection ports. There is also a PMOD connector for using an optional WIFI module. The idea is to use the Ethernet or WIFI link to connect to a mobile device with a screen to display the NMR data, that could be an iPad or even a smartphone. The NMR data can be stored locally on the MicroZed board using the Linux host system or on an SD card.

The controlling pulse sequence is stored in the FPGA system and transmitting and receiving are through the DDS and ADC respectively. The ADC is needed because the input RF signal is in analogue form.

The sensor to be used with the system is the 17 MHz Mini-MOUSE, therefore a duplexer is designed to operate at that frequency. The duplexer controls the signal flow direction of the RF. During transmission it only connects to the RF amplifier allowing the high power RF signal to drive the probe, and during reception it isolates the RF amplifier and only connects to the receiver amplifier to receive the signal. An amplifier is needed on the receiver because of the low power level of the NMR signals, typically in the micro-volt range and cannot be read by the ADC directly.

Based on the system outline, new hardware needs to be built to communicate with the MicroZed module. A new duplexer, receiver amplifier, and a 17 MHz RF amplifier are needed to form the full system. A carrier board with DDS, ADC and Clock chips was built to interface the Zynq system on the MicroZed module. The new board provides the same functionality as the two digital (DSP and Transceiver) boards on the KEA system, this greatly reduced the size and cost of the digital system. A summary of the system design specification is shown in Table 5.2. The next section details the design of the new spectrometer hardware.

Table 5.2 Technical specifications of the full system design

Modules	Parameters	Values
Amplifier	Frequency, power	17 MHz, 30 W
Transceiver	Sample rate	100 Msps
Receiver	Frequency, gain	Broadband, 72 dB
Duplexer	Frequency	17 MHz, 500 kHz BW
Spectrometer	Size, weigh	Hand held, < 1 kg

5.5. The Digital Transceiver Carrier Board

The method of building this handheld NMR system is to make use of the new SoC systems available on the market, implementing the transceiver hardware with it and using the onboard processor for data processing. This is effectively replacing the functionality of the computer with an SoC module. Other supporting hardware needs to be developed for this to work and will be discussed next.

A carrier board was built to provide connections to the MicroZed module in order to use the processor and the IOs; it is an interface between the digital system on Zynq SoC and the analogue system (RF signals). An overview block diagram is shown in Figure 5.18. The board needs to output signals to the RF amplifier, therefore a DDS is used for signal generation. The NMR signal from the sensor is in analogue form so an ADC is needed at the input of the digital receiver. A dedicated clock chip is used for generating synchronised clocks for the system and to also provide a low jitter clock for the ADC sampling.

Figure 5.18 Overview block diagram of the carrier board

The ADC used in the design is a 16-Bit, 105Mps device manufactured by Linear Technology, LTC2207. While the Mini-MOUSE operates at 17 MHz, the desire here is to have a broadband digital system that enables future development. This broadens the application of the NMR system when other sensors working at higher frequencies become available in the future. There are other devices that can be used, the selection criteria here is to have 16-Bit resolution and fast enough to sample an input analogue signal of up to 50 MHz. The input RF signal on this system is unlikely to be higher than 50 MHz as the operating frequency of the Class-D amplifier in the system is limited by the switching speed of the MOSFET devices available. The cost of a 16-Bit ADC with 100 Mps is similar to one with 40 Mps, so that is an

investment worth doing. The LTC2207 only require a single 3.3V supply, which is also very convenient to use. A schematic layout of the ADC is shown in Figure 5.19.

Figure 5.19 The ADC schematic connection diagram

Figure 5.20 The DDS schematic connection diagram

The design of the transmitter was aimed at a broadband design to match the 50 MHz design of the receiver. The transmitter device used is a 14-Bit, 400 Msps DDS, AD9951, manufactured by Analog Devices. The selection criterion for this device is to be able to generate a high precision analogue output of at least 50 MHz. While the required frequency in this design is lower, using a higher capability device is good for future system development. The difference in component cost is under 10 USD. A schematic layout of the DDS circuit is shown in Figure 5.20.

A dedicated clock chip, AD9513, is used as the clock source in the system. It is a three-output clock distribution IC with low jitter performance. Having the clock signal from the same source makes precise timing and phase control possible. A schematic layout of the clock chip circuit is shown in Figure 5.21.

Figure 5.21 Clock chip schematic connection diagram, all the clock outputs are 100 MHz

The IO lines for controlling the other modules are available through a 48-pin DIN connector, power supplies are also feed through this connector, A schematic layout of the connector is shown in Figure 5.22.

Figure 5.22 DIN schematic connection diagram

There are two sets of IO lines, IO_[0 to 7] and P[0 to 7]. The different labels are just indications that the lines are coming from different banks of the FPGA. The PMOD lines are

also available, PMOD_[0 to 7], they can be used for future development and connecting to other PMOD extension modules. One requirement on using the MicroZed board with a carrier board is that a power up sequence needs to be followed. That is the supply to the IO banks of Bank34 and Bank35 (VCCO_34 and VCCO_35) should be powered up last. The MicroZed module provides an enable line (VCCIO_EN) through Pin10 of microheader JX2. This pin is connected to P7 of the carrier board and will be used to control a power module on the power supply board. A full schematic of the design is shown in Appendix VII.

Figure 5.23 The carrier board for MicroZed module. Top side shows the microheaders and bottom side shows the ADC, DDS and clock components. PCB size: 110x62 mm.

The carrier board is laid out on a 4-layer PCB with two internal planes as power supply and ground planes. The track connections are on top and bottom layer. Having an internal ground plane can minimise noise pick up. Pictures of the top and bottom sides of the PCB are

shown in Figure 5.23. The carrier board with the MicroZed module attached is shown in Figure 5.24.

Figure 5.24 Carrier board with the MicroZed module attached

5.6. Power Supply and RF Amplifier Board

The 17 MHz Class D RF amplifier as described earlier in Chapter 4.2 was redesigned to fit onto one board with the power supplies. This is also a power supply board as it provides all the different voltages to the digital boards. A block diagram is shown in Figure 5.25.

Figure 5.25 Block diagram of the RF amplifier and power supply board

The voltages required for the SoC system are 5 V, 3.3 V and 1.8 V. The nominal input to the system is 24V and switch mode regulators were used to convert it to the required levels. The LMZ series regulators manufactured by Texas Instrument were used in the design and they are the recommended power supply sources for the MicroZed board. Power supply to

the IO banks of Bank34 and Bank35 are controlled by a power up signal, P7, as shown in Figure 5.26. Other digital power supplies (3.3 V and 1.8 V) do not require power up control and the Enable pins are tied to the supply input. The full power supply schematic is shown in Appendix VIII.

Figure 5.26 IO bank power supply with power up enable line P7

The three logic control lines, TTL, Enable, and Gate (as described in Chapter 4.2) used to control the RF amplifier are now coming from the carrier board through the back plane connector, labelled as IO_0, IO_1, IO_2 respectively. A schematic showing those lines is in Figure 5.27.

Figure 5.27 Digital control lines for the Class D RF amplifier, IO_0, IO_1, IO_2

The power supply to the RF amplifier needs both 24V and 16V supply for amplitude modulation and the same power supply design as in Chapter 4.2 is used. A separated 5V supply is used to supply the logic ICs and the isolators. This single board has the functions of both the Power Supply and RF Amplifier boards combined on the KEA system. A picture of this board is shown in Figure 5.28.

Figure 5.28 Power Supply and RF Amplifier board (110x62 mm)

5.7. Duplexer and Receiver Amplifier Board

The duplexer and receiver amplifier board design was based on the existing Duplexer module and Receiver Amplifier module on the KEA system. The goal was to provide the same functions but with reduced size. The signal and power flow of the duplexer system is illustrated in a block diagram in Figure 5.29. The main components are the directional coupler and three amplifier blocks.

Figure 5.29 Block diagram of Duplexer and Receiver Amplifier

The duplexer consists of a quarter-wave line, some diodes and a directional coupler as shown in Figure 5.30. The PI network formed by C3, C4, L1, C5 and C6, is the equivalent of a quarter-wave line at the resonance frequency of 17 MHz. During transmit the high power RF pulse comes in through J2, the bidirectional diode D2 on the right hand side of the quarter-wave line conducts and acts like a short circuit termination, resulting in a high impedance path looking into the PI network. Therefore all the RF power goes to the sensor/probe and excites the sample. Once the RF pulse is turned off, the NMR signal coming back from the sensor is in the micro-volt scale, and is not enough to turn on either diodes D1 or D2. Therefore it goes through the directional coupler (“out” pin) and into the receiver amplifier stages.

Figure 5.30 Duplexer circuit

The NMR signal has to be amplified before it can be captured by an ADC. For the MOUSE, a 70 dB gain is needed as shown by the KEA system. This design uses three cascaded stages of wideband amplifiers. The first amplifier in the system is a BFR360F based amplifier with 20 dB gain and providing impedance matching to 50 ohms. A schematic of this amplifier is shown in Figure 5.31.

Figure 5.31 BFR360F based wideband amplifier [72].

It replaces the Miteq amplifier module used in the existing duplexer design; this reduced the component cost and overall size of the duplexer and still provides enough signal gain. The Miteq amplifier has a noise figure (NF) specification of 1dB. The BFR360F based design has a NF of 1.2 dB as measured on a network analyzer [10]. The Miteq amplifier module costs 600 USD and the BFR360F based amplifier costs less than 10 USD.

The second amplifier is based on the AD8369 IC; it is a proven working design from the existing KEA receiver amplifier, Figure 5.32. The variable gain control is done by the three input lines P0, P1, and P2 controlling the Bit0, Bit1 and DENB serial input pins of the IC using serial gain mode. Those lines are controlled by the program in the FPGA. Using a variable gain at this stage allows the adjustment of the total gain the system needs. The AD8369 has a maximum gain of 35dB and it is adjustable digitally in 3 dB steps.

Figure 5.32 Second stage amplifier based on AD8369.

The third stage amplifier is a fixed 26 dB gain MMIC, BGM1013. A fixed gain module is used here because no more gain adjustment is needed and it simplifies the design. The BGM1013 requires only a few supporting components and has enough gain needed for the system, Figure 5.33. Combining the three stages gives an overall maximum gain of 81 dB. That is more than the gain needed for the MOUSE. To have a 70 dB gain, the variable gain amplifier is adjusted to 26 dB gain to give a total of 72 dB. The variable gain amplifier is adjustable in steps of 3 dB, so either 69 dB or 72 dB can be used for the MOUSE.

Figure 5.33 Third stage amplifier based on BGM1013

Another function of the duplexer is to provide the ability to do a Wobble experiment for finding the resonance frequency of a sensor. The directional coupler allows a low power RF signal to be fed to the MOUSE, this makes the Wobble experiment possible as it works by measuring the reflected power from the sensor. A low power signal in the range of -60dB is sufficient as the over gain of the receiver amplifiers is more than 70 dB. However the transceiver is not able to output a signal as low as -60 dB, therefore an attenuator is needed to reduce the input RF power for Wobble. A two port output network with 1 dB and 25 dB attenuations is used and shown in Figure 5.34.

Figure 5.34 Power divider network for 1 and 25 dB division

The top output port to RF Amp (RF_2) has 1dB attenuation and it is connected to the input of the Class D RF amplifier. The bottom output (RF_1) has 25 dB attenuation and it is connected to the directional coupler as input for doing Wobble. During Wobble the Class D RF amplifier is disabled by the TTL control lines therefore even though there is a signal on the input, there is no high power pulse at the output. The receiver amplifiers are broadband designs but the MOUSE sensor is only at 17MHz, therefore a low pass filter (LPF) is used at the receiver output. The LPF used in here is PLP-21.4 from Mini Circuits. It has a cut off

frequency at 21.4 MHz. All the components used in circuits described are housed inside a tinned box to provide noise shielding. A Full schematic of the design is shown in Appendix IX. A picture of the PCB is shown in Figure 5.35 with the Tin box cover removed to show the inside.

Figure 5.35 Duplexer and Receiver Amplifier board (110x62 mm)

5.8. Backplane Board

Since the system is designed in modular form, a back plane is needed to connect all the modules together. This is done on another 4-layer board with three matching Mini-DIN connectors for connecting to the three modules. The tracks linking the connector pins are laid out in the middle layers of the PCB and ground planes are on the top and bottom layers; this provides good shielding for the tracks. The 48-pin DIN connector has three rows (a,b,c) of 16-pins, each row connection is shown in Figure 5.36.

Figure 5.36 Schematic connections of a 48-pin DIN connector on backplane

The three connectors have the same connection, ie, connected in parallel, this allows the modules to plug into any connector. A picture of the backplane board is shown in Figure 5.37. With all the PCB modules built, putting them together gives an idea of how big the actual system would be. Figure 5.38 shows all the modules plugged into the backplane, measuring approximately 130x110x62 mm (LxWxH).

Figure 5.37 Backplane board (110x62 mm)

Figure 5.38 The mobile system hardware, measuring approximately 135x110x62 mm (LxWxH)

5.9. System Integration and Testing

Having the PCB modules built completes the first step in developing the full system hardware, the next step is testing. The KEA system with Prospa was first used for testing the power and high power RF part of the system; a successful signal acquisition in this setup would be a good indication that the new hardware is functioning. The digital part of the system requires the development of new interface software and pulse sequences; these will be discussed in this chapter.

5.9.1. Testing the Power, RF Amplifier, Duplexer and Receiver Amplifier Boards

The high power part of the system was first tested using control lines from the KEA; that is using the RF signals coming out of the KEA transceiver board to drive the new RF amplifier directly. The logic control lines to the new Duplexer and receiver amplifier were also coming from the KEA through the D-connector on the receiver amplifier board, a picture of the experiment setup connecting to the MOUSE probe is shown in Figure 5.39. Both the MOUSE and the home made Aluminium box sensor were used in testing.

Figure 5.39 Setup for testing the new PCB modules using KEA control signals

First a Wobble experiment was run to test the duplexer and receiver amplifier board. The aluminium box sensor was used here and Prospa shows a resonance frequency of 17.1 MHz, Figure 5.40.

Figure 5.40 Wobble output from the Aluminium box probe on Prospa

The resonance frequency of the Aluminium box sensor was measured again using a network analyzer, it was also 17.1 MHz, Figure 5.41, it agrees with the values from Prospa. This is an indication that the duplexer and receiver amplifier board is working.

Figure 5.41 Network analyzer output for the Aluminium box probe

Measurements on the output of the RF amplifier from a CPMG sequence shows similar signals to the ones in Figure 4.26 of Chapter 4 earlier, this indicates that the new amplifier board is working, Figure 5.42.

Figure 5.42 New amplifier output on MOUSE

An NMR signal was then acquired in Prospa. Figure 5.43 shows a good CPMG signal from the box sensor and shows similar amplitude and decay shape to the results shown in Figure 4.28 of Chapter 4 earlier. This shows that the stability of the amplifier board is good and the receiver amplifier gain control is also working. Hence the high power and receiver parts of the new system are confirmed to be working.

Figure 5.43 CPMG echo data from Aluminium box probe

5.9.2. Testing The Digital System

The digital part of the system involved both hardware and software. First the Zynq processor and FPGA need to be configured using Vivado, then software pulse sequences need to be developed using SDK and user interface software is also needed to drive the full system.

The digital system in Vivado has been developed by our research group previously and part of it was based on the KEA system. The development of all the IP blocks (Zynq SoC, ADC, DDS, etc) used in Vivado is not part of this work, my task here is to use the existing IP blocks and configure them to represent my new design, and develop the pulse sequences needed in SDK to drive the whole system. The system in IP blocks is as shown in Figure 5.44.

Figure 5.44 The full system in IP block connections

The IP block representations of the DDS and ADC in the Vivado design are there to provide the interface connections to the FPGA only, the actually function is still performed by the real components. The IP block connection interface for the ADC (LTC2207) is shown in Figure 5.45. There are control lines for Clock, SHDN, DITH, RAND, etc, as on the actual component. Similarly for the DDS (AD9951), the block connection interface is shown in Figure 5.46.

Figure 5.45 Block connection interface of ADC in Vivado

Figure 5.46 Block connection interface of DDS in Vivado

The user IO lines for controlling the Duplexer gain (P[7:0]), RF amplifier and power module (IO[7:0]) are set inside the TTL interface block, Figure 5.47. The TTL control lines for the ADC and DDS are also coming from this IP block.

Figure 5.47 Block connection interface of TTL lines Vivado

The digital receiver IP block consisting of the two digital multipliers and decimating (CIC) low pass filters is shown in Figure 5.48.

Figure 5.48 Digital receiver IP block

Apart from the main ARM processor, our research group has implemented a soft processor, MicroBlaze, to run in the FPGA fabric, this IP block is shown in Figure 5.49. The MicroBlaze processor runs the pulse sequence code and controls the DDS and digital receiver blocks as well as the TTL outputs.

Figure 5.49 MicroBlaze IP block

The data busses of the IP blocks and MicroBlaze are connected by the AXI interconnect IP block as shown in Figure 5.50. This IP block configures a high speed AXI data bus and is an IP block from the Xilinx library.

Figure 5.50 Block representation of AXI Interconnect in Vivado

The Zynq peripheral IOs are configured to use UART1, GPIO, SD0, USB0, and ENET0. This is shown with a "tick" next to the IO in Vivado, Figure 5.51.

Figure 5.51 Zynq Peripheral IOs

The memory spaces in the system (1G DDR3 + 512K BRAM) are divided into sections for Linux OS, Instructions, Data, Parameters and Registers. A memory map [73] is shown in Figure 5.52. Configuration of the address spaces in Vivado is shown in Figure 5.53.

Figure 5.52 Memory map

Cell	Interface Pin	Base Name	Offset Address	Range	High Address
processing_system7_0					
Data (32 address bits : 4G)					
microblaze_ppu/microblaze_0_local_memory/...	S_AXI	Mem0	0x40000000	32K	0x40007FFF
microblaze_ppu/microblaze_0_local_memory/...	S_AXI	Mem0	0x40008000	32K	0x4000FFFF
microblaze_ppu/microblaze_0_local_memory/...	S_AXI	Mem0	0x40020000	128K	0x4003FFFF
microblaze_ppu/pp_reset	S_AXI	Reg	0x41000000	4K	0x41000FFF
microblaze_ppu/microblaze_core/mailbox	S1_AXI	S1_AXI_Reg	0x41001000	4K	0x41001FFF
ddc/dma_con					
Data_S2MM (32 address bits : 4G)					
processing_system7_0	S_AXI_HP0	HP0_DDR_L...	0x30000000	256M	0x3FFFFFFF
microblaze_ppu/microblaze_core/microblaze_0					
Data (32 address bits : 4G)					
microblaze_ppu/microblaze_0_local_memory/...	SLMB	Mem	0x00008000	32K	0x0000FFFF
microblaze_ppu/microblaze_0_local_memory/...	SLMB	Mem	0x00020000	128K	0x0003FFFF
microblaze_ppu/microblaze_core/axi_intc_0	s_axi	Reg	0x41200000	64K	0x4120FFFF
microblaze_ppu/microblaze_core/mdm_1	S_AXI	Reg	0x41400000	4K	0x41400FFF
microblaze_ppu/microblaze_core/axi_timer_0	S_AXI	Reg	0x41C00000	64K	0x41C0FFFF
DDS_AD9951/dds_spi	AXI_LITE	Reg	0x42000000	4K	0x42000FFF
DDS_AD9951/dds_outputs	S_AXI	Reg	0x42001000	4K	0x42001FFF
ADC_LTC2207/axi_gpio_0	S_AXI	Reg	0x42100000	4K	0x42100FFF
TTL/gpio_ttl	S_AXI	Reg	0x42300000	4K	0x42300FFF
ddc/dma_con	S_AXI_LITE	Reg	0x42400000	64K	0x4240FFFF
ddc/gpio_DDS	S_AXI	Reg	0x42410000	64K	0x4241FFFF
ddc/gpio_DDC_fifo	S_AXI	Reg	0x42420000	64K	0x4242FFFF
ddc/gpio_DDC_control	S_AXI	Reg	0x42430000	64K	0x4243FFFF
microblaze_ppu/microblaze_core/mailbox	S0_AXI	S0_AXI_Reg	0x43600000	64K	0x4360FFFF
Instruction (32 address bits : 4G)					
microblaze_ppu/microblaze_0_local_memory/i/...	SLMB	Mem	0x00000000	32K	0x00007FFF

Figure 5.53 Memory address configuration in Vivado

In this hardware design dual port memory is used between the ARM and MicroBlaze processors. In order to manage data movement from the Linux OS to control the MicroBlaze, a program called "pulse" is used; this program was developed by our research group previously. Not to be confused with the actual NMR pulse sequence, this "pulse" program has four main functions: to read and write to the MicroBlaze accessible memory, and to run or stop the MicroBlaze processor. The "pulse" program is essentially an "interface layer" that can be used as an API to load and execute MicroBlaze payload code. The actual NMR pulse sequence code talks directly to the peripheral hardware and runs solely from the MicroBlaze, this guarantees synchronous execution of the code because it runs directly on bare-metal without any OS overheads. Development of the pulse sequence is done in the next section.

5.9.3. Full System Testing And Pulse Sequence Development

Once the hardware development is completed in Vivado, a board support package (BSP) file that contains system memory maps and register spaces is exported into the SDK. SDK helps manage projects and connections to the hardware platform using a variety of methods. In our implementation the Zynq processor runs a Linux operating system on the

dual Core ARM A9 processor and a soft-core MicroBlaze processor runs in the FPGA fabric. SDK helps manage the compilation process to target different platforms whether it is Linux or MicroBlaze.

Xilinx SDK provides remote access through the ethernet port to the development platform using a secure shell (ssh) link to the target OS. It provides remote debugging capabilities using gnu project debugger (gdb) by running a gdb server on the target platform. Thus making code development and debugging straight forward. Once the code development is complete the programs are packaged using Petalinux into a root file system.

To test the digital part of the new system and to develop pulse sequences, a sensor with strong SNR is needed. This was done using a Cryogen free superconducting magnet available in the lab, Figure 5.54. The magnet system was adjusted to work at 17.3 MHz to have similar frequency to the MOUSE.

Figure 5.54 Cryogen free superconducting magnet system

The control of the RF output from the DDS for driving the RF amplifier is not in dB units, instead it is using a number between 0 and 1 with 0 being no output and 1 being maximum output from the DDS. Therefore it was necessary to measure the amplifier output directly to calibrate the output power. A simple two pulse sequence was used in this calibration; it has both the 90 and 180 degree pulses, timing of the pulses are not critical at this point as it is doing an amplitude calibration task only. To match the KEA output settings of -10 dB for 90 degree pulse and -4 dB for 180 degree pulse in Prospa, the parameters were found to be 0.75 units for the 90 degree pulse and 0.65 units for the 180 degree pulse. Note that the power supply rails on the amplifier are separated for the two pulses, with the higher voltage rail on for the 180 degree pulses. Therefore there is no correlation between the two amplitude setting parameters of 0.75 and 0.65 units. An extraction of the source code from SDK is shown below for the pulse frequency and amplitude settings.

```
void testPulse(p_mem_t * pMem)
{
    ...
    // TxRx frequency, MHz
    pMem->pulse.freqTx = 17.33;           // float
    pMem->pulse.freqRx = pMem->pulse.freqTx;
    // Set amplitude
    //P90 pulse
    pMem->pulse.A90 = 0.75;               // float, 0 to 1
    //P180 pulse
    pMem->pulse.A180 = 0.65;             // float, 0 to 1
    ...
}
```

The amplifier output into a 50 ohm load is shown in Figure 5.55. The RMS power of the 180 degree pulse is 30 Watt.

Figure 5.55 RF amplifier output calibration using a 50 ohm load

The first pulse sequence developed was the single RF pulse sequence for getting an FID. The FPGA system uses time delays between pulse events and the way it is done can be explained using Figure 5.56. T1 is the length of the RF pulse; T2 is the time delay after the RF pulse turns off and before the ADC starts data acquisition; T3 is the time length of data acquisition. The flow diagram of the pulse sequence is shown in Figure 5.57. During T1, only the DDS and the RF Amplifier outputs are switched on. All devices are on standby during T2, and during T3 the ADC and Transceiver are switched on.

Figure 5.56 FID one-pulse timing diagram

Figure 5.57 Flow diagram of a FID sequence

The pulse sequence starts by declaring and initialising the pulse parameters such as number of scans to run, the number of echoes, pulse frequency and timing, etc. A code snippet is shown below:

```
pMem->pulse.Avg = 32;           //Number of averages
pMem->pulse.NLoops = 128;        //Number of echoes
pMem->pulse.IgnoreSamples = 7;   // set to 7 to ignore all ramp up
pMem->pulse.Samples = 32;        //Number of points in each echo

pMem->pulse.freqTx = 17.33;      //Tx frequency
// DSP receive processor
pMem->pulse.Dec = 50;            // 50 for 2MHz sampling
pMem->pulse.freqRx = pMem->pulse.freqTx;
pMem->pulse.phaseRx = 0;         // 0-360 float
//P90 pulse
pMem->pulse.P90 = 90.0;          // float 90.0
pMem->pulse.A90 = 0.75;          // float, 0 to 1
// pulse timing
pMem->pulse.T1 = 14000;           // nano seconds
pMem->pulse.T2 = 500000;          // nano seconds
pMem->pulse.T3 = 12000000;        // nano seconds
pMem->pulse.Tend = 1000000000;    // nano seconds
```

For the Cryogen free superconducting magnet working at 17.33 MHz, the one-pulse timing parameters were found to be as follows:

T1 = 14 us
T2 = 0.5 us
T3 = 12000 us

Peripheral hardware is initialised as follows:

```
// default variables
u32ttl = 0;
u32 adc_run = ADC_RAND | ADC_DITH | ADC_PGA; // high
u32 adc_other = 0;
u32dds = 0;
u32dsp = 0; // dsp is the transceiver

ttl_set(ttl | TTL_P2); // TTL to zero apart from TTL_P2
rxa_set(12);           //set receiver gain
adc_set(adc_other | adc_run); // turn ADC on
dds_set(dds);          // set DDS to zero
dsp_set(dsp | DSP_DDS_RESET | DSP_CIC_RESET); // reset TxRxerdds&cic
```

Phase Cycling parameters set as follows:

```
float Pcycle90[] = {180, 0, 180, 0};
float PcycleRx[] = {90, 270, 90, 270};
```


The pulse parameters are update as follows:

```
// T90 pulse parameters set
dds_write_ASF(ASF_T90);
dds_write_FTW(FTW_TX);
dds_write_FOW(POW_T90);
dds_ioUpdate(dds);           // IO UPDATE to put spi settings in memory
```

Outputting the RF and turning the RF amplifier on is done as follows:

```
// T90
ttl_set(ttl | TTL_IO_0 | TTL_P2 );           //enable RF amp
timer_set_ns(0, pMem->pulse.T90, (TMR_AUTO_RELOAD | TMR_START));
// TX A90 pulse
ttl_set(ttl | TTL_IO_0 | TTL_IO_2 | TTL_DDS_SWT_EN | TTL_P2 ); //start
```

After some time the RF is then turned off. After another delay the data capturing process is started by turning on the ADC as follows:

```
timer_set_load_ns(0, pMem->pulse.T2); // Set T2
// clear CIC, latch in data
dsp_set(dsp | DSP_CIC_DEC_SET | DSP_CIC_DEC_SHIFT_SET | TTL_DDS_SWT_EN);
dsp_set(dsp); // update to default
timer_wait(0); // T2 - wait
timer_set_load_ns(0, pMem->pulse.T3); // Set T3
// Get ready for data
fifo_reset();
//Start ADC
timer_wait(0); // throw error if timer times out
ttl_set(ttl | TTL_IO_0 | TTL_IO_1 | TTL_ADC_RUN | TTL_P2 ); //start ADC
```

After the NMR data is captured, it then needs to be transferred from the digital receiver FIFO to the shared memory space.

```
// Capture data
int j, data;
for(j=0; j < pMem->pulse.IgnoreSamples; j++) {
    read_FifoStream(data); read_FifoStream(data);
}
for(j=0; j < pMem->pulse.Samples; j++){
    read_FifoStream(data);           //Get Real data
    *(ptrData++) = data;             //Write Real data
    read_FifoStream(data);           //Get Imag data
    *(ptrData++) = data;             //WriteImag data
}
```

At the end of the sequence, the status flag is updated to stop the sequence from running again.

```
pMem->status.action = action_finished;
```

To execute the sequence, it was first compiled in SDK, and then the resulting “.elf” file is transferred to the MicroBlaze memory by running the “pulse” program described earlier in ssh using the “run” command. After execution the data can be read and written to a csv file named “output_x.csv” and stored on the “root” directory of the linux system by running this command:

```
read -f root/outputp_x.csv -m u -a 0x20100 -l 0x8000
```

This reads 4000 points starting at the memory location 0x20100 and writes the data into a file. Pulse execution can be stopped anytime by running the “stop” command.

5.9.4. A Web Interface

To have the system operating without the use of a computer, it is possible to control the system through a webpage interface on a mobile device such as an iPad. The Zynq SoC system has a built-in Linux web server; this allows the communication through an internet connection. The system was designed to be controlled by an iPad using Wifi; however the USB driver for the Wifi module intended to be used with the spectrometer is not yet fully implemented for the PetaLinux system, therefore the system was test using an external Wifi router with the iPad. This was done by using a router with both the Wifi and Ethernet cable connections. The router was setup as a DHCP host with IP address of 192.168.0.1. The spectrometer connects to the router via cable using a static IP address 192.168.0.2; the iPad connects via Wifi and obtains a dynamic IP address. Static IP is used for the spectrometer so the web server can be accessed using the same IP address after power reset. An illustration of the connection is shown in Figure 5.58.

Figure 5.58 Network connection for the NMR system

A webpage was designed to provide the basic functions of running the system. There are two experiments for the Mini-MOUSE, CPMG and Wobble. The web interface displays the NMR data in real time and allows pulse sequence data adjustments for data analysis and curve

fitting to find T_2 . A flow diagram of the actions of the buttons is shown in Figure 5.59. A screenshot of the web interface is shown in Figure 5.60.

Figure 5.59 Flow diagram of the Web user interface

Figure 5.60 The Web interface displayed on iPad

The web interface was written in java script and hosted on the web server directory of the Linux system. On load, the web interface presents the buttons (CPMG and Wobble) for running the experiments. Once an experiment button is pressed a shell script is called "runpulse.sh" (See code snippet below), which will deliver the NMR pulse sequence payload to the MicroBlaze, start the processor and then write the acquired data to a file, which is then processed and displayed on a browser. There are three radio-buttons for selecting different options of displaying the CPMG data, same as the options available in Prospa: AutoPhase, CPMG Add and CPMG Int. The AutoPhase options maximized the real data; the CPMG Add option displays the summation of all echo data for each point; the CPMG Int option displays the integral of the echo points for each echo and a single exponential fit finds T_{2eff} .

```
#Configure Variables
UBLAZE_BIN=/home/root/bin/pulse
ELFLIB=/home/root/lib/uSpec_uBlaze
DATA_DIR=/home/httpd
UPTIME=`uptime`

# Log execution start time
echo "Pulse Run Evidence since uptime:"$UPTIME>>pulserun.txt

# Stop uBlaze before writing to programm memory
```

```

$UBLAZEBIN stop
# Write ELF payload file to uBlaze memory
$UBLAZEBIN write-elf -f $ELFLIB/CPMG.elf

echo "Run Pulse"
# Pause script for 1 second
sleep 1
#execute payload from uBlaze memory
$UBLAZEBIN run
# Wait for the program to complete
sleep 32
# Read acquired data from uBlaze memory space starting at 0x20100, 0x8000 long
$UBLAZEBIN read -f $DATA_DIR/outputp_x.csv -m u -a 0x20100 -l 0x8000>/dev/null
sleep 1
#Stop uBlaze operation
$UBLAZEBIN stop

```

The web application calls “runpulse.sh” in the “cgi-bin” directory using the “get” function in the “jQuery” library, it is an open source javascript library.

```
jQuery.get("cgi-bin/runpulse.sh");
```

To test the interface, the “.elf” from an FID sequence was placed in the ELFLIB directory and called by the “runpulse.sh” when the CPMG button is pressed. This is because the web interface does not have a FID button. Once a pulse sequence is executed, the data file is read by the browser using the “ajax” function in the jQuery library, the data was first split into two arrays of real and imaginary data, then passed to the plotting function for display.

```

$.ajax({
  type: "GET",
  url: "outputp_x.csv",
  dataType: "text",
  success: function (data) {
    rows = data.split("\n");
    var x = 0;
    for (var i = 0; i < rows.length - 1; i++) {
      if (i % 2 == 0) {
        real_data.push((parseFloat(rows[i].split(",")[1]))*scale_factor/scans);
        x = x + 1;
        x_data.push(x);
      }
      else {
        imag_data.push((parseFloat(rows[i].split(",")[1]))*scale_factor/scans);
      }
    }
  } // End of reading file, close the For loop

```

The jQuery library has a plotting function that can plot multiple data sets and it is used in here for plotting both the real and imaginary data on the same graph. There are options for axes labels and legends.

```

plotdata = [
    {label: "Imaginary", data: imaginerydata, color: '#ff9933'},
    {label: "Real", data: realdata, color: '#0000e6'}
];
$.plot($("#placeholder"), plotdata, {
    xaxis: {
        axisLabel: x_label,
        axisLabelUseCanvas: true,
        axisLabelFontSizePixels: 14,},
    yaxis: {
        axisLabel: y_label,
        axisLabelUseCanvas: true,
        axisLabelFontSizePixels: 14,},
    series: {lines: {show: true }, },
    legend: {
        labelBoxBorderColor: "#ffffff",
        position: "right"
    }
});

```

The output captured by the web interface on an iPad from the cryogen free magnet system is shown in Figure 5.61. Note that the voltage amplitude scale of the display is not calibrated at this time. Although the exact amplitude of the signal is not known, it is clear that this is an NMR signal and it shows that the digital part of the system is working.

Figure 5.61 FID data from the cryogen free magnet system

The next pulse sequence developed was the spin echo sequence that consists of two RF pulses. The timing diagram is shown in Figure 5.62 and a flow diagram for the sequence is shown in Figure 5.63.

Figure 5.62 Spin echo sequence timing diagram

Figure 5.63 Flow diagram of a Spin echo sequence

The Spin echo sequence is very similar to the FID sequence, apart from the addition of the 180 degree pulse. The time parameters of the spin echo sequence for an echo time of 5 ms is as follows:

$$T_{90} = T_{180} = 14 \text{ us}$$

$$T_1 = 2486 \text{ us}$$

$$T_2 = 2365 \text{ us}$$

$$T_3 = 2621 \text{ us}$$

```
pMem->pulse.T90 = 14000;
pMem->pulse.T1= 2486000;
pMem->pulse.T180 = 14000;
pMem->pulse.T2 = 2365000;
pMem->pulse.T3 = 2621000;
```

The output capture by the web interface on an iPad is shown in Figure 5.64. As before, the voltage amplitude scale of the display is not calibrated.

Figure 5.64 Spin echo data from the Cryogen magnet system

The MOUSE has very low SNR compared to the Cryogen free magnet, therefore signal accumulation and averaging will be required, this is done inside the FPGA.

The NMR data was captured, an averaging operation was performed, and then the result written to memory space. Averaging is done by first reading the old value in memory space, adding it to the new value, then saving the sum to the same memory space.

```
// Capture data
int j, data;
int avgdata, tmpdata;
// Throw away ignoresamples
for(j=0; j < pMem->pulse.IgnoreSamples; j++) {
    read_FifoStream(data); read_FifoStream(data);
}
// Grab samples
for(j=0; j < pMem->pulse.Samples; j++){
    read_FifoStream(data);           //Get Real data
    avgdata = data + *ptrData;
    *(ptrData++) = avgdata;          //Average Real data
    read_FifoStream(data);           //Get Imag data
    avgdata = data + *ptrData;
    *(ptrData++) = avgdata;          //Average Imag data
}
```

To show if the signal accumulation is working, an acquisition from four scans is shown in Figure 5.65. The signal amplitude is now four times bigger which suggests that the accumulation is working.

Figure 5.65 Spin echo data accumulated from 4 scans on the Cryogen magnet system

Knowing that the new hardware is working and the signal accumulation for averaging is also functioning, the next step is to calibrate the display to show the actual signal amplitude. System calibration is done by feeding a known amplitude signal (180 mV) into the input of the

ADC port, reading the corresponding output from the system (80 million), then scale the system output to display the correct voltage in micro volts using the equation:

$$V_{actual} = Input * \frac{V_{in}}{V_{out}} * 10^{\left(-\frac{G}{20}\right)} \quad (9)$$

where Input is the value to be calibrated, V_{in} is the input calibration voltage (180 mV), V_{out} is the corresponding output (80 million), G is the system gain, 71 dB.

The calibrated output from the same spin echo experiment is shown in Figure 5.66, the signal amplitude shown agrees with the same experiment from Prospa using KEA system.

Figure 5.66 Calibrated spin echo output from the Cryogen magnet system

The final pulse sequence implemented was the CPMG sequence. This sequence has the same timing parameters as the spin echo but with the number of 180 degree pulses repeated many times, a code snippet is shown below.

```
int n;
for(n=0; n < pMem->pulse.NLoops; n++)
{
    // T180
    timer_wait(0); // throw error if timer times out
    //start 180 RF
    ttl_set(ttl | TTL_IO_0 | TTL_IO_1 | TTL_IO_2 | TTL_DDS_SWT_EN | TTL_P2 );
    timer_set_load_ns(0, pMem->pulse.T2); // Set T2
    // clear CIC, latch in data
    dsp_set(dsp | DSP_CIC_DEC_SET | DSP_CIC_DEC_SHIFT_SET | TTL_DDS_SWT_EN);
    dsp_set(dsp); // update to default
    // T2 - wait
    timer_wait(0); // throw error if timer times out
}
```

```

t1l_set(t1l | TTL_IO_0 | TTL_IO_1 | TTL_P2 ); //end 180 RF
timer_set_load_ns(0, pMem->pulse.T3); // Set T3
// Get ready for data
fifo_reset();
// T2 - Start ADC
timer_wait(0); // throw error if timer times out
t1l_set(t1l | TTL_IO_0 | TTL_IO_1 | TTL_ADC_RUN | TTL_P2); //start ADC,
timer_set_load_ns(0, pMem->pulse.T180); // Set T180

// Capture data
t1l_set(t1l | TTL_IO_0 | TTL_IO_1 | TTL_P2); // turn ADC off
// -----
// T3 - next loop
}

```

A flow diagram showing the pulse repetition is shown in Figure 5.67. A CPMG output from this sequence with 128 echoes is shown in Figure 5.68.

Figure 5.67 Flow diagram showing the repetition of 180 degree pulses in CPMG

Figure 5.68 CPMG output from the Cryogen magnet system

The small humps along the decay curve is due to the shape of the truncated echoes. The results from the Cryogen free magnet for the implemented CPMG sequence shows that the full system is working. The next step is to test the full system using the Aluminium box sensor to see if the results agree with results from the KEA system earlier.

5.9.5. Full system Testing Using The Aluminium Box Sensor

The pulse sequence for Wobble is implemented next as that allows the system to find the resonance frequency of the sensor. Wobble measures the reflection from the sensor over a range of frequencies, a flow diagram for the sequence is shown in Figure 5.69.

Figure 5.69 Flow diagram of a Wobble sequence

The Wobble sequence differs from other sequences because it is doing a frequency sweep. This means the output frequency changes compared to fixed frequencies on other sequences. New parameters in this sequence are the sweep span and step size, a code snippet is shown below.

```
// Sweep setup
double span = 2; //MHz
double step = span/pMem->pulse.NLoops;

int n;
for(n=0; n < pMem->pulse.NLoops; n++)
{
    //Frequency Sweep
    FTW_TX = dds_convertFTW(pMem->pulse.freqTx-span/2+step*n); // MHz
    FTW_RX = dsp_ConvertFTW(pMem->pulse.freqTx-span/2+step*n); // MHz
    dsp_dds_freq(FTW_RX); // set ADC freq
    dds_write_FTW(FTW_TX);
    dds_ioUpdate(dds); // IO UPDATE to put spi settings in memory

    // Wait for SPI ~50ns
    timer_set_ns(0, 50, (TMR_AUTO_RELOAD | TMR_START)); //set next wait time
    timer_wait(0); // throw error if timer times out

    ttl_set(ttl| TTL_DDS_SWT_EN | TTL_P2 ); //start RF
    // clear CIC, latch in data
    dsp_set(dsp | DSP_CIC_DEC_SET | DSP_CIC_DEC_SHIFT_SET| TTL_DDS_SWT_EN);
    dsp_set(dsp); // update to default
}
```

Output from a Wobble on the Aluminium box sensor is shown in Figure 5.70. The centre frequency is at 17.032 MHz, a frequency sweep from a spectrum analyzer gives 17.029 MHz, which is very close to the Wobble value.

Figure 5.70 Wobble experiment on the Aluminium box sensor

A CPMG sequence with 128 echoes and 100 μs echo time was used, the raw echo data is shown in Figure 5.71. The $T_{2\text{eff}}$ decay curve is shown in Figure 5.72 and a curve fit calculates $T_{2\text{eff}}$ to be 4.08 ms. This value is close to the value of 4.23 ms as obtained by the KEA system and shown in Figure 4.19 earlier.

Figure 5.71 CPMG experiment on the Aluminium box sensor

Figure 5.72 $T_{2\text{eff}}$ decay curve from the CPMG Int experiment on the Aluminium box sensor

5.9.6. Full System Testing Using The MOUSE

The experiments performed on the Aluminium box sensor using the new system shows that system is fully functional. The next step is also the main goal of the project, which

is to work with the MOUSE. The MOUSE has a resonance frequency of 17.3 MHz when loaded with a sample as measured by a network analyzer, Figure 5.73.

Figure 5.73 Resonance frequency of Mini-MOUSE sensor

The Wobble experiment finds the resonance frequency of the Mini-MOUSE at 17.33 MHz, Figure 5.74; and that is close to the value found by the network analyzer.

Figure 5.74 Wobble experiment on the MOUSE

The Mini-MOUSE is a low field single sided sensor, when looking at solid samples the NMR signal is weak and the duration is short, therefore experiments such as FID and Spin echo are not good enough to get a T_{2eff} measurement. Only the CPMG sequence is used on the Mini-MOUSE.

First the noise measurements were performed on a 50 ohm resistive load, FID acquisition shows that noise level is at 0.02 μV , Figure 5.75. When the Mini-MOUSE is connected to the system, noise level of 0.2 μV amplitude is observed. This value is ten times higher than the 50 ohm resistive load noise, Figure 5.76.

Figure 5.75 Noise measurements using a 50 ohm load

Figure 5.76 Noise measurements on MOUSE without shielding

The Mini-MOUSE used for testing is a prototype and the noise shielding is not optimal, later versions of the Min-MOUSE have better SNR. For testing the system a temporary shielding method is used on the Mini-MOUSE and that reduced the noise level. It is done by simply by putting the MOUSE inside an Aluminium tube and connecting it to the Mini-MOUSE ground, Figure 5.77.

Figure 5.77 MOUSE shielding inside an Aluminium tube

Figure 5.78 Noise measurements on Mini-MOUSE with shielding

With the shielding on, the noise level drops down to $0.03\ \mu\text{V}$; this is close to the 50 ohm resistive load noise level of $0.02\ \mu\text{V}$ and at an acceptable level, Figure 5.78. The system was not able to detect any NMR signal from rubber samples without the shielding; therefore all experiments on samples were done with shielding.

5.9.7. Testing of Industrial Materials

There were four rubber samples used for testing as shown in Figure 5.79. Measurements were done to test the operation of the system and not to find any particular properties of the individual samples. The rubber samples have different stiffness and are ordered from soft to hard in Table 5.3. The Echo Time parameter in the CPMG pulse sequence was adjusted from $100\ \mu\text{s}$ to $300\ \mu\text{s}$ to suit each sample according to the decay curve. Echo numbers were either 128 or 256; for samples with longer decay time, 256 were used. The experiment parameters are as follows:

Total scans: 1024
Echo Time: $100\ \mu\text{s}$ or $300\ \mu\text{s}$
Echoes: 128 or 256
Points per echo: 32
Sampling interval: $0.5\ \mu\text{s}$
Repetition time (between scans): 0.5 seconds

Figure 5.79 Rubber samples

Table 5.3 Summary of T_{2eff}

Samples	Description	Echo Time (μs)	T_{2eff} (ms)
A	Silicone pipe	300	50.0
B	Silicone rubber	300	43.0
C	Tyre rubber	100	2.16
D	Nitrile rubber	100	0.96

The raw experiment data from all those samples are shown from Figure 5.80 to Figure 5.87. The system was able to determine the T_{2eff} values for all the samples. The stiffer the sample the shorter the T_{2eff} .

Figure 5.80 CPMG data for Sample A – Silicone pipe

Figure 5.81 T_{2eff} decay curve for Sample A – Silicone pipe

Figure 5.82 CPMG data for Sample B – Silicone rubber

Figure 5.83 $T_{2\text{eff}}$ decay curve for Sample B – Silicone rubber

Figure 5.84 CPMG data for Sample C – Tyre rubber

Figure 5.85 $T_{2\text{eff}}$ decay curve for Sample C – Tyre rubber

Figure 5.86 CPMG data for Sample D – Nitrile rubber

Figure 5.87 T_2 decay curve for Sample D – Nitrile rubber

NMR technology has been used in the quality control of polymer manufacturing using T_{2eff} because it is directly related to the cross linking of the polymer molecules [74]. Here the system was tested on different compositions of silicone elastomers [75]. This will test the operation and sensitivity of the system. The Silicone elastomer is made of two liquid components, one is a base and the other is a curing agent. The mixing ratio is either by weight

or volume, curing agent to base. The four samples were cured for many days before the measurements were taken. The experiment parameters are shown below and a summary of T_{2eff} is shown in Table 5.4. A picture of the four samples is shown in Figure 5.88.

Experiment pulse parameters:

Total scans: 1024

Echo Time: 300 us

Echoes: 256

Points per echo: 32

Sampling interval: 0.5 us

Repetition time (between scans): 0.5 seconds

Table 5.4 Summary of T_{2eff} for four silicone elastomers

Sample (# as on label)	Composition	T_{2eff} (ms)
#1	1:10	15.25
#2	1:10	15.15
#3	1:20	16.19
#4	1:30	19.89

Figure 5.88 Four silicone elastomer samples

The T_{2eff} CPMG data with curve fitting is shown from Figure 5.89 to Figure 5.92. The T_{2eff} value is higher for softer samples and that is expected.

Figure 5.89 T_{2eff} decay curve for Sample #1

Figure 5.90 T_{2eff} decay curve for Sample #2

Figure 5.91 T_{2eff} decay curve for Sample #3

Figure 5.92 T_{2eff} decay curve for Sample #4

5.9.8. Reaction Monitoring

The final experiment done with the system was to monitor a Silicone curing process over 48 hours, measured every 15 minutes using an automatic timer to trigger the system to run. The silicone mixture used is the same material as in previous experiment, using a composition ratio of 1:10.

Experiment pulse parameters:

Total scans: 1024

Echo time: 300 us

Echoes: 256

Points per echo: 32

Sampling interval: 0.5 us

Repetition time (between scans): 0.5 seconds

The full data set for the 48 hours were curved fitted and the T_{2eff} values are plotted in Figure 5.93. It clearly shows the T_{2eff} is decreasing over time as the polymer is getting harder; starting with a T_{2eff} of around 56ms and ending with around 20 ms. This is a successful experiment and it shows that the stability of the system is very good over a 48 hour operation period.

Figure 5.93 T_{2eff} changes over time for Silicone mixture

Chapter 6. Discussion and Conclusions

The goal of this research was to develop high efficiency Class D amplifiers for mobile NMR applications, with the ambition of building a compact 17 MHz amplifier that would work with the newly developed Mini-MOUSE sensor, therefore giving the opportunity of building a full mobile NMR system. This section will now provide a summary and discussion of the important results of this research.

The operating frequency of a Class D amplifier is limited by the switching capability of the MOSFET devices. The availability of the MOSFET (CSD17313Q2) and driver IC (ISL55110) makes it possible for the Class D amplifier to operate up to 20 MHz with a resonant output setup. Their small device body makes them ideal to use for a compact design. However the voltage rating of the CSD17313Q2 is only 30 V on V_{DS} , which limits the power supply level and hence the power output.

The first amplifier built was a resonant output setup working at 2 MHz. The design was very straight forward with the only caution being setting the dead-time long enough for the devices to recover. Output power of 100 W with 90% efficiency is a lot better than the existing Class A amplifier used in mobile systems. This achieved the first milestone. The rise time of less than 1 μ s and ring down time of 3 μ s are well within the range needed for NMR applications. The output maintaining a constant level while doing 100 μ s pulses at 20% duty cycle is very good performance. The CPMG pulse sequence for this amplifier has fixed amplitude but the length of the 180 degree pulse is double the length of the 90 degree pulse. NMR test results from the Rock Core Analyzer system showed the decay curve from a water sample matches the one from the Class A amplifier. However there is an oscillation on the imaginary data which is a lot bigger than that of the Class A amplifier (Figure 3.29). While this amplifier worked well, there is a drawback of not being able to change amplitude, which means it cannot be used on other sensors that require less than 100 W of power.

The second amplifier built used a simple amplitude modulation technique, which is changing the width of the driving pulse with one pulse for each half cycle of the signal. The circuit design for this amplifier is more complex with a new dead-time control circuit. The change of output circuit from a transformer coupled design to a broadband LC filter design means that MOSFET switching network needs to generate the negative cycle of the output

signal, therefore a dual polarity power supply rail was needed. Distortion on the amplifier output was overcome by using bigger capacitors on the supply rails and increasing the Q of the output filter from 5 to 9. The addition of a RC snubber circuit compressed the voltage spikes on the switching node. All of those changes helped to improve the amplifier output. Different amplitudes for 90 and 180 degree pulses meant the modulation technique was working. Measurements of the voltage levels of the two pulses showed their amplitudes were correct. The output power of this amplifier was also 100 W. The CPMG pulse sequence for this amplifier is the same as the one for the Class A amplifier, which is standard in Prospa. The pulses in this sequence have the same length but with the amplitude of the 180 degree pulse double the amplitude of the 90 degree pulse. NMR test results from the RCA system showed very similar data to the Class A amplifier from the same water sample. However there was still an oscillation on the start of the imaginary data curve (Figure 3.46) but it was a lot smaller compared to the first Class D amplifier. This could be the advantage of having a broadband LC filter output compared to a transformer. The broadband output has a ring down time of less than 1 μ s compared to 3 μ s of the transformer output.

While this second amplifier had the amplitude modulation capability, it can also work on a fixed amplitude mode as the first Class D amplifier. This operation mode was also tested using the same CPMG pulse sequences as the first amplifier, that is having fixed amplitude but the length of the 180 degree pulse double the length of the 90 degree pulse. NMR test results from the RCA system showed almost exact data to the Class A amplifier, even the oscillation at the start of the imaginary data curve was similar in size (Figure 3.49). This was a great improvement compared to the first Class D amplifier.

Comparing the NMR results from the two different operation modes of the second Class D amplifier, the reduction of the oscillation at the start of the imaginary data curve suggests that the oscillation could be caused by the imperfect power level of the 90 degree pulse and the ring down time. Changing the length of the pulse is more precise than changing the amplitude as the amplitude is controlled by the width of the driving half cycle pulse, which does not have good resolution at low power. Imperfect 90 degree pulse power causes imperfect tipping of the magnetization vector. Other researchers have also suggested that the oscillations are due to imperfect phasing due to the start and end parts of the RF pulses [76].

The third amplifier built using single cycle control is truly a PWM controlled Class D amplifier. It uses multiple PWM pulses to control the amplitude of each half cycle (Figure 3.57, 3.58). The circuit is a lot more complex compared to the previous amplifiers. The stacked FET setup allows for higher supply voltage rails and hence greater output power is possible. The amplifier was again set to work at 2 MHz with 100 W output power to test on the RCA system. The efficiency of this amplifier is 86%. This time a rock core sample was used for testing. The decay curve and the relaxation spectrum (Figure 3.65) are very similar for the Class D and the Class A TOMCO amplifier. The external TOMCO amplifier was used because the pulse sequence contains 50000 echoes and the internal Class A amplifier overheats with such a long sequence.

The single cycle controlled PWM amplifier working at 2 MHz is a new design and no other PWM Class D amplifiers have been reported to operate at that high frequency with output power of 100 W. The proposed design used a low pass filter as an integrator to provide a reference to the input for generating a PWM control signal. This design avoids the need for high precision comparator components, therefore reduced component cost. The use of a feedback signal from the output means it is a closed-loop design, thus significantly more stable than the standard PWM techniques used in audio amplifiers.

The 20 MHz Class D amplifier used a full bridge configuration with transformer coupled output. The use of a low Q tank circuit plus intelligent switching of the MOSFETs results in good rise and ring down performances (Figure 4.3). Spin echo and CPMG experiments on the MOUSE sensor show similar results compared to the Class A amplifier. The output power of 100 W with 73% efficiency at 20 MHz is superior to any other Class D amplifiers that have been reported.

The development of the 17 MHz Class D amplifier with amplitude modulation capability, output 30 W with 82% efficiency is also operating at higher frequency, with higher output power and efficiency than the ones reported by other researchers. It used two fixed voltage rails to output two different amplitudes of pulses as the 90 and 180 degree pulses. This is not exactly amplitude modulation as in the previous PWM controlled amplifiers, however it is good enough for outputting two different power levels of pulses for NMR applications.

A 17 MHz sensor was constructed for testing the new amplifier. It was a very simple design using a 0.5 T permanent magnet and housed inside an Aluminium box. The rubber sample is also a coil former for the inductor, this means the sample for the sensor will never change. It has a Q of 30 (same as the targeted Mini-MOUSE), adjustable capacitors were used to tune and match the sensor to 50 ohm at 17 MHz. This was a very crude design but was good enough to use as a load for testing the amplifier.

The raw CPMG echo data and decay curve for the new Class D amplifier is very similar to that of the Class A amplifier tested using the Aluminium box sensor (Figure 4.20, 4.21). This is a good indication that the new amplifier design was working. A single exponential curve fit on the decay curve finds the T_{2eff} of the sample to be 4.3 ms, this agrees with previous measurements of 4.23 ms.

The successful implementation of the compact and efficient 17 MHz Class D amplifier means the first project goal had been achieved, allowing the development of a mobile hand held NMR system. With the availability of a new SoC FPGA module from Xilinx, the MicroZed board, an attempt to build a fully functional mobile NMR system working with the Mini-MOUSE was made.

Using the development tools from Xilinx (Vivado, SDK, PetaLinux) a digital transceiver system was implemented on the FPGA with the Zynq processor. A carrier board with high speed ADC and DDS devices were built to interface with the MicroZed board. The 17 MHz amplifier was modified to be controlled by the FPGA signals. A new duplexer and receiver amplifier board was built to enable the Wobble experiment and with amplifier gain adjustable up to 72 dB. A new power supply board was built to supply all the different voltage levels to the system. The completion of the digital hardware design achieved the second project goal.

The new system was designed to be controlled remotely using a web based program on an iPad, a user interface was developed using javascript. Pulse sequences for this new system was developed using a Cryogen free superconducting magnet sensor, as it provided good signal to work with during the development stage. The two most useful pulse sequences for working with the Mini-MOUSE are the Wobble and CPMG sequences. Implementing signal averaging improved the SNR. With the system hardware built and the pulse sequences implemented, this achieved the third project goal. The integration of the new spectrometer

with the Mini-MOUSE gave a fully functional mobile NMR system. The new spectrometer system was first thoroughly tested using a home-made sensor, then using the MOUSE sensor on rubber samples. Successfully obtaining T_{2eff} parameters from different rubber samples means the system is functional and this achieved the fourth project goal. The full system was then tested on polymer samples and T_{2eff} measurements were successfully made to reflect the different stiffness and compositions of the samples. A reaction monitoring experiment was also performed to test the stability of the system. It monitored the curing of a silicone elastomer over 48 hours. The results showed a clear trend of decreasing T_{2eff} over time as the mixture hardened. This experiment showed that the system is very stable. These tests shown the new system is capable of industrial applications and the fifth project goal had been achieved.

Overall the development of the mobile system has been successful and the ultimate goal of this research has been achieved. The full system prototype fits in a case measuring 140x120x100 mm (LxWxH) and weighs 800 grams, Figure 6.1. While this is only a prototype system, it is a fully functional mobile NMR system and no other NMR systems with similar performance have been reported to be smaller. The development work on the Class D amplifiers has shown the potential of the high efficiency amplifiers for NMR systems. The successful implementation of the digital system using a SoC FPGA module resulted in a platform that can be used to develop compact and mobile NMR systems.

Compared to the LapSpec mobile spectrometer, the new spectrometer is lighter (0.8kg vs 3.6kg), more efficient (82% vs 25%), longer battery life (5 hours vs 4 hours) and more portable with the use of an ipad control instead of a computer. The cost of the system is also reduced as the component cost for the full system is under 800 USD.

While the new mobile system has many advantages, there is also a disadvantage compared to the bench top systems. The used of a Class D amplifier with a resonant tank output limits the bandwidth of the amplifier output. This means when using another sensor with a different frequency, a hardware modification on the amplifier is needed. This would not be the case in the benchtop systems as the use of a Class A amplifier normally has a very broad frequency range.

Figure 6.1 The full system, 140x120x100 mm (LxWxH)

Future work on the system is to perform more experiments on different material samples and find other potential applications. All the essential hardware of the system has been implemented, only the packaging needs to improve to turn this prototype into a commercial product.

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Appendices

Appendix I: Transformer Coupled 2 MHz Class D RF amplifier

Appendix II: PWM Controlled Class D RF Amplifier

Appendix III: Class D RF Amplifier with Single Cycle PWM Control

Appendix IV: Class D RF Amplifier with Stacked FET Setup

Title		
Size	Number	Revision
A4		
Date:	14/01/2015	Sheet of
File:	D:\Workspace\IPVM IP Unipolar LimitDrawn.dwg	4

Appendix V: The 20 MHz Full Bridge Class D RF Amplifier

Appendix VI: The 17 MHz Class D RF Amplifier with Amplitude Modulation

1 x Heatshrink Dugkey HS190-MD

Title	
Size	Number
A4	
Revision	
Date:	14/01/2015
File:	D:\Workspace\Resonant 17MHz Modulator\Board 1\Board 1.schDoc

Appendix VII: Carrier Board

Title *			
Size: A4	Number: *	Revision: *	*
Date: 13/01/2015	Time: 2:55:58 p.m.	Sheet: * of *	*
File: D:\Workspace\Mobile\NIR_FPGA_Adaptor\MobileSystem_SchDoc			

Appendix VIII: RF Amp and Power Supply Board

Appendix IX: Duplexer and Receiver Amplifier Board