Self-Powered Soil Moisture Monitoring Sensor Using a Picoampere Quiescent Current Wake-up Circuit

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Abstract—Low power wireless standalone sensors which can operate without any wiring have received significant attention in sensor network applications. These devices harvest environmental energy resources to supply their power and transfer their collected data using wireless RF links. In many instances the power supplied from the environment is far less than the power required by the sensor device. In this case the main solution is to accumulate energy on a storage element and when enough energy is stored, the sensor node is instantaneously activated using an under voltage lockout, UVLO, circuit. During this short time burst, the sensor performs the required acquisition, transmits the results and enters a sleep mode until again enough energy is collected. The quiescent current of the UVLO is the main factor that determines the minimum power level at which the sensor node is still operational. Most wake-up circuits used in conventional devices suffer from a quiescent current of a few hundred nanoamperes. In this work, using a zero bias current MOSFET based approach, a new wake-up circuitry is presented which lowers the quiescent current down to the picoampere range. As a practical application, the effectiveness of the proposed circuit is shown in a soil moisture monitoring sensor setup.

Index Terms—Energy harvesting, Low power electronics, MOSFET circuits, Soil moisture monitoring, Sensors

I. INTRODUCTION

WITH the advances achieved in telecommunications and wireless systems, wireless sensors nodes have found wide application in different fields of industry [1]–[3], agriculture [4] and environmental protection. They are extensively used for monitoring of a wide area using multiple numbers of smaller local sensors. The problem with this scenario is that the battery replacement of many units is difficult. Many successful monitoring sensor node setups supply the power of the units using environmental energies [5], [6]. Solar power is one of the most common solutions; however at indoor setups the supplied power is considerably low [7]. Other alternatives have also been considered for harnessing of surrounding energies such as the use of environmental vibrations [8], [9], electromagnetic waves, environment heat and magnetic fields [10], [11]; however these sources also deliver limited energy to the operational device and generally smaller energy harvesters

which are integrated with the electronic circuit board harness lower power.

A lot of research has been devoted on the design of high efficiency voltage rectifiers, charge pumps, switching DC-DC converters (buck/boost) [12], [13] and low drop out regulators in energy harnessing sensor nodes to minimize the power dissipation of the power delivery blocks. Appropriate zero bias current circuits can also help increase the efficiency of the available power [14].

When the harnessed power is much lower than that required by the electronic circuits an effective approach known as sleep/wake-up is used. In this method all units, even the switching converter and linear regulators, are put to sleep and energy is accumulated on a storage element such as a super capacitor with low leakage current. When enough energy is accumulated, it is transferred momentarily to the electronic circuits [15]–[17]. The circuit which monitors this event is known as the wake-up block or under voltage lockout, UVLO, detector. Technically the UVLO is a Schmitt trigger [18] and commonly used architectures for such a device include opamp-based and CMOS inverter-based topologies.

UVLO circuits are commercially available in voltage supervisors and charger devices such as LTC3588 and its similar families [19], [20]. However, most circuits presented so far have a quiescent current of a few hundred nano amperes. Reducing this value will be advantageous since it means that the sensor node can be operated with lower levels of available transducer power.

In this work a new topology is presented which reduces the quiescent current of the UVLO circuit and thus lowers the harvester power dissipation. The concept presented here uses non-overlapping activation of pull-up and pull-down switches in the output stage of the UVLO circuit. Using positive feedback, the amount of time required for the output signal state change is decreased. The required reference-level voltages are also generated using a low-power subtractor. The performance of the proposed approach is investigated using both simulation and experimental setups. Also, a working proof of the concept is presented to show the effectiveness of the approach in a wireless and self-powered soil moisture monitoring sensor. The rest of the paper is organized as follows: In section II energy harnessing sensor nodes and the function of UVLO circuits in these devices is explained. The proposed circuit and its analyses are presented in section III. Simulation and experimental results are given in section IV. Finally concluding remarks are presented in the last section.

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Fig. 1. A typical configuration of a low power energy harvesting sensor node.

Fig. 2. (a) The function of a Schmitt trigger as the UVLO block of a low-power sensor node. (b) The basic concept used in the proposed ultra-low power Schmitt trigger.

II. CONVENTIONAL UVLO

A typical configuration of an electronic energy harnessing system used in sensor network devices is shown in Fig. 1. In sensor network applications, the power requirements are relatively low and thus simple environmental energy harvesters such as small solar panels, RF antennas, piezoelectric elements, electro-dynamometric generators and thermopile transducers are appropriate choices. These devices, shown as the power source block in Fig. 1, produce limited power output and suitable designs must be considered to minimize any source of power dissipation for efficient operation.

The system shown in Fig. 1 includes the frontend energy harvesting transducer (power source), the rectifier which can be used to convert AC voltage sources to a DC potential. A voltage multiplier or charge pump can also be used instead of this block if higher V_{power} potentials are required. This voltage then enters the DC-DC converter to convert the input voltage required by the electronic circuitry of the final stage. Switching DC-DC converters help perform this conversion with lower power dissipation compared with linear regulators. A maximum power point tracking (MPPT) controller can also be used to help extract the maximum available power from the rectifier. The low drop out regulator in the final stage helps to better regulate the achieved voltage and to remove any unwanted voltage ripples from the switching converter. The achieved V_{DC} voltage can now be used for all other electronics including the sensor, processor and wireless transmitter.

Fig. 2(a) shows the configuration of the Schmitt trigger (UVLO) block in the energy harnessing system. The load shown in the figure represents all electronic blocks after the rectifier, including the DC-DC converter or MPPT circuits. The harvesting frontend is also modeled with the current source, I_s , charging a storage capacitor, C_s .

Fig. 3. (a) I-V characteristics of the load placed after the rectifier. (b) Instantaneous power delivery to the load using the UVLO block.

The current-voltage characteristic of the typical electronic power consuming block is shown in Fig. 3(a). The operational region of these devices is at supply voltages above the nominal level, V_{nom} . With no UVLO circuit, if lower powers are available, the electronic blocks will still draw current and dissipate power; however the provided power cannot place the electronic circuitry at a suitable operation point. As shown in Fig. 3(b), while the consumed average power remains equal to P_{in} , with an UVLO the operation point can move between points B and C which is suitable for the operation of the load electronic circuitry.

Opamp-based and inverter-based Schmitt triggers have conventionally been used for ULVO realization. In the opamp-based approach, 2 opamps are used to compare the accumulated input voltage with 2 different reference levels. If the voltage is higher than the upper threshold limit, V_{T+} , the Schmitt trigger latches into the wake-up state, and if lower than the lower threshold limit, V_{T-} , it latches into the sleep state. The static current of the two opamps is the main source of quiescent current in this case. Although CMOS inverter-based Schmitt triggers avoid the static current of the opamp-based approach, however whenever the input is crossing the upper/lower threshold limit, a short circuit current will be drawn from the supply resulting in a specific average quiescent current throughout the periodic cycle.

III. PROPOSED METHOD

Similar to a CMOS inverter gate, the core of the proposed Schmitt trigger is composed of a nMOS (Mno) and a pMOS (Mpo) device, however for all input voltages these two devices are never activated simultaneously even in transient states to avoid any static currents. With the proposed configuration, three states can be considered for the nMOS-pMOS pair. When Mno is on, the output is low and when the Mpo switch is on, the output is high. Finally, if both Mno and Mpo devices are off, the output retains its previous value. As shown in Fig. 2(b), the idea is to connect the input voltage, V_i , to Mpo and $V_i - V_{shift}$ to Mno. Subsequently, for $V_i < V_{DD} - |V_{tp}|$, a high level will be produced at the output, for $V_i > V_{tn} + V_{shift}$ a low level and for $V_{DD} - |V_{tp}| < V_i < V_{tn} + V_{shift}$ the output will retain its previous state. The aforementioned behavior is similar to a Schmitt trigger with two separate comparison levels with an upper threshold limit, V_{T+} , of $V_{tn} + V_{shift}$. As will be explained latter, the supply voltage of the Schmitt trigger itself,

V_{DD} , will be eventually adjusted at about V_{T+} using an auxiliary rectifier. In the proposed circuit the lower threshold limit, V_{T-} , will be equal to $V_{tn} + V_{shift} - |V_{tp}|$. When each of the nMOS or pMOS devices are activated, they will reside in the triode region and thus the output can be switched to V_{DD} or GND with less delay than devices in the subthreshold region used in conventional low-power designs. As shown below, a positive feedback further helps the output switch to its activated state.

An important challenge here is the design of a subtractor circuit which can produce the $V_i - V_{shift}$ level with no static power usage. As shown in Fig. 2(b), a simple nMOS diode connected device (Mnd) in series with V_i and a parasitic capacitance of C_p at its output, may seem to achieve the necessary function via the $V_y \approx V_i - V_{tn}$ equation expected at its source terminal. However, this subtractor will show different behavior with rising or falling inputs. A resetting switch (Mnr) can solve the aforementioned problem. When the input voltage, V_i , is increasing, the reset switch should be turned off. However, the reset switch will still impose some leakage current which is put into effective use here. The leakage current of the reset switch should be adjusted higher than the leakage current of the diode load. In this case, the subtractor output voltage will experience a drop in relation with V_i .

In Fig. 4 the resetting switch Mnr is shown while deactivated, however it still produces some subthreshold leakage current which can be modeled by I_{0r} . To extract the relationship of V_y with respect to V_i it is assumed that V_i changes exhibit a ramp-waveform profile with time, either increasing due to the charging of the storage capacitor by the energy harnessing source or decreasing due to the discharging of the storage capacitor by the load. It is also initially assumed that in this case V_y follows V_i with a constant voltage shift. With these assumptions, the current on capacitor C_p will be $C_p \cdot m$ where m is the slope of V_i . Thus, using subthreshold drain current equations, the relation of V_i and V_y can be obtained using (1) where (W/L) is the corresponding MOSFET dimension ratio, V_{th} is the thermal voltage, V_{tn} is the threshold voltage, I_s is a current factor and η is a subthreshold conduction factor.

$$C_p \cdot m + \left(\frac{W}{L}\right)_{nr} \cdot I_s \cdot e^{\left(\frac{-V_{tn}}{\eta V_{th}}\right)} = \left(\frac{W}{L}\right)_{nd} \cdot I_s \cdot e^{\left(\frac{V_i - V_y - V_{tn}}{\eta V_{th}}\right)} \quad (1)$$

The first term of the left hand side of equation (1) is the current on capacitor C_p while the second term is the subthreshold leakage current of Mnr. The subthreshold leakage current of Mnr is modeled with I_{0r} as shown in Fig. 4. Simplifying (1), (2) is obtained which proves that the initial assumption was correct and V_y follows V_x with a constant voltage shift. This constant voltage shift is however dependent on the input voltage slope, m .

$$V_y = V_i - V_{tn} - \eta V_{th} \ln \left(\frac{C_p \cdot m}{I_s \cdot \left(\frac{W}{L}\right)_{nd}} + \left(\frac{W}{L}\right)_{nr} \right) \cdot e^{\left(\frac{-V_{tn}}{\eta V_{th}}\right)} \quad (2)$$

Looking back at (1), it is observed that if I_{0r} is chosen much larger than $C_p \cdot |m|$, the first term on the left-hand side

Fig. 4. Circuit model used for the analysis of the proposed subtractor.

of (1) can be neglected and thus the voltage shift between V_i and V_y will be independent of m as shown in (3).

$$V_y = V_i - \eta V_{th} \ln \left(\left(\frac{W}{L}\right)_{nr} / \left(\frac{W}{L}\right)_{nd} \right) \quad (3)$$

The voltage shift, V_{shift} , in this case can be expressed as follows:

$$V_{shift} = \eta V_{th} \ln \left(\left(\frac{W}{L}\right)_{nr} / \left(\frac{W}{L}\right)_{nd} \right) \quad (4)$$

However the power dissipated by the static current of I_{0r} is expressed with (5) and large values of I_{0r} will result in higher power dissipation.

$$P_{diss} = I_{0r} \cdot V_i \quad (5)$$

It should be noted that m_{rise} , the slope of the V_i transient during charging of C_s (by the energy harnessing source), is much smaller than the absolute discharge slope of V_i , $|m_{fall}|$, due to the instantaneous connection of the load. The approach used here is to choose I_{0r} much larger than only $C_p \cdot m_{rise}$. Subsequently when the load is connected, V_y is discharged through another path and by activating the Mnr MOSFET. With this approach I_{0r} can be kept at relatively low values to limit the static power dissipation.

The complete circuit design is shown in Fig. 5. With the proposed circuit, V_i increases relatively slowly since it happens due to the charging of the output capacitor by the low environmental energy source. In this case V_y follows V_i with a constant voltage shift. When the accumulated voltage reaches the upper threshold limit, the output power switch Mns is activated and power is transferred to the load. In this phase V_i drops rapidly with a high slope. Although in this phase the Mnd subtractor alone cannot produce a correct voltage shift between V_y and V_i however during this phase, the reset switch Mnr is activated to quickly return the subtractor output to its correct state.

To prevent any short circuit power dissipation a pMOS switch (Mpr) is used to disconnect the power supply path when the reset switch is activated. The final elements of the design chain are Mpr1 and Mpr2. As stated earlier, when the supply potential passes the upper threshold limit, the Schmitt trigger output should switch is a short period of time. To facilitate this transition a positive feedback is generated using Mpr1. When the Schmitt trigger output V_O' begins to drop, Mpr1 will be activated thus helping the gate potential of Mno to further increase and to pull down the output of the Schmitt trigger,

Fig. 5. Complete design of proposed Schmitt trigger, solar panel and load.

Fig. 6. Quiescent and maximum output currents of the Opamp and inverter based Schmitt triggers as a function of V_{T+} .

V'_O . Again, to prevent any static power dissipation, a pMOS device Mpr2 is placed in series with Mpr1 which disconnects the power supply path when the output is fully activated. It should be noted that the resetting of the Mno gate voltage starts immediately after Mpr1 is disconnected.

IV. EVALUATION RESULTS

The proposed method is evaluated regarding its upper and lower threshold limits, quiescent currents, power dissipation and overall performance using both simulations and experimental setups. Both an integrated and also a discrete design is used for verifications. The integrated circuit design is evaluated using a $0.18\mu\text{m}$ standard CMOS process. For the discrete design, CD4007 MOSFET arrays are used for both simulations and also experimental evaluation.

For comparison, other approaches such as the conventional opamp-based and inverter-based Schmitt triggers are also investigated and simulated for quiescent current in a $0.18\mu\text{m}$ standard CMOS process technology.

In Fig. 6, the quiescent and output current driving capability of the opamp-based and inverter-based Schmitt triggers are plotted as a function of the upper level activation voltage, V_{T+} . With higher V_{T+} levels, a higher gate-source potential can be placed on the output power MOSFET and thus a higher current can be delivered to the output. However, a higher V_{T+} requires a higher supply potential and subsequently larger currents will be drawn in the actual block or its succeeding drivers.

Fig. 7. Quiescent and maximum output currents of the proposed Schmitt trigger as a function of V_{T+} .

Fig. 8. V_{T+} of proposed design implemented by thick oxide MOSFETs in $0.18\mu\text{m}$ as a function of W/L ratio.

In Fig. 7 the same parameters are investigated for the proposed circuit. The designed Schmitt trigger eliminates the short circuit currents and also the required bias currents. The only source of quiescent current is mainly the leakage current of switches in the off region. As the Figure shows, the proposed design shows a relatively constant and also considerably low quiescent current for different threshold voltage detection levels. With higher threshold voltage levels, due to the higher provided gate-source voltage, higher currents can be delivered to the output.

As shown in Fig. 8, V_{T+} of the proposed Schmitt trigger can be adjusted by changing W/L ratio of diode connected MOS or placing MOS devices in series with the V_i path.

To investigate the functional dependence of the proposed wake-up circuit on external factors, process and mismatch Monte Carlo evaluations and temperature sweeps were performed on the two diode circuit. Fig. 9(a) and (b) show the histogram of V_{T+} and the quiescent current of the circuit using Monte Carlo simulation respectively. The number of

Fig. 9. Monte Carlo simulation of the proposed wake-up generator circuit.

Fig. 10. Temperature effect investigation of the proposed wake-up generator circuit.

runs are 1000 and 500 for the two cases and conventional room temperature of 27°C is used. According to the histogram plots, V_{T+} has a mean and standard deviation of 1.74V and 0.14V respectively. This shows 68% of the chips will have a V_{T+} which changes under $\pm 8\%$ around the designated value. Fig. 9(b) shows the quiescent current experiences an average and sigma of 23pA and 6pA respectively.

The temperature dependence of V_{T+} and the quiescent current of the proposed circuit is also investigated in Fig. 10. It should be noted that although Fig. 10 shows V_{T+} and quiescent current changes over a temperature range of 0 to 100°C, however in the application given in this paper, the soil moisture is measured for indoor plants and greenhouses. Thus here, the conventional indoor temperature range is considered from 10 to 40°C. Judging by the obtained results over the indoor temperature variation range, V_{T+} will only experience 5% changes.

The performance of the proposed approach is also investigated using experimental evaluations. For the experimental results, discrete MOSFETs are used in the implementation. In Table I both simulation results and also experimental results of the proposed method configured with discrete MOSFETs are reported. The table investigates the effect of the number of diode-connected loads (Mnd) in the path of V_i on V_{T+} . It also shows how changing V_{T+} affects other parameters such as quiescent current, maximum load current and maximum load power.

The effect of storage capacitor voltage slope of V_{T+} is also investigated in Fig. 11. Consistent with the behavior predicted in (2), the rate at which V_i increases will have a small effect

TABLE I
SIMULATION AND EXPERIMENTAL RESULTS OF DISCRETE MOSFET IMPLEMENTATION

Type		V_{T+} (V)	I_{Qui} (pA)	I_{Lmax} (mA)	P_{Lmax} (mW)
Sim.	Mnd x1	2.8	230	16.9	45.5
	Mnd x2	3.8	420	23.1	85.5
Exp.	Mnd x1	2.8	200	10	27
	Mnd x2	3.8	200	12.2	40.3

Fig. 11. Effect of V_i increasing rate on the V_{T+} threshold voltage.

on V_{T+} .

Fig. 12(a) shows the signal waveform at nodes V_O , V_y and V_{power} of Fig. 5 which are acquired by oscilloscope channels 1, 2 and 3 respectively. Since the activation period of V_O is very short and can be merely seen during the voltage drop of V_{power} in Fig. 12(a), that time period is expanded in Fig. 12(b) to show how V_{power} , V_y and V_O change during the activation period.

To investigate the effectiveness of the proposed approach under low-energy conditions, the proposed wake-up circuit is used in an indoor/greenhouse soil moisture monitoring setup. Although passive tags are used extensively for the monitoring of parameters such as humidity or oxygen, but most of these sensors require a base station or observer in close proximity to sense the resulting reading [21]. Active sensors on the other hand can transmit the reading to distances far away using an active transmitter. As shown in Fig. 13(a), in a conventional active setup usually a moisture transducer is used to sense moisture and convert it to a digital code. An RF transmitter is used to transmit the digital data to the base station and finally a microcontroller is used to configure the units and also control the flow of data from the sensor to the transmitter. While some simplifications can be applied to the conventional method, the general approach tends to be power hungry. In this work, a simple circuit is used as the load of the proposed

Fig. 12. (a) Oscilloscope waveforms of different circuit nodes from Fig. 5. (b) Time zoomed version of waveform at the activation instance.

Fig. 13. (a) conventional block diagram of a soil moisture detection sensor node, (b) the load used in this work for both the sensing and transmitting of soil moisture.

Fig. 14. Fabricated prototype board placed into the plant soil.

wake-up circuit for soil moisture detection and transmission. As shown in Fig. 13(b), the load consists of a low dropout regulator and a Colpitts oscillator. The oscillator transmits an RF signal to the antenna. The oscillation frequency of the Colpitts circuit is modulated by the capacitance effect of the soil electrode. So any changes in the soil moisture will result in a frequency shift of the transmitted RF signal. Although the circuit is sensitive to external factors such as temperature, however as it will be shown in the evaluation results, for well regulated environments such as indoor rooms or greenhouses, this drawback will not be a limiting factor.

The actual prototype board used for this purpose is shown in Fig. 14. As it can be seen in the figure, the solar panel is constructed from 12, 5mm×5mm photodiodes. These p-n junctions produce energy when illuminated by light. All photodiodes are arranged in series to provide the necessary operational voltage level. Starting off from the top to bottom, after the solar panel arrangement there is the polyester main storage capacitor, the Schmitt triggers circuitry and finally the regulator and the Colpitts oscillator/transmitter. In the current picture the board electrodes are inside the soil.

Fig. 15. Number of wireless transmitter bursts per hour for different indoor surrounding illumination levels.

Fig. 16. Sensor reading versus soil moisture level.

With the 10 μ F low leakage polyester storage capacitor, when the voltage has reached the trip point, the wireless transmitter can be kept active for approximately 5ms duration and a short RF burst is transmitted in this time interval. In Fig. 15, the number of data bursts transmitted by the aforementioned transmitter is measured with a low-power solar panel energy source. The moisture of the soil can be assessed considering the RF frequency of the transmitted burst.

To investigate the accuracy of the proposed approach, different soil samples were prepared with specific moisture levels as described in [22]. In this procedure 35 containers were prepared by filling each with about 250mL compressed garden soil. Different water volumes were poured in every group of 5 containers. The soils were mixed well to get a homogenous sample. With this approach each container group contained a certain volumetric water content (VWC) level. The average frequency measurement of each group and also the minimum and maximum reading of the sensor at each VWC level is reported in Fig. 16. It should be noted that the reported results are normalized over the entire measurement procedure. In the proposed sensor, the normalized reading of 0 corresponds to an oscillation frequency of 27.28MHz and 1 corresponds to 26.96MHz. For the sake of comparison, the calibration curve measurement of the standard Diviner 2000 sensor [22] is also shown in Fig. 17.

The performance of the sensor was also investigated under different ambient temperatures. As shown in Fig. 17, the effect of temperature on the normalized sensor reading (oscillator frequency) is shown under different VWCs. Better temperature regulation (such as greenhouses) or temperature compensation methods can reduce the error due to this effect.

The effect of temperature on the transmission burst intervals and also burst duration is shown in Fig. 18. As the plot suggests with higher temperatures, the repetition rate will increase slightly. This result is due to the fact that at higher temperatures, V_{T+} drops slightly leading to a higher average charge current from the solar panel. Thus eventually the accumulated

Fig. 17. Proposed sensor reading variation versus ambient temperature.

Fig. 18. Repetition and burst time drifts due to ambient temperature.

charge reaches the trip point earlier. Also according to this experiment the burst duration also experiences a small change when the temperature increases. This can also be contributed to the fact that the available voltage swing to the power rail decreases at higher temperatures. Also the oscillator bias current has a small increase at higher temperatures resulting in the slight reduction of the burst signal duration.

The performance of the proposed wake-up circuit in both a simulation and also experimental setup is summarized and compared with previous methods in Table II.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON OF PROPOSED CIRCUIT WITH PREVIOUS METHODS

Work	Threshold Voltage	Quiescent current
LTC3588	3.3V	900n
[15]	1.9V	1u
[13]	3V	8u
[14]	2V	300n
CMOS inverter-based ^a	2.8V	250n
Opamp-based ^a	2.8V	1.5u
This work 0.18 μ m	1.5V	100p
This work discrete ^a	2.8V	200p

^aDesigned for a maximum output power transfer of 40mW.

As can be seen, the proposed method outperforms previous techniques regarding the quiescent current requirements. Thus the proposed method is more appropriate for energy sources with very low output current delivery.

V. CONCLUSIONS

Efficient energy delivery to low-power loads has been the focus of many recent researches and is an important aspect in energy harvesting circuits [23]. In this paper an ultra-low quiescent current under voltage lock out circuit was presented and successfully implemented using all-MOS devices. With

the proposed circuit, low-power energy harvesters can store their energy on a low leakage capacitor and when the voltage level reaches a certain level the power can be instantaneously delivered to the electronic blocks. By avoiding any static bias current and at the same time, operating the output switches in the deep triode and cut-off region the quiescent current was significantly reduced. It was shown that the quiescent current of a discrete prototype could be as low as 200 pA, a value much smaller than those reported in previous works. At this quiescent current, the proposed under voltage lock out circuit can drive electronic loads with powers as high as 40 mW. The proposed design approach was also compared with conventional designs of under voltage lock out techniques in the same operational conditions such as opamp-based and CMOS inverter-based. The results showed that the new approach outperforms conventional methods of UVLO design for ultra-low power energy harnessing applications.

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