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Interleaved Half-Bridge Submodules with Sensorless Leg Current Balancing in Modular Multilevel Converters

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Abstract—A new state observer-based current balancing method for Modular Multilevel Converters with Interleaved half-bridge Sub-Modules (ISM-MMC) is presented in this paper. The developed observer allows estimating currents through interleaved half-bridge legs in each submodule of ISM-MMC basing only on arm current and submodule's capacitor voltage measurements. Then, the interleaved current balancing control uses the estimated currents to reduce the interleaved currents imbalance caused by upstream control actions. This technique minimizes the number of required current sensors in ISM-MMC, thereby reducing the converter's cost, weight, and volume. Capabilities of the proposed interleaved currents sensorless balancing control has been tested against standard parameter tolerances of the composing passive elements. The feasibility of the proposed method is verified by extensive simulation and experimental tests.

I. INTRODUCTION

Demand for efficient high-power conversion systems has recently increased in industrial applications at all voltage levels. The common objectives in converter design are larger power capacity, higher power density and better power quality. In this sense, modular multilevel converters (MMCs) have already taken over the market in high- and ultra-high voltage applications [1], [2]. Recently, they have been also expanded on medium- and low-voltage applications [3]–[5]. The scalable structure of MMCs allows meeting the imposed voltage requirements by stacking the so-called submodules (SMs) in a series. SMs are normally composed by half-bridge or full-bridge configuration, while other structures are also possible [4], [6]. An increase in current capacity can be attained in several ways, for instance by parallel connection of power units at submodule level, arm and phase leg paralleling or even synchronized operation of several converters, as it is already reported in [7]. Another solution to achieve a higher current capacity in MMCs has been proposed in [8]. The new MMC architecture is based on interleaved half-bridge submodules, and as the name suggests, it employs the interleaving effect of the parallel-connected half-bridges. In such an arrangement, the Modular Multilevel Converters with Interleaved half-bridge Sub-Modules (ISM-MMC) demonstrates superior performance than classical MMCs, considering identical power ratings and power switch count [9]. However, as revealed in [8], [9], particular attention in ISM-MMC must be drawn to the typical

problem for all interleaved configurations, namely proper current sharing among interleaved units. An excessive power loss, thermal stress, inductors saturation are just a few undesirable aspects that accompany unequal current sharing among interleaved units. Most of the conventional ways to solve this problem are based on sensing each interleaved current to provide the current information for the dedicated active control loop. This approach is well established for dc/dc [10], [11] and some ac/dc converters [12]. A similar method has been proposed in [13] for an ISM-MMC. An obvious drawback of these current balancing methods is the large number of current sensors that is almost proportional to the number of interleaved units. To compact the converter and reduce its cost and complexity, several current estimation techniques have been developed for interleaved dc/dc converters, based on parasitic resistance estimation [14], small-signal duty cycle perturbation [15], self-tunable digital filter [16], temperature equalization [17] and many other. Similarly, several works have been dedicated to estimation algorithms to solve another common balancing problem for MMC structures, namely capacitor voltage balancing. For instance, authors in [18] proposed a current sensorless capacitor voltage balancing method based on a state observer. The observer provides estimates of arm currents that are typically used in most capacitor voltage balancing algorithms.

Since ISM-MMC has been just recently introduced, very few works are dedicated to this topology. Thus, to the best of the authors' knowledge, no publications have been focused on estimating the interleaved currents in ISM-MMCs. The sensorless solution, in general, requires a computation-intensive estimation algorithm that can be sensitive to parameter variation. Moreover, the estimation method must run in real-time in order to get the estimated values at the proper instant. Therefore, the main contribution of the current work is the implementation of a sensorless current balancing method for ISM-MMC that is capable to evenly allocate interleaved HB-leg currents, while purely relying on their estimation. In this context, the word “sensorless” means that there are no interleaved currents measurements needed. It is also demonstrated that even though the circuital parameter variation affects performance of the implemented observer, the current balancing method can still compensate for the current imbalance, which originates from the actions of the upstream

capacitor voltage balancing strategy. Capabilities of the newly introduced observer and the implemented interleaved current control loop has been thoroughly investigated via numerous numerical simulations and experimental tests.

The required mathematical background of the proposed state observer is explained in Section II. In this section, observability and stability of the implemented state estimator is discussed in great detail. The modified current balancing technique is discussed in Section III. Sections IV and V verify the usefulness of the proposed current sharing technique by presenting simulation and experimental results. In addition to that, some considerations about the observer's sensitivity concerning parameter variation, are highlighted there as well. Section VI summarizes and concludes the paper.

II. DESIGN OF THE STATE OBSERVER

As depicted in Fig. 1, a single-phase ISM-MMC consists of two arms; each one of them comprises a series connection of switching cells, referred to as submodules. The submodules are formed using multiple half-bridge converters (units) connected in parallel to a common dc capacitor (C). Inductors (L) are used to connect each half-bridge converter to a common point, which forms a positive terminal of the submodule. Resistances (R) placed in series with inductors represent equivalent series resistances of each branch. For the following analysis, parameters (R, L, C) in the N submodules and in the K units are assumed to be identical among themselves, unless otherwise stated. The second terminal of the submodule constitutes the negative dc rail.

Fig. 1. Circuit diagram of a single-phase ISM-MMC.

With respect to Fig. 1, the voltage of a generic n -th submodule can be written as

$$v_{SM} = \frac{1}{K} \left[\mathfrak{z} v_c - L \sum_{k=1}^K \frac{di_k}{dt} - R \sum_{k=1}^K i_k \right], \quad (1)$$

where i_k , v_c , v_{sm} and $\mathfrak{z}$ are the current flowing in the k -th interleaved unit, submodule's capacitor voltage, submodule voltage and number of active half-bridge legs, respectively. In other words, $\mathfrak{z}$ correspond to the summation of the switching functions g_k (binary values) of all the K legs

$$\mathfrak{z} = \sum_{k=1}^K g_k. \quad (2)$$

By applying the second Kirchhoff's law for a generic half-bridge unit within the SM, the derivative of the current, flowing through the branch, can be found by

$$\frac{di_k}{dt} = \frac{1}{L} [v_c g_k - R i_k - v_{SM}]. \quad (3)$$

Current passing through the SM's capacitor (i_c) at any instant can be determined either from the capacitor equation or as an active legs' current summation:

$$i_c = -C \frac{dv_c}{dt} = \sum_{k=1}^K (i_k g_k). \quad (4)$$

Therefore, from (4) one can obtain the time derivative of the capacitor voltage as

$$\frac{dv_c}{dt} = -\frac{1}{C} \sum_{k=1}^K (i_k g_k) = -\frac{i_c}{C}. \quad (5)$$

Summing up each single current derivative in (3) evaluated for all active HB-legs (only the ones having $g_k = 1$) capacitor current time derivative can be written as:

$$\frac{di_c}{dt} = \frac{\mathfrak{z}}{L} \left[v_c - \frac{R}{\mathfrak{z}} i_c - v_{SM} \right] = \frac{1}{L'} [v_c - R' i_c - v_{SM}], \quad (6)$$

where R' and L' accordingly represent SM's equivalent resistance and inductance with respect to a number of active HB-legs. In other words, capacitor current can be referred to an equivalent branch current that accounts for all interleaved currents in $\mathfrak{z}$ active HB-legs. Equations (5) and (6) form the basic set of equations that describe state variables (v_c and i_c) of an equivalent SM.

A. Observability Verification

A system is said to be observable if the entire system's behavior can be estimated from the system's outputs, which are generally sensed. It can be noted from (5) that the capacitor voltage, by means of the capacitor current, contains information about all interleaved currents that flow in the submodule. Therefore, by selecting capacitor voltage as an output of the system, the observability of the newly proposed state estimator can be verified based on any arbitrarily selected number of half-bridge units. Equations (5) and (6) can be transformed into the state-space representation:

$$\begin{cases} \dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \\ \mathbf{y} = \mathbf{C}\mathbf{x} \end{cases}, \quad (7)$$

where state, input and output vectors can be defined as $\mathbf{x} = [v_c, i_c]^T$, $\mathbf{u} = v_{SM}$ and $\mathbf{y} = v_c$, respectively. Matrices $\mathbf{A}$, $\mathbf{B}$ and $\mathbf{C}$ denote state, input, and output matrices, respectively. Replacing (5) and (6) inside (7), the state-space form can be rewritten as

$$\begin{cases} \frac{d}{dt} \begin{bmatrix} v_c \\ i_c \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{C} \\ \frac{\mathfrak{z}}{L} & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} v_c \\ i_c \end{bmatrix} - \frac{\mathfrak{z}}{L} \begin{bmatrix} 0 \\ 1 \end{bmatrix} v_{SM} \\ v_c = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} v_c \\ i_c \end{bmatrix} \end{cases}. \quad (8)$$

The observability matrix $\mathbf{O}$, in the form

$$\mathbf{O} = \begin{bmatrix} \mathbf{C} \\ \mathbf{C}\mathbf{A} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & -\frac{1}{C} \end{bmatrix}, \quad (9)$$

has always full rank regardless the time varying nature of $\mathbf{z}$. Therefore, as foreseeable, it is always possible observe states v_c and i_c , having sensed the capacitor voltage only.

Carriers phase shift, associated with interleaved modulation scheme, has a crucial role in interleaved currents estimation since it opens a possibility, within each switching period T_{sw} , to formulate multiple values of capacitor current ($i_{c,k}$) derived from corresponding sets of HB-leg currents i_k bearing in mind HB-leg's active states (i.e., $g_k = 1$). If K capacitor currents related to a set of independent K -tuple gate signals g_k can be identified, the set of K HB-leg currents i_k can be reconstructed every switching period from the sole knowledge of the capacitor voltage v_c . The latter statement can be formalized by stacking K time (4) in the form

$$\begin{bmatrix} i_{c,1} \\ i_{c,2} \\ \vdots \\ i_{c,K} \end{bmatrix} = [\mathbf{G}] \begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_K \end{bmatrix} = \begin{bmatrix} g_{1,1} & g_{2,1} & \cdots & g_{K,1} \\ g_{1,2} & g_{2,2} & \cdots & g_{K,2} \\ \vdots & \vdots & \ddots & \vdots \\ g_{1,K} & g_{2,K} & \cdots & g_{K,K} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_K \end{bmatrix}, \quad (10)$$

where each row represents a different capacitor current composition, depending on the binary states of high switch in each HB-leg.

If the duty cycle δ given by the modulating signal stays below $1/K$, it is always possible to rewrite $\mathbf{G}$ as the identity matrix. On the other hand, if the duty cycle δ attain values above $(K-1)/K$, the matrix $\mathbf{G}$ converts into a matrix of ones with the main diagonal made of zeros. For all the remaining values of duty cycle δ , the Hamming space of gate signals K -tuple is characterized by non-repetitive configurations, which sequentially permute with unity Hamming distance. Therefore, it is always possible to find K set of independent K -tuple gate signals g_k . In other words, regardless of the number of interleaved half-bridges, at least one invertible matrix $\mathbf{G}$ can be identified every switching period. Hence, being (10) solvable, the observability of each interleaved current can always be guaranteed.

These considerations are intuitively depicted in Fig. 2 for a submodule having three half-bridges ($K = 3$).

Fig. 2. SM's interleaved carriers and their Hamming space in case of $K = 3$.

It clearly stands out that a SM is observable only in the occurrence of switching actions. Interleaved currents in bypassed or fully inserted submodules with all the gate signals of upper switches in HB-legs either equal to 0 or 1 are not observable (at least within a generic switching period).

B. Observer

The state observer model of a physical LTI system can be represented by

$$\begin{cases} \dot{\hat{\mathbf{x}}} = \mathbf{A}\hat{\mathbf{x}} + \mathbf{B}\mathbf{u} + \mathbf{L}(\mathbf{y} - \hat{\mathbf{y}}) \\ \hat{\mathbf{y}} = \mathbf{C}\hat{\mathbf{x}} \end{cases}, \quad (11)$$

where $\hat{\mathbf{x}}$ and $\hat{\mathbf{y}}$ are estimates of the corresponding plant's state and output. Matrix $\mathbf{L}$ comprises observer gains.

By substituting (5) and (6) into (11) and denoting variables of matrix $\mathbf{L} = [l_v, l_i]$, the following equations can be derived

$$\frac{d\hat{v}_c}{dt} = -\frac{\hat{i}_c}{C} + l_v(v_c - \hat{v}_c) \quad (12)$$

$$\frac{d\hat{i}_c}{dt} = \frac{\mathbf{z}}{L} \left[v_c - \frac{R}{\mathbf{z}} \hat{i}_c - v_{SM} \right] + l_i(v_c - \hat{v}_c), \quad (13)$$

being $\hat{v}_c$ and $\hat{i}_c$ estimates of capacitor voltage and current, respectively. By analyzing (13), one may notice that the knowledge of submodule voltage is required to derive the state of the capacitor current. Although this voltage can be measured directly, such an approach requires to double number of voltage sensors in ISM-MMC in comparison with classical MMCs, which is not an optimal solution from many perspectives (cost, volume, etc.), including a concern about sufficient bandwidth of the voltage sensors. Thus, the voltage can be derived indirectly from (1), bearing in mind that the sum of interleaved currents inside an SM is actually the arm current

$$i_{u,l} = \sum_{k=1}^K i_k \quad (14)$$

resulting in the following expression of SM voltage

$$\hat{v}_{SM} = \frac{1}{K} \left[\mathbf{z}v_c - L \frac{di_{u,l}}{dt} - Ri_{u,l} \right] \quad (15)$$

Estimate sign ("hat") is added to submodule voltage in (15) to point out that it is indirectly obtained based on sensed capacitor voltage and arm current. It should be noted that the arm current sensors are required in addition to typical capacitor voltage measurements. Nevertheless, the arm currents are commonly measured in MMC structures (depending on the control design). It also must be highlighted that the considered in (15) equivalent circuit parameters (R/K , L/K) are rated values and likely to be different in a real system. However, the voltage drops accounted by the parameters in (15) have significantly lower magnitude with respect to the capacitor voltage ($v_{c,n}$). In addition, variation of real circuitry parameters is generally limited by manufacturing tolerances, which are in the range of few tens of percent. Therefore, the reconstructed SM voltage has quite a good accuracy with respect to the actual value, and it can be treated as an independent variable in (13).

Having the estimates of capacitor current in each SM's switching configuration, the HB-leg currents can be derived by

$$\begin{bmatrix} \hat{i}_1 \\ \hat{i}_2 \\ \vdots \\ \hat{i}_K \end{bmatrix} = [\mathbf{G}]^{-1} \begin{bmatrix} \hat{i}_{c,1} \\ \hat{i}_{c,2} \\ \vdots \\ \hat{i}_{c,K} \end{bmatrix}. \quad (16)$$

C. Stability of the Observer

Considering definition of the estimated model (capacitor voltage and current) given by (12), (13) and subtracting it from the plant's model formulated by (5) and (6), the observation error dynamics has the following form:

$$\frac{d\tilde{v}_c}{dt} = -\frac{\tilde{i}_c}{C} - l_v\tilde{v}_c \quad (17)$$

$$\frac{d\tilde{i}_c}{dt} = -\frac{R}{L}\tilde{i}_c - l_i\tilde{v}_c \quad (18)$$

The first simulation test was designed to demonstrate the performance of the proposed state observer-based interleaved legs current balancing control under ideal working conditions, namely when the system R, L, C parameters are well known and equal among themselves. Fig. 4 depicts simulated interleaved currents, their comparison against the corresponding estimated

values and distribution of observation errors when interleaved current control in the entire ISM-MMC is enabled (zones with white background) or disabled (gray zone). It is interesting to note that when the implemented state observer-based interleaved current balancing method is active, the fundamental components of currents within a SM are perfectly balanced. Once it is deactivated, these currents start getting instantly imbalanced. The reason is that the capacitor voltage balancing control forces switches commute to satisfy its objective, balance capacitor voltages around their mean [13]. The equivalent resistance of individual HB-legs acts as a damping factor limiting this unbalance. As lower the value of the equivalent resistance, as larger the current imbalance. Nevertheless, as it is visible from Fig. 4b-Fig. 4h, the estimated interleaved currents nicely repeat the simulated counterparts with minimal observation error staying within $\pm 1.2\%$ of each individual current rms value. The absolute error value is calculated at each sample within a given time range, subtracting simulated from estimated values. The error normalization is done with individual current rms since these currents are composed of dc, fundamental and high (switching) frequency components. Probability density functions (PDF) are calculated by using either “normal” or “kernel” distributions.

Fig. 4. Simulated interleaved currents in SM1 (a), timeseries of simulated and observed interleaved currents (b,d,f) with corresponding distribution of observation error (c,e,h) under **equal** R, L, C parameters and timeslots of enabled/disabled interleaved current balancing control.

To verify that the current balancing can be implemented in a real system, where all internal components are subjected to manufacturing tolerances, the next numerical test is done with unequal circuitry parameters within each SM. The following simulation test shows similar zones (cf. Fig. 4) with active and inactive interleaved currents balancing loops. However, this time the R, L, C parameters of each SM in ISM-MMC have

randomly distributed values. The parameter tolerances are limited by 30% of their nominal values (cf. Table I). Accounting for these tolerances in the simulation is made by generating random numbers with a Gaussian distribution and confidence interval of $\pm 4\sigma$. For example, equivalent resistances per HB-leg of SM1 (upper arm) are [229.3, 252.7, 228.5] mΩ, inductances [2.3, 2.4, 2.8] mH and capacitance of the SM’s capacitor is 6 mF (cf. Table I). It can be noted from Fig. 5a that due to these unequal parameters within a SM, the interleaved currents cannot be perfectly aligned as it was in the case of Fig. 4a, even with activated interleaved current control. However, those currents are stabilized around their average value, demonstrating balanced, sinusoid-like waveforms. Again, once the control is disabled, the currents got imbalanced, however, with a larger magnitude due to the parameter’s inequality. This time the estimation error is almost uniformly distributed in $\pm 15\%$ of each individual current rms. Nevertheless, state observer performs quite well, following the real, simulated currents in interleaved legs.

Fig. 5. Simulated interleaved currents in SM1 (a), timeseries of simulated and observed interleaved currents (b,d,f) with corresponding distribution of observation error (c,e,h) under **random** R, L, C parameters and timeslots of enabled/disabled interleaved current balancing control.

To demonstrate estimation performance in terms of capacitor and submodule voltage, which are variables of the observer law, Fig. 6 depicts time-series with simulated and observed capacitor and submodule voltage of SM1 with corresponding observation errors. The absolute values of these errors were normalized with the corresponding rms value of the voltage, similar to interleaved currents. The observation error for capacitor voltages is close to 0, showing that inequality of the parameters does not play a relevant role here. In the case of capacitor voltage estimation, this happens mainly because capacitor voltage is an output of the observer and it is a

simulated value; hence, the observer can track this voltage precisely. Unlike the capacitor voltage, the submodule voltage is estimated based on arm current and simulated capacitor voltage, and it depends on the equivalent circuit of an SM (cf. Equation (15)). Despite that, as explained in Section II, the voltage drops on the R, L elements of the circuit are small compared to SM capacitor voltage. Hence relatively small mismatch in the parameters does not produce a vast estimation error.

Fig. 6. Timeseries of simulated and observed capacitor voltage (a) and submodule voltage (c) of SM1 with corresponding distribution of observation error (b) and (d) under **random** R, L, C parameters and timeslots of enabled/disabled interleaved current balancing control.

Overall, the implemented state observer-based interleaved legs current balancing control is able quite well to reach its objective, namely balancing the individual interleaved currents around their average even in the case with unequal circuit parameters. In this context, the current regulator compensates the current imbalance due to upstream control (the main contribution comes from the capacitor voltage balancing algorithm). Hence, there is always a current error present between individual interleaved leg current and the legs common average value even in the case with equal circuitry parameters. This error provokes the controller to generate a proportional voltage increment that adds to the HB-leg's average voltage. This action repeats until the estimated current does not reach the target. The current imbalance given by characteristic inequality of the composing elements (typically small due to the proper design of the converter) cannot be eliminated since the designed observer operates with rated values rather than real system parameters. An additional estimation loop can be implemented to assess the actual parameters of the SM circuit. However, this subject falls out of the scope of this paper.

V. EXPERIMENTAL TESTS

The experimental tests were carried out to demonstrate dynamic and steady-state behavior of ISM-MMC, operating with newly proposed state observer-based interleaved legs current balancing control. The tests were executed on a laboratory prototype, the view of which is depicted in Fig. 7a with its circuit diagram in Fig. 7b. The laboratory ISM-MMC has a single-phase structure with two SMs per arm ($N = 2$) and three HB-legs per SM ($K = 3$). Each SM is entirely built by a three-leg converter with attached to it dc-link capacitor (C). Ac terminals of the three-leg converter are coupled with iron-core

inductors (L). The second ports of these inductors are joined together, forming a positive terminal of an SM. The negative port is attached to the negative rail of the SM converter. The ISM-MMC operates as a rectifier, supplying power to an electronic load (i_{dc}). The ISM-MMC on its ac side is connected to a grid emulator that adjusts ac voltage to the required level and provides galvanic isolation from the grid. A controller for rapid prototyping RT Box 1 (Plexim) governs the power stage of the laboratory prototype. Measured currents and voltages enter the controller either as analog (marked in red, Fig. 7b) or as digital (marked in blue, Fig. 7b) input signals. In addition to the depicted in Fig. 7b analog measurements, the interleaved currents from SM2 (i_{21}, i_{22}, i_{23}) and SM3 (i_{31}, i_{32}, i_{33}) were sampled via RT Box 1 (are not depicted in Fig. 7b) for comparison with estimated values that are used in the new control strategy. The digital outputs of RT Box 1 provide drive circuits of power switches with PWM signals. Optical fibers are used to isolate both digital I/O of the controller from the power stage. Analog ports have galvanic isolation as well. RT Box 1 has a high-speed Ethernet connection with PC for real-time targeting via the Plecs (Plexim) model and data acquisition. The maximum sampling period of the controller is set to 20 μ s. The stored data points later have been plotted via Matlab (MathWorks). Table II provides a summary of the main parameters of the laboratory setup.

Fig. 7. View of the test setup (a) and its circuit diagram (b).

TABLE II
MAIN PARAMETERS OF THE LABORATORY TEST SYSTEM

Description	Labels	Parameters
number of SMs per arm	N	2
number of interleaved HB legs in each SM	K	3
individual interleaved leg inductor parameters	R_L, L	244 mΩ, 12.6 mH
capacitance in each SM	C	3.54 mF
dc-link split capacitance (2x)	C_{dc}	5.2 mF
rated line-to-neutral voltage (rms)	V	50 V
power factor	-	1
fundamental frequency	f	50 Hz
rated dc power and dc-link voltage	P_{dc}, V_{dc}	600 W, 200 V
carrier frequency	f_{cr}	2 kHz
sorting frequency	f_{sort}	400 Hz
observer current and voltage gains	l_i, l_v	$10 \text{ H}^{-1}, 20000 \text{ s}^{-1}$

The dc current step from 0 to 3 A has been introduced to the test ISM-MMC to demonstrate the dynamic performance of the implemented observer and associated with that interleaved current regulator. Based on the state observer, the discussed interleaved current balancing loops were always active during the conducted experiment. Fig. 8 and Fig. 9 depict the main input, output and internal characteristics of ISM-MMC, namely supplied ac power (active and reactive), ac phase current, dc-bus voltage, capacitor voltages, arm currents and individual currents of SM2 (cf. Fig. 7). It should be stressed here that the quantities presented by Fig. 8 and Fig. 9 are directly measured or derived by employing common calculus rules (Kirchhoff's current law, power calculation, etc.). It is well visible from these pictures that all quantities are well balanced and reach their steady-state value after some transient time that finishes around 2.5 s of the plot scale. The key point here to be checked is the distribution of interleaved currents within the SM (cf. Fig. 9a). In fact, they are pretty nicely balanced, having a minor mismatch at the peaks of sinusoids, provoked by circuitual parameter inequality. However, as will be demonstrated shortly, the rms values of these currents are pretty close.

Fig. 8. Dc current step. Active and reactive powers (a) supplied by the grid (solid traces) along with their reference values (dashed lines); dc-link voltage (b) – measured value (solid trace) and its reference (dashed trace); ac phase current (c); measured capacitor voltages (d) from each submodule of ISM-MMC (solid traces) along with its $\pm 5\%$ tolerance band and mean value (dashed lines).

Fig. 9. Dc current step. Measured currents through interleaved legs of the submodule SM2 (a) and arm currents of ISM-MMC (b).

To visualize the dynamic behavior of the implemented state observer, measured interleaved current of the first HB-leg from Fig. 9a is plotted versus its estimate (cf. Fig. 10a). The corresponding error distribution over the steady-state range (from 2.5 s to 4.5 s of the plot scale in Fig. 9a) is depicted in Fig. 10b. The normalization of the error is done based on measured rms values of the corresponding interleaved currents (left-upper corner of the plots). It is noticeable from both time-series and error distribution plots that the estimate of interleaved current fits quite well to the real waveform with absolute error in the range $\pm 20\%$ of the measured current rms. It is also visible that the errors fit quite well to Gaussian distribution. Nevertheless, even though the estimated currents cannot repeat their measured counterpart, the fact that the interleaved currents are decently balanced in Fig. 9a proves the feasibility of the proposed state observer-based interleaved current regulator.

Fig. 10. Dc current step. Measured and estimated currents through interleaved leg of the submodule SM2 (a) with corresponding distribution of observation error (b).

Fig. 11. Dc current step. Measured and estimated capacitor voltage of submodule SM2 (a) with corresponding distribution of observation error (b).

In addition to the current estimate, it is also essential to depict a similar comparison in the case of capacitor voltages (cf. Fig. 11) since the observer is built based on capacitor voltage error. This fact is particularly evident when the ac phase current is zero (open-circuit case). At this operating point, the variation of capacitor voltage is minimal and interleaved currents almost purely consist of high (switching) frequency components. In such conditions, precisely estimating interleaved currents is very difficult.

Overall, the dynamic and steady-state behavior of the newly proposed interleaved currents balancing strategy is stable and predictable.

VI. CONCLUSION

A current sharing problem in interleaved SMs of ISM-MMC originated from the upstream control actions is solved in this paper with new current sensorless method, by introducing a new state observer-based feedback control that operates individually with each SM. Observers typically add complexity to the control system and demand high computational resources, especially in the highly modular structure of ISM-MMC. However, the implemented state observer employs only a few mathematical operations and can fit an entry-level

controller. In addition to that, it requires only a few measured quantities, namely capacitor voltages and arm currents that are typically sensed in classical MMC structures for operation of internal control loops. Therefore, the proposed sensorless interleaved current balancing method does not need excessive and costly current measurements of each interleaved current. It can adequately share the arm current among interleaved legs of a SM, compensating the primary cause of the high current imbalance, namely actions of capacitor voltage balancing technique. Both numerical simulations and experimental tests verified the steady-state and dynamic performance of the introduced current balancing method. It has been shown thought that the implemented observer does not provide correct current estimations when the circuit parameters vary from their observer preset values. However, in a good converter design, the variance of the element parameters is limited; hence the observer-related estimation error is also limited. In this case, the potential current imbalance due to parameter variance can be effectively bounded. On the other hand, additional observer loops can be implemented trying to estimate the true value of the circuit parameters.

REFERENCES

- [1] F. Briz, M. Lopez, A. Rodriguez, and M. Arias, "Modular power electronic transformers: Modular multilevel converter versus cascaded h-bridge solutions," *IEEE Ind. Electron. Mag.*, vol. 10, no. 4, pp. 6–18, Dec. 2016.
- [2] L. Zhang *et al.*, "Modeling, control, and protection of modular multilevel converter-based multi-terminal HVDC systems: A review," *CSEE J. Power Energy Syst.*, vol. 3, no. 4, pp. 340–352, Dec. 2017.
- [3] Y. S. Kumar and G. Poddar, "Balanced Submodule Operation of Modular Multilevel Converter-Based Induction Motor Drive for Wide-Speed Range," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3918–3927, Apr. 2020.
- [4] M. A. Perez, S. Ceballos, G. Konstantinou, J. Pou, and R. P. Aguilera, "Modular Multilevel Converters: Recent Achievements and Challenges," *IEEE Open J. Ind. Electron. Soc.*, vol. 2, pp. 224–239, Feb. 2021.
- [5] Y. Zhong, N. Roscoe, D. Holliday, T. C. Lim, and S. J. Finney, "High-Efficiency mosfet-Based MMC Design for LVDC Distribution Systems," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 321–334, Jan. 2018.
- [6] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 18–36, 2015.
- [7] S. Milovanovic and D. Dujic, "On Power Scalability of Modular Multilevel Converters: Increasing Current Ratings Through Branch Paralleling," *IEEE Power Electron. Mag.*, vol. 7, no. 2, pp. 53–63, Jun. 2020.
- [8] A. Viatkin, M. Ricco, R. Mandrioli, T. Kerekes, R. Teodorescu, and G. Grandi, "Modular Multilevel Converters Based on Interleaved Half-Bridge Submodules," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2021, pp. 440–445.
- [9] A. Viatkin, M. Ricco, R. Mandrioli, T. Kerekes, R. Teodorescu, and G. Grandi, "A Novel Modular Multilevel Converter Based on Interleaved Half-Bridge Submodules," *TechRxiv*, pp. 1–9, Jul. 2021, doi: 10.36227/techrxiv.15022920.
- [10] K. Siri, C. Q. Lee, and T. E. Wu, "Current Distribution Control For Parallel Connected Converters: Part I," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 28, no. 3, pp. 829–840, 1992.
- [11] D. Liu, A. Hu, G. Wang, and W. Hu, "Current Sharing Schemes for Multiphase Interleaved DC/DC Converter with FPGA Implementation," in *Proc. Int. Conf. Elect. Cont. Eng.*, 2010, pp. 3512–3515.
- [12] J. Burkard, M. Pfister, and J. Biela, "Control Concept for Parallel Interleaved Three-Phase Converters with Decoupled Balancing Control," in *Proc. Europ. Conf. Power Electron. Appl.*, 2018, pp. 1–9.
- [13] A. Viatkin, M. Ricco, R. Mandrioli, T. Kerekes, R. Teodorescu, and G. Grandi, "Current Balancing Control for Interleaved Half-Bridge Submodules in Modular Multilevel Converters," *TechRxiv*, pp. 1–9, 2021, doi: 10.36227/techrxiv.16645861.
- [14] J. Gordillo and C. Aguilar, "A Simple Sensorless Current Sharing Technique for Multiphase DC-DC Buck Converters," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3480–3489, May 2017.
- [15] R. F. Foley, R. C. Kavanagh, and M. G. Egan, "Sensorless current estimation and sharing in multiphase buck converters," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2936–2946, 2012.
- [16] Z. Lukić, S. M. Ahsanuzzaman, Z. Zhao, and A. Prodić, "Sensorless self-tuning digital CPM controller with multiple parameter estimation and thermal stress equalization," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3948–3963, 2011.
- [17] A. Elbanhawy, "Current Sharing in Multiphase Converters Using Temperature Equalization," in *Proc. IEEE Power Electron. Spec. Conf.*, 2005, pp. 1464–1468.
- [18] P. Hu, R. Teodorescu, and J. M. Guerrero, "State observer based capacitor-voltage-balancing method for modular multilevel converters without arm-current sensors," *Int. J. Electr. Power Energy Syst.*, vol. 113, pp. 188–196, Dec. 2019.
- [19] S. R. Sanders and G. C. Verghese, "Lyapunov-based control for switched power converters," *IEEE Trans. Power Electron.*, vol. 7, no. 1, pp. 17–24, Jan. 1992.