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Surface Field Dynamics in dc Film Capacitors under an Impulse Voltage Perturbation

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ABSTRACT

For metalized polymer film capacitors, the dynamics of electric field on the electrode surface and its resulting energy dissipation influence the onset and scale of breakdown discharges within the capacitor unit, which in turn is indicative of the reliability and lifetime. To gain an understanding of the dependence of surface electric field on key system parameters, an equivalent circuit model is developed to simulate the temporal evolution of the electric field distribution within a dc film capacitor subjected to an external impulse electric stress. A mosaic pattern of electrode segmentation is taken into account by means of an effective surface resistance and its effects on surface electric field and energy dissipation are computed numerically. Also considered are the effects of the number of electrode segments across a given length. In addition, electric energy dissipation is calculated to assess the level of possible temperature rise within the capacitor. By addressing these two issues, it is shown that the numerical code developed and its underlying methodology can serve as a complimentary tool to the present practice of capacitor designs and performance assessment.

1 INTRODUCTION

THERE is at present a considerable drive to improve the maximum energy density and device reliability for power film capacitors, largely because of their very wide range of applications such as power factor correction, power distribution filtering, traction drives, pulsed power drive, laser energization, and space based application [1–4]. Extensive research and development at both industrial and university laboratories have seen numerous technology advances in the past 20 years, an example of which is the significant enhancement of the maximum electric stress realized by the conception of metalized polymeric film capacitors [3, 4]. Through a predominately experimental approach, various aspects of metalized film capacitors have been studied, for instance the electric, thermal, and chemical properties of capacitor dielectrics [5–7], the electric and chemical properties of liquid impregnants [3, 8, 9], and waveforms and peak values of electric stress [10–12].

These advances of power capacitor technology have however experienced a marked slow-down recently. This is perhaps in part due to the growing magnitude of influential system parameters that become increasingly time-consuming and expensive to optimize experimentally. On the other hand, improvement in the technology of one individual capacitor component is now much less likely to make significant impact on capacitor performance than in the past, because other component technologies need to be improved themselves and optimized collectively. This situation is further compounded by the fact that there is a lack of adequate theoretical guidance to the present experimental ef-

forts. It is therefore highly desirable to develop appropriate theoretical models for film capacitors.

A rigorous simulation requires simultaneous computation of slow-varying fields, fast transients, thermal evolution, and discharge ignition and dynamics in three dimensions [13]. This is clearly a formidable task and will take many progressive steps of improvement in their physical and numerical models for such a 3D simulation to be viable on today's computers. As a first step, we consider in this paper an equivalent circuit model of metalized film capacitors based on certain simplifying approximations to permit a computation task, routinely repeatable on a PC, and provide a quantitative evaluation of capacitor performance for different combinations of system parameters. This will be a useful aid for capacitor designers and manufacturers, because it provides an additional assessment tool of different aspects of capacitor design. The development of such simple theoretical models also allows removal of less important features of capacitor performance as well as introduction of more important physics into future and more sophisticated capacitor models.

For metalized film capacitors, the electric field and its distribution on the surface of capacitor electrode coatings (the interface between air and an electrode coating layer) influence very significantly the onset and the subsequent development of surface breakdown. The latter in turn contributes to capacitor reliability that can be achieved. On the other hand, surface electric fields also lead to electric energy dissipation via ohmic losses and this results in a temperature rise within the capacitor unit. It is known that capacitor operation at elevated temperature

reduces the capacitor life considerably [14] and therefore energy dissipation is an important indicator of achievable capacitor lifetime. To this end, it is useful to assess our equivalent circuit model through its application to these two important indicators of capacitor performance. In this paper, the equivalent circuit model will be established first with formulation of appropriate circuit equations in Section 2. To assess its validity, the model will be used in Section 3 to simulate a dc film capacitor whose operation can be understood reasonably easily. Then in Section 4, it will be employed to calculate the surface electric field and energy dissipation in a dc film capacitor under an impulse voltage perturbation that mimics an imposing breakdown event originating from an externally connected power system. Finally in Section 5, observations from numerical examples will be summarized to provide insights into their possible implications to capacitor designs.

2 AN EQUIVALENT CIRCUIT MODEL OF FILM CAPACITORS

A power film capacitor typically consists of a few thousand flattened polymer layers stacked together and immersed in an impregnation medium (silicon oil or insulating gas) enclosed in a packaging case unit [15]. As shown in Figure 1(a), each flattened polymer layer is coated on one side with a thin metallic film, which has one of its side edges connected to an electrode terminal and the other insulated with a side margin. These side margins are arranged to be on alternating sides of the stacked polymer layers such that the metallic coatings are connected alternatively to two external electrode terminals [3, 4, 14, 16].

Figure 1. (a) A section of a typical polymer film capacitor; and (b) a simplified single-layer film capacitor model.

To bring out the underlying fundamentals of capacitor performance without unnecessary computational complication in this first study, we consider a simplified capacitor configuration consisting of a single polymeric layer to allow a one-dimensional simulation. This is illustrated in Figure 1(b). The presence of the impregnation medium and the case is ignored. Also neglected are thermal effects. Furthermore we assume that the polymeric film is deposited on both sides each with a thin metallic coating which is then connected to an external voltage. Thus the top and bottom metallic films act as the electrodes for the single-layer film capacitor. The electrode materials are however assumed to be resistive rather than perfectly conductive. This allows them to be described by means of surface resistors in equivalent lumped circuit models of film capacitors.

Figure 2. (a) A simplified model film capacitor with its patterned electrode coating and side margins; and (b) a representation of one stripe of its electrode area by means of an array of mosaic segments.

Figure 3. An equivalent circuit model for a single layer film capacitor.

Electrode coatings in power capacitors usually are segmented and their segmentation can be decomposed into inter-connected square segments each having the same mosaic design as shown in Figure 2(a) [14, 16, 17]. This allows us to describe each one of them with a lumped surface resistor of identical resistance. As a result, a two-dimensional network of identical lumped resistors may be used to describe one electrode layer. Based on the above model, a horizontal stripe of the capacitor electrode coating with a width equal to the size of one electrode segment can be divided by an array of identical segments as shown in Figure 2(b). Since there are two electrode coatings, each on one side of the polymer film, they are modeled by two parallel arrays of series-connected identical resistors, each having the same surface resistance R_s , as shown in Figure 3. To account for the presence of the polymeric film, a series of shunt capacitors also are added to connect the two arrays of lumped resistors.

In Figure 3, R_e represents the resistance from the electrode edge to the external voltage source, which in the case of practical film capacitors is the resistance from the edge of the metallic coating, through the end-spray, to one terminal of the voltage source. Resistance of the capacitor's external connection usually is much lower than the surface resistance of the electrode. If the surface resistances of the first and the last mosaic elements are absorbed into the two end resistors, respectively, in the lumped circuit of Figure 3, R_e may be approximated by R_s . It should be mentioned that the equivalent circuit of Figure 3 only models one stripe of a single-layer film capacitor. Nevertheless since this is a one-dimensional model, the remaining part of the single-layer film capacitor of area $W \times L$ may be considered as being charged up by separate but identical voltage sources. Their behavior should therefore be at least very similar to that of the single-layer film capacitor, especially the electric field distribution.

For numerical examples discussed here, the length of the capacitor

stripe is fixed to 15 cm and divided by m divisions to form an array of m square segments. Thus every lumped resistor used in Figure 3 takes the value of the surface resistance of one segment. Depending on the mosaic pattern used, the surface resistance is between 50 and 200 Ω although surface resistance as high as 1 k Ω has been considered [16, 17]. Note that large surface resistance may lead to large electric energy dissipation on the electrode coatings. Thus a small nominal surface resistance of $R_s=50 \Omega$ is assumed, although the effects of different surface resistance will be assessed through numerical examples in the following two sections. On the other hand, the capacitance of each shunt capacitor depends on the number of segments in the length of L . Assuming all individual shunt capacitors have the same capacitance, we have

$$C_m = \epsilon_0 \epsilon_r m \frac{\left(\frac{L}{m}\right)^2}{d} \quad (1)$$

where d is the film thickness and ϵ_r is its relative permittivity. For all cases studied here, $d=10 \mu\text{m}$ and $\epsilon_r=2.3$. Thus

$$C_m = \frac{4.5799 \times 10^{-8}}{m^2} \quad (2)$$

3 CHARGING PROCESSES IN A dc FILM CAPACITOR

Circuit equations for the equivalent circuit of Figure 3 are formulated and further discretized for numerical coding. The resulting computer code takes typically a few minutes of CPU time on a Pentium III 550 MHz to complete the simulation of charging processes in a power film capacitor of given parameters. To validate the numerical code developed, it is used to simulate the charging processes of the simplified single-layer capacitor of Figure 2 when it is subjected to an external dc voltage of 2.5 kV. dc operation of film capacitors can be understood reasonably well in an intuitive and straightforward fashion and so it provides a means to assess the validity of our numerical code.

The characteristic time constant of the circuit, an effective RC , in Figure 3 can be estimated approximately by grouping together all individual shunt capacitors into a single lumped shunt capacitor C_T , and all series resistors into a single lumped series resistor R_T . It can be shown that

$$C_T = \epsilon_0 \epsilon_r \frac{L(L/m)}{d} = \frac{4.5799 \times 10^{-8}}{m} \quad (3)$$

$$R_T = 2R_e + 2(m-1)R_s \approx 2mR_s$$

So with $R_s=50 \Omega$, the time constant is approximate, regardless of the segmentation number m . Therefore we expect the charging process of the circuit in Figure 3 to have a characteristic time constant $\sim 5 \mu\text{s}$. This requires the time step used in our computation to be a very small fraction of 5 μs .

Figure 4 is a plot of capacitor voltage normalized to the applied voltage $V_0=2.5 \text{ kV}$, vs. x , the distance from the left-hand edge of the capacitor along its electrode surface, at $t = 0.1 \tau_0$. It is seen that during the charging processes, the capacitor voltage has a spatial distribution and therefore there exists a finite surface electric field. The maximum surface electric field occurs at the edge of the electrode coating. Also if there are more mosaic segments over a given electrode length (and hence larger m), this surface electric field tends to be larger. When the

Figure 4. Spatial distribution of normalized capacitor voltage at $t = 0.1 \tau_0$.

capacitor is fully charged, its voltage will become the same across the electrode surface and so the surface electric field will reduce to zero eventually.

Figure 5. Peak surface electric field reached for different segmentation number.

The surface electric field at the capacitor edge reaches its peak at the beginning of the discharge processes. Figure 5 is a plot of the peak surface electric field as a function of segmentation number. As shown, the peak surface electric field can reach 283 V/cm at $m=17$, well below the breakdown field of $\sim 3 \text{ kV/mm}$ in air [18]. However experiments done with contaminated glass and porcelain suggest that a surface electric field as low as 300 V/cm can assist an initially small spark surface discharge to become an elongated surface flashover discharge and cause the insulator to fail [19]. Given that the mosaic pattern and surface defects may enhance the local surface field considerably, a surface field of 283 V/cm for the $m=17$ case implies that field assisted elongation of surface discharges can be an important issue for film capacitors. It should be noted that capacitance reduction due to evaporation of the electrode coating can be controlled and possibly minimized subsequently with smaller segment area (hence larger m). Thus when segment number over a given film length is determined in capacitor design, there is a

trade off between minimization of surface electric field and capacitance reduction. It is also found that when operated at dc, the peak surface electric field reached in film capacitors is independent of the surface resistance. Thus for dc operation, surface resistance is a free design parameter as far as the surface electric field is concerned.

Figure 6. Temporal evolution of power dissipated on electrode coatings for different values of surface resistance.

The establishment of surface electric field leads to power dissipation on the capacitor electrode. The resulting dissipated heat is an important quantity for estimate of the extent of temperature rise within the capacitor unit. This allows one to address a number of closed related issues, for instance that of thermally assisted decoupling of distant current gates [14]. In Figure 6, the power dissipated on the two electrode coatings is plotted as a function of time for different values of surface resistance for $m=17$. It is shown that low surface resistance leads to a large instantaneous dissipation power with a rapid decrease from its peak value. On the other hand, large surface resistance results in a comparatively low peak value of the instantaneous power but gradual reduction from the peak power. In other words, a low level of surface resistance leads to strong and short power dissipation whereas large surface resistance results in gentle and lengthy power dissipation.

The time-averaged impact of the power dissipation in Figure 6 may be appreciated by means of the eventual energy density. It is found that the energy density is independent of surface resistance. Also as the segment number increases from $m=5$ to $m=17$, the energy density is found to reduce monotonically from 0.644 to 0.637 mJ/cm², a reduction of 1.1%. This implies that for film capacitors with a large segment number, the induced temperature rise is only slightly less than that with a small segment number.

From numerical results shown in Figures 4 to 6, the surface electric field is ~ 280 V/cm and the total accumulated dissipated energy density ~ 0.6 mJ/cm². It should be noted that the peak surface field only occurs at one time instant and the energy dissipation process ceases ~ 20 μ s after charging. Thus for most cases the calculated level of surface field and dissipated energy should not cause an internal breakdown within the capacitor unit unless there are considerable defects in polymer films and their coatings or/and significant amount of heat is accumulated, or the impregnant suffers from contamination.

4 SURFACE FIELD DYNAMICS WITH AN IMPULSE VOLTAGE PERTURBATION

It has been established that for typical system parameters of film capacitors their charging processes, when subjected to a dc voltage, do not necessarily lead to breakdown within the capacitor, unless the local electric field is enhanced significantly and a considerable amount of heat is accumulated. This explains, at least in part, why dc capacitors are in practice reasonably reliable with long lifetime. However for dc capacitors used in power systems, they are also subject to impulse electric stresses resulting from either a failure of an externally connected capacitor or switching signals propagating in the external network. Therefore it is important to assess how film capacitors react electrically to an external pulse signal [11].

Figure 7. Evolution of capacitor voltage for $m=17$, $\tau=0.1$ μ s and $V_m = 0.1V_0$.

We consider an impulse voltage signal superimposed onto the nominal dc voltage and the total voltage applied to the terminals of the capacitor is given by

$$V_s = V_0 + V_m \exp \left[-\frac{t^2}{\tau^2} \right] \quad (4)$$

For all numerical examples discussed here, $V_0=2.5$ kV. Figure 7 shows the capacitor voltage across the capacitor film as a function of time for $V_m/V_0=0.1$, $\tau=0.1$ μ s, $m=17$ and $R_s=50$ Ω . As it can be seen, there is a spatial variation in capacitor voltage and as such there exists a finite surface electric field. The largest surface field is likely to be near the capacitor edge, similar to the dc case as shown in Figure 4.

Further numerical simulations confirm that the peak surface field does occur at the edge of the electrode film. It is also found that the peak electric field is in linear proportion to V_m/V_0 for cases studied for $0.5 < \tau < 2$ μ s. In Figure 8, it is shown that the largest peak field is ~ 18 V/cm for the $\tau=0.5$ μ s case at $V_m/V_0=0.1$ for $m=17$. This should be compared to the dc case of Figure 4 where the peak surface electric field at an applied voltage of 2.5 kV is ~ 280 V/cm for $m=17$. Assuming the largest peak electric field is in the ballpark of 180 V/cm when V_m/V_0 is increased from 0.1 to 1, the surface electric field is higher in the dc case than that in the impulse case for impulse duration >0.5 μ s.

Peak electric field increases with the segment number, as shown in Figure 9. This finding is consistent to the dc case shown in Figure 5, and

Figure 8. Surface electric field varies as a function of time for different impulse durations at $V_m/V_0=0.1$, $m=17$, and $R_s=50 \Omega$.

Figure 9. Peak surface field vs. segmentation number for $\tau=1 \mu s$ at $m=17$ and $V_m/V_0=0.1$.

so its trade off between the minimization of surface electric field and capacitance reduction remains the same as for the dc case. However, different from the dc case is the dependence of peak surface electric field upon surface resistance. As indicated in Figure 9, the peak surface field is higher for larger surface resistance and so this will have an impact on the overall capacitor design. Figure 10 is a more detailed illustration of the effects of surface resistance. It is shown that the high surface electric field at large surface resistance will be increased further when the impulse duration decreases.

The eventual dissipated energy density is shown in Figure 11 as a function of surface resistance. Interestingly, the $\tau=1 \mu s$ case results in the largest energy density even though the surface electric field at $\tau=1 \mu s$ is the lowest in Figure 10. This is because the total energy associated with the initial voltage impulse is large when the pulse duration is large. Consequently an impulse voltage of long pulse duration induces low peak surface electric field but results in large dissipated energy density. It is worth emphasizing that these two aspects are related to the onset of breakdown and thermal effects, respectively.

It is also of interest to note that in Figure 11 the electric energy den-

Figure 10. Peak surface electric field vs. surface resistance for different impulse durations at $m=17$ and $V_m/V_0=0.1$.

Figure 11. Energy density as a function of surface resistance for different impulse durations at $m=17$ and $V_m/V_0=0.1$.

sity decreases when the surface resistance goes up. Since energy density is proportional to the square of the surface electric field, divided by surface resistance, this is a result, mathematically, of the increment rate of surface field at large surface resistance being smaller than that of surface resistance itself in Figure 10. In terms of fundamental processes, large surface resistance, on the one hand, leads to large surface electric field at a given surface current. On the other hand, it also increases the characteristic time constant of the capacitor and so slows down the pace at which the external impulse voltage penetrates into the capacitor system of Figure 3 from its end terminals. Consequently, during the impact of the impulse voltage, shunt capacitors across the electrode coatings in Figure 3 have more time to be charged to similar voltage from one spatial point to another and so the resulting surface electric field becomes not as large. These two contrasting effects of surface resistance mean that large surface resistance does not necessarily lead to higher temperature rise under impulse stress conditions. Given also that the energy density and peak surface field depend on the surface resistance in an opposite manner, the above implies that a good balance has to be weighed carefully when choosing the surface resistance value.

Figure 12. Dissipated energy as a function of the impulse voltage.

The level of dissipated energy density in Figure 11 is small, in the region of a $\sim 2 \mu\text{J}/\text{cm}^2$, much lower than the dc case of $0.6 \text{ mJ}/\text{cm}^2$. It is conceivable that the charging period in the dc case is equivalent to the pulse duration for the impulse voltage case. For numerical examples studied for dc capacitors, the charging period is $\sim 5 \mu\text{s}$ compared to $\sim 1 \mu\text{s}$ of the pulse duration in the impulse case. More importantly, the capacitor voltage is charged to V_0 in the dc case whereas for the impulse case it is $0.1V_0$. These contribute to the small energy density figures in Figure 11. For large V_m/V_0 values, Figure 12 shows considerably increased energy density to $0.14 \text{ mJ}/\text{cm}^2$ at $V_m/V_0=0.5$.

5 CONCLUSION

An equivalent circuit model has been developed for metalized film capacitors used in power systems. Based on a simplified film capacitor model, the surface electric field and associated dissipated power have been calculated for dc film capacitors subjected to an external impulse voltage. It has been established that segmentation number and surface resistance influence the level of surface electric field and dissipated power. It has also been shown that pulse duration of the impulse voltage also can affect significantly the surface electric field and dissipated energy density.

While the work presented here is aimed at generic features of capacitor performance without specifications on impulse waveform and their possible repetitions, these practical issues can be taken into account easily with our code. Hence the numerical code developed and its underlying methodology can serve as a complementary tool to the present practice of capacitor design and performance evaluation. Issues to develop our equivalent circuit model further include an extension to two dimensions so as to permit the inclusion of surface plasmas. These will be addressed in a future paper.

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