Supporting Information for

Sub-10 nm Carbon Nanotube Transistors

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1. Methods

Local bottom gate fabrication on 200 mm wafers. In a 200 mm silicon production fab, beginning with intrinsic Si wafers, 1 μm thick SiO_2 was thermally grown at 1050 $^\circ\text{C}$ in a wet oxidation furnace. The wafer was then spin-coated with photoresist and patterned using an ASML Deep UV stepper. High power reactive ion etching with a mixture of CHF_3 and Ar for 150 sec was used to remove ~ 350 nm SiO_2 followed by photoresist stripping in oxygen plasma. Tungsten (W) was then sputter deposited to a thickness of ~ 500 nm, filling the trenches and coating the wafer. Next, the wafer was polished to planarize the W in a Westech CMP system. 30 $\text{\AA}$ HfO_2 was then deposited at 200 $^\circ\text{C}$ in a Cambridge Nanotech Fiji atomic layer deposition system to cover the whole wafer and an HBr based RIE process was used to etch open the contact pad to the gate.

Carbon nanotube growth and transfer. Single-walled carbon nanotubes (CNTs) were synthesized on ST-cut quartz substrates in a chemical vapor deposition (CVD) tube furnace at 900 $^\circ\text{C}$ using 1000 sccm forming gas (95 % Ar, 5 % H_2) bubbled through ethanol held at 5 $^\circ\text{C}$ as the hydrocarbon precursor. The CNTs nucleated in predefined catalyst particle areas and proceeded to grow in parallel arrays, laterally across the quartz surface with final lengths of approximately 50 μm (distance between catalyst lines) as shown in the scanning electron microscope (SEM) image of Fig. S1a. Following CNT synthesis, the quartz substrates were coated with 100 nm electron-beam evaporated Au and then the entire Au film (with CNTs attached) was transferred to the W local bottom gate wafer using Revalpha thermal tape, as described elsewhere^{1,2}. A low magnification scanning electron microscope (SEM) image of the transferred CNTs is given in Fig. S1a.

Device fabrication. After fabrication of initial contacts that were spaced by 3 μm between source and drain (and all CNTs were etched away outside of the 3 μm (500 nm wide) channel area in an oxygen plasma), a Cascade Summit semi-automated probestation was used to quickly test hundreds of devices to determine if a nanotube was present and if it was semiconducting. The final fabrication of the different source and drain electrode layers then proceeded on the identified semiconducting locations. The SEM image in Fig. S1c shows an example set of devices with different channel lengths that were obtained by the 10 nm staggered offset between the source and drain contact layers. Enough redundancy was included in the design to

account for both the expected widening of contacts from slight overexposure/development and overlay mismatch.

Electrical characterization. Electrical characterization was carried out in air, with no additional passivation or annealing treatments. A Lakeshore probestation was used along with an Agilent B-1500 Semiconductor Parameter Analyzer for measurements.

Nanotube diameter. To ascertain the diameter of the CNT, atomic force microscope (AFM) imaging was performed at several positions along the nanotube, yielding images like the one in Fig. S1b. Because the nanotube was several microns long, high quality AFM images could be obtained along the CNT, both in the channel region for the long channel devices and further away from the devices. The final extracted diameter was an average of hundreds of section measurements from different images. The diameter of the CNT from these AFM images is considered accurate to within ± 0.2 nm. Since all four devices reported in the manuscript are assembled on the same nanotube, this diameter is applicable to them all.

Transmission electron microscopy. Devices were prepped for transmission electron microscope (TEM) imaging using an FEI focused ion beam (FIB) and SEM system. First, a layer of ~ 200 nm thick Pt was deposited *in situ* in the FIB using the SEM electron beam. The device area was then prepared for extraction by creating a trench on either side of a ~ 300 nm thick cross-section. The cross-section piece was transferred to a grid where it was further thinned with the FIB to between 50-100 nm thickness. TEM imaging was then performed on the cross-section piece. The amorphous carbon (a-C) shown in the Fig. S1d TEM is from heavy SEM imaging of the device causing a-C to deposit.

Figure S1. (a) SEM image of aligned CNTs after transfer onto substrate with local bottom gates. CNTs are $\sim 50 \mu\text{m}$ long, extending from one catalyst stripe (bright, vertical line) to another. (b) AFM image of nanotube used for diameter extraction. Average diameter was obtained from several AFM images. (c) SEM image of a set of devices on a single CNT showing how the staggered source/drain contacts enable a variety of channel lengths, including sub-10 nm. (d) Cross-sectional TEM image showing the sidewall structure of the contacts and a sub-10 nm channel.

2. Contact Resistance Extraction

Because a set of transistors with different channel lengths were fabricated along the same CNT, useful information can be obtained by plotting the total resistance (R_{tot}) versus channel length—similar to a transfer length model plot. Figure S2 is the R_{tot} vs. L_{ch} plot for the CNT that the 9 nm transistor was constructed on. By applying a linear fit to the data points and extrapolating to zero channel length, the contact resistance ($2R_c$) is extracted to be 13.2 k Ω . This $2R_c$ is comparable to other recent reports of CNT transistors using Pd contacts.¹ Another useful extraction from the Figure S2 plot is to extrapolate where the linear fit crosses the $R_{tot} = 0$ (x-axis) giving the transfer length of transport at the contacts. However, this transfer length extraction (which yields ~ 150 nm) relies on the assumption that transport in the CNT under the metal contacts is the same as transport in the channel portion of the CNT—an assumption that cannot be confirmed and is likely not accurate. Therefore, the transfer length will be smaller than the 150 nm extracted from the plot.

Figure S2. Plot of the total resistance versus channel length from one of the CNTs used in the study. R_{tot} was extracted from the output characteristics at -1 V overdrive on the gate. Extrapolation to zero channel length of a linear fit to the data provides the contact resistance, which is comparable to similarly contacted devices in a previous report¹.

3. Gate Hysteresis and Gate Leakage Current

Comparison of the subthreshold characteristics for a set of devices in Fig. 2a of the manuscript shows slight shifts in threshold voltage (V_{th}). These V_{th} shifts are primarily components of the hysteresis in the devices, as shown in Fig. S3a. Therefore, it is not possible to determine the effect that scaling has on V_{th} for these CNT transistors. Another important aspect of the devices to consider is the gate leakage current. With an extremely thin high-k dielectric of approximately 3 nm and source/drain contacts that overlap the gate, there is a significant chance for leakage in the devices. The typical gate leakage current in this work is shown in Fig. S3b for an 18 nm channel length transistor. While beyond ± 1.5 V the leakage begins to dominate, within the $-1.5 \text{ V} < V_{gs} < 1.5 \text{ V}$ window the gate leakage is inconsequential.

Figure S3. (a) Gate voltage sweep from -1.5 V to 1.0 V and back on 18 nm device, yielding hysteresis of 375 mV. (b) Drain and gate currents for an 18 nm device showing the operating range for the 3 nm HfO_2 as $|V_{gs}| < 1.5 \text{ V}$.

4. Scaling Impact on Output Characteristics

Most of the emphasis regarding the impact of scaling to sub-10 nm has been on the *off*-state metrics, such as inverse subthreshold slope because these are traditionally more acutely affected by scaling. However, there is also considerable change in the *on*-state performance of a scaled CNT transistor—in this case, improved performance. As shown in the Fig. S4 comparison, the *on*-current nearly doubles when scaling the channel from 320 nm down to 9 nm, as does the transconductance. This improvement from L_{ch} scaling primarily relates to suppression of scattering in the channel, with the CNT reaching the nearly ballistic transport limit.

Figure S4. Output characteristics of shortest (9 nm) and longest (320 nm) channel devices showing improved *on*-state performance with enhanced current while maintaining clear saturation at much lower drain-source bias.

5. Numerical Simulation with Gate Modulation of Contacts

To simulate the I-V characteristics of bottom-gated CNT transistors, a real-space 3-D, self-consistent Schrödinger-Poisson solver based on the Non-equilibrium Green's Function (NEGF) formalism³ and the finite element method (FEM) and including electron-phonon scattering was used.⁴ The electrical properties of each carbon atom are represented by a single p_z -orbital with nearest-neighbor hopping parameters $V_{pp\pi} = -3.2$ eV.

The simulation domain (Fig. S5) closely matches the experimental structure and forms a 3-D box of size $6 \times 6 \times (5 + L_{ch})$ nm³: all the considered CNTs have a diameter $d_{CNT} = 1.33$ nm (band gap $E_g = 0.694$ eV).

They are deposited on a $t_{ox} = 3$ nm-thick HfO_2 layer with a relative dielectric constant $\epsilon_R = 18$ corresponding to an EOT of 0.65 nm (as observed in the experimental metal-insulator-metal structures). The back gate covers the channel region as well as the source and drain contacts. The value of $V_{pp\pi}$ and therefore E_g was optimized to obtain a good fit of the minimum leakage current of the CNT transistor. The total structure length is set to $L = 5 + L_{ch}$ nm with $L_s = L_d = 2.5$ nm on each side of the channel to model source and drain extensions. As explained in the manuscript, the doped source and drain extensions are added to demonstrate the impact that carrier transport in the contacts has on the performance of sub-10 nm CNT transistors. Additionally, since the gate overlaps the contacts in the present devices, there is potential for the gate to modulate carrier concentration in the contacts, as recently observed for metal-graphene contacts.⁵ Therefore, the inclusion of these doped source/drain extensions is also a way of considering the impact of such carrier modulation.

If we assume that x is the current flow direction, then at $x = 0$ and $x = 5 + L_{ch}$, two Schottky contacts with a barrier height $\Phi_B = 0.1$ V are inserted. To match the subthreshold region of the $L_{ch} = 9$ nm device, the gate contact should be able to modulate the source and drain extensions at $0 \leq x \leq 2.5$ and $L_{ch} + 2.5 \leq x \leq L_{ch} + 5$, otherwise SS is too large (without the source/drain extension modulation). To achieve this without artificially increasing the channel length to $L_{ch} + 5$, we dope these two regions with acceptors (doping concentration: $1/4$ doping atom per nm homogeneously distributed over all carbon atoms) so that they behave as metallic contact extensions whose electrostatic potential can be slightly raised and lowered by the gate contact. What is assumed is that in reality extra charges are directly transferred from the metallic contacts into the CNT channel at the interface. The electrostatic potential in the source/drain extension areas is therefore no more fixed, but is coupled to the gate contact that can modulate its behavior. However, due to the doping, the coupling between the gate and the source/drain extensions is not as strong as between the gate and the intrinsic CNT channel.

Finally, between the source and drain contacts, the CNTs are surrounded by an air box with $\epsilon_R = 1$, which is explicitly taken into account in the simulation domain so that gate-induced electric field lines can propagate around the CNT. While these simulations only provide a potential explanation for the impressive

scaling behavior observed, they suggest that in ultra-small devices, greater understanding of transport at metal-CNT contacts is required to accurately simulate device performance.

Figure S5. Schematic of structure used in numerical simulations.

Figure S6. Results from the numerical simulation (fit) plotted with the subthreshold curves of a 9 nm CNT transistor.

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