Supporting Information

Solution-Based TiO₂-Polymer Composite Dielectric for Low Operating Voltage OTFTs

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1. Complete References 3, 5, 7

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2. Experimental Procedures

Synthesis of the PVP solution (5 wt%), TiO₂ precursor and PVP composite solution:

In order to synthesize the TiO₂ precursor and PVP ($M_w = 25,000$, Sigma-Aldrich) composite solution, PVP, poly(melamine-co-formaldehyde) methylated/butylated ($M_n = 637$, Aldrich), and propylene glycol methyl ether acetate (PGMEA) ($M_w = 132.16$, Fluka) were mixed in a weight ratio of 2 : 1 : 37. The cross-linked PVP solution was stirred for 24h at room temperature. The TiO₂ precursor was mixed from titanium (IV) butoxide ($M_w = 340.32$, Sigma-Aldrich) and acetyl acetone ($M_w = 100.12$, Fluka), at a molar ratio of 1:1. The cross-linked PVP solution and TiO₂ precursor, at a ratio of 9:1 (w/w), were mixed by stirring until they formed a gelatin. In order to avoid the aggregation of PVP solution and TiO₂ precursor due to rapid cross link, the solution was stirred under low temperature (2 °C). The gelatin was dissolved in ethanol ($M_w = 46.07$, DAE JUNG) at a ratio of 1:3 (w/w).

TFTs Fabrication: The transistors were fabricated on ITO substrates (thickness: 120 nm, sheet resistance: 15 $\Omega/\square$). The ITO substrates were subjected to 10 min washes in trichloroethylene, acetone, and isopropyl alcohol, and then rinsed with distilled water before

being dried with nitrogen. The TiO_2 precursor and PVP composite (TPC) solution was deposited on an ITO substrate as a bottom gate using spin casting at 3,500 rpm for 40 sec. The whole was then heated at 200 °C for 1 h. The TFTs device was designed as a top-contact electrode structure. The pentacene, the TFTs semiconductor was deposited by thermal evaporation in $\sim 3 \times 10^{-6}$ Torr (500 Å, 0.5 Å/s). The source and drain electrodes, Au, were deposited through a shadow mask with a channel length (L) and width (W) of 100 μm and 1,000 μm, respectively, in $\sim 3 \times 10^{-6}$ Torr (1000 Å, 5 Å/s).

Characterization Method: The current-voltage measurements were executed under ambient conditions using an Agilent 4155B semiconductor parameter analyzer. The capacitance-voltage measurements were carried out under air environment using as Agilent 4284A 1 KHz precision LCR meter. All electrical measurements were taken in dark ambient conditions. An atomic force microscope (XE-100, PSIA) was used to investigate the surface morphology. The thickness of polymer thin film was measured using K-MAC, ST2000-DLXn.

3. Device structure

Figure S1. The organic transistor structure with TiO_2 -polymer composite (TPC) thin film as a dielectric layer.

Figure S1 shows the schematic structure of top-contact organic transistors made with a TiO_2 -polymer composite (TPC) thin film as a gate insulator. The TPC dielectric layer was spin-coated with a composite solution consisting of a TiO_2 precursor and a cross-linkable PVP solution. Also, the Indium-Tin-Oxide (ITO) and Au were used as a gate electrode and source-drain electrodes respectively, and pentacene was deposited by thermal evaporation for use as semiconductor material.

4. Solubility

Figure S2. The solubility of TPC gelatins according to various solvents.

Table S1. The chemical structures of solvents shown in Figure S1.

Materials without hydroxyl group			Materials with hydroxyl group

Toluene	PGMEA	Acetone	2-propanol	Ethanol

5. Surface properties

Figure S3. The contact angles of (a) pristine PVP and (b) TPC surface. AFM images of (c) the pristine PVP (roughness rms: 0.514 nm) and (d) TPC surface (roughness rms: 1.303 nm) as a dielectric layer, (e) and (f) pentacene morphology onto the pristine PVP and TPC surface, respectively.

Figures S3(a) and (b) show the contact angles of PVP and TPC surfaces: the surface energy of the TPC composite layer was lower than that of the pristine PVP. The low surface energy

of the TPC induced the vertical alignment and dense packing of pentacene, resulting in better performance of OTFTs. Figures S3(c) and (d) show the roughness of pristine PVP and TPC surface morphology and Figures S3(e) and (f) show the pentacene morphology deposited onto the pristine PVP and TPC surfaces, measured using atomic force microscopy (AFM). The pentacene morphology on the pristine PVP surface exhibited a larger grain size and a broader void (black color) than those on the TPC surface. The lower charge carrier mobility in OTFTs that include a pristine PVP dielectric layer was caused by the obstructed electron flow in the semiconductor channel due to voids and sparse packing in the pentacene morphology. The pentacene morphology on the TPC surface (Figure S3(f)) showed small, densely packed grains.

6. Hysteresis

Figure S4. The hysteresis of OTFTs with (a) pristine PVP and (b) TPC dielectric layer.