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Interfacial Reaction Between Molten Sn-Bi Based Solders and Electroless Ni-P Coatings for Liquid Solder Interconnects

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Abstract—This paper reports on the interfacial reactions and lifetime of electroless Ni-P coatings in contact with molten Sn-Bi based solders. A layer of approximately 4 μm thick electroless Ni-P in contact with the molten Sn-58Bi solder began to fail at 48 h at temperatures between 200 °C and 240 °C. Elemental additions to modify the solder, included 1–2wt. % of Al, Cr, Si, Zn, Ag, Au, Ru, Ti, Pt, Nb, and Cu. Of these, only Cu modified the interfacial intermetallic compound growth from Ni_3Sn_4 to $(\text{Cu,Ni})_6\text{Sn}_5$, resulting in significantly decreased consumption rates of the Ni-P substrate in contact with the molten solder and increasing the lifetime of the Ni-P layer to between 430 and 716 h. Micro cracks were observed in all but the thinnest Ni-P layers, allowing the solder to penetrate.

Index Terms—Coatings, high-temperature electronics, interfaces, liquid solder interconnects, metallization, scanning electron microscopy (SEM).

I. INTRODUCTION

THERE is an increasing need of electronic assemblies and interconnections to function at higher temperatures in power, automotive and aerospace applications or in oil and gas drilling operations [1]. The conventional approach to high-temperature solder joints for electrical connection is to use solder materials with higher melting points than the standard 63Sn-37Pb solder which melts at 183 °C (e.g., 90Pb/10Sn or 96Sn/4Cu). However, these joints can still be prone to strain hardening and eventual crack formation resulting in loss of electrical continuity. As a result, using molten solder is one potential method for improving the reliability of electronic interconnections and assemblies operated at temperatures above 125 °C [2]–[5]. The principle behind using solders that are molten during operation is that fatigue damage cannot accumulate, and the solder joints can accommodate large

thermal expansion mismatches between the different metals in the assembly. Mechanical integrity is retained by other means, such as use of a polymer underfill or glob top in bare die applications. However, a number of scientific and technological issues have to be addressed for the successful implementation of such liquid solder interconnects. These include optimization of underfill or glob top materials, stable solder connections able to withstand thermal and mechanical shocks, as well as applicability to different assembly geometries. In particular, it is crucial to control the rate of intermetallic compound (IMC) formation between the solder and the contact metallizations. This is due to the fact that the formation of an IMC layer between the contact metallization and the molten solder is necessary to achieve a strong metallurgical bond when the solder is solid (during low temperature excursions), but excessive IMC formation would cause the contact metallization to be consumed too quickly leading to device failure. In previous work [6], it has been demonstrated that Nb as the contact metallization is an excellent diffusion barrier to slow down the IMC growth when used with eutectic In-Sn solder. However Nb requires sputtering or evaporation methods for deposition and hence is only suitable for niche applications.

For investigation of alternative approaches, the reactions of molten Sn-Bi based solders with contact metallizations consisting of electroless Ni-P and of Cu have been considered. Eutectic Sn-58Bi, with a melting point of 138 °C, is chosen as the basic solder alloy because it is cheaper than other low melting point solders e.g., In-Sn solder, while the volume change on melting is negative; use of an off-eutectic composition can reduce this change to zero [7]. Additionally, the properties of Sn-Bi as a solder are well known since it is used in soldering applications and offered commercially in paste form by many solder manufacturers. Ni-P and Cu were chosen because they are common contact metallizations used for both substrates and flip-chips in conventional electronic assemblies and interconnections.

Many studies have concentrated on the kinetics of IMC growth during thermal ageing between solid Sn-based solders and contact metallizations such as electroless Ni-P and Cu [8]–[10]. IMC growth kinetics in such systems are generally controlled by bulk diffusion, leading to parabolic growth kinetics. Compared to solid/solid systems, the growth kinetics of the IMCs in liquid/solid interfacial reactions are more complicated. They may involve multiple simultaneous processes, such as phase nucleation, lattice and/or grain boundary diffusion in

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the intermetallics, grain boundary grooving, grain coarsening, grain faceting, grain coalescing, and creation and/or annihilation of point defects [11]. There have also been studies of IMC formation between molten solders, such as Sn-Ag-Cu, Sn-Pb, Sn-Ag, Sn-Sb, Sn-Zn, Sn-Bi and pure Sn, and contact metallizations containing Ni-P or Cu [12]–[15]. In a few cases, the reaction times investigated extended to several hours, however, the majority of studies were short term, lasting from several seconds to under 1 h. Although IMC formation in the molten Sn-Bi/Cu and molten Sn-Bi/Ni-P systems is expected to be high from the results of these short term studies, it is important to explore the long term behavior of these systems so that the mechanism for IMC formation may be better understood, and modified to acceptable levels for molten solder interconnects.

The long term interfacial reaction kinetics between molten Sn-58Bi solder and Cu substrates and studies of the effects of elemental additions, including 1–2wt.% of Al, Cr, Cu, Si, Zn, Ag, Au, Pt, and Nb, into the basic Sn-58Bi solder, has been reported in a previous paper [16]. It was found that for the Sn-58Bi/Cu system at temperatures between 200–240 °C, grain boundary/molten channel controlled growth of η -phase (Cu_6Sn_5), was followed by diffusion-controlled simultaneous growth of the ε -phase (Cu_3Sn) and η -phase (Cu_6Sn_5). Among the different additions, only the addition of 1wt.%Zn into the basic Sn-Bi solder led to the formation of an effective barrier layer; forming γ - Cu_5Zn_8 IMC, instead of the ε - and η -phases. This caused the lifetime of a layer of $\sim 6 \mu\text{m}$ Cu at 200 °C to increase from ~ 48 h to longer than 120 h.

Electroless Ni-P coatings are well known to slow down IMC formation compared to Cu contacts [10]. In this paper, the interfacial reaction between molten Sn-58Bi based solders and Ni-P substrate is described. First, the reaction between Sn-58Bi and Ni-P was investigated to provide a benchmark for the IMC growth rates. It was found that the lifetime (defined as the time to break through to the underlying substrate) of a $\sim 4 \mu\text{m}$ thick Ni-P layer was approximately 48 h, and the failure mechanism is reported in detail. Next, a number of 1–2wt.% of additives, including Al, Cr, Si, Zn, Ag, Au, Ru, Ti, Pt, Nb, and Cu, were added into the basic Sn-Bi solder, to observe any reduction in IMC growth rates between the molten solders and the Ni-P substrate in the temperature range 200–240 °C. It was found that 1wt.% of Cu added into the basic Sn-Bi solder could significantly extend the lifetime of $\sim 4 \mu\text{m}$ thick electroless Ni-P to longer than 430 h, but that the other additions did not significantly extend the lifetime.

II. EXPERIMENTAL PROCEDURE

The Au/Ni-P substrate [Electroless Nickel Immersion Gold (ENIG)] used in this study consisted of square metal pads, 3 mm by 3 mm, on polyimide printed circuit boards (PCB) manufactured using standard commercial processes. The metal structure nominally consisted of a top layer of Au ($\sim 0.1 \mu\text{m}$), then Ni-P ($\sim 4 \mu\text{m}$), applied over an etched Cu ($25 \mu\text{m}$) foil pattern. Energy dispersive X-ray (EDX) analysis indicated that the as-received electroless Ni-P contained 8.5–10.4wt.%P. The basic eutectic Sn-58Bi solder used was a commercially available Sn-Bi solder paste. The alloyed Sn-Bi-X solders, where X stands for an additional element, with 2wt.% of Al, Si and Cr were custom prepared by a supplier. The other alloyed solders with 1wt.% of

Fig. 1. Schematic cross-sectional geometry of the Sn-Bi/Ni-P samples using the Ni-P pads on the commercial PCB boards.

Fig. 2. Schematic geometric dimensions of the lab-manufactured Ni-P substrate pads.

Zn, Ag and Au were fabricated in-house by dissolving the corresponding metallic wires or foils at temperatures from 240 to 540 °C for 10 to 30 min, and those with 1–2wt.% of Cu, Pt, Nb, Ru and Ti were fabricated by dissolving the corresponding metallic foils (for Cu, Pt, and Nb) or powders (for Ru and Ti) at 1150 °C for 8 h, in the basic Sn-58Bi solder. In order to prevent solder oxidation at 1150 °C, fabrication for the last five alloyed solders was carried out in evacuated and sealed quartz tubes.

The substrate pads were cleaned using isopropyl alcohol (IPA), acetone and finally rinsed using deionized water. The basic eutectic Sn-Bi solder paste was deposited onto the surfaces of the pads by printing through a 0.20 mm thick stencil and then reflowed in air at a peak temperature of 220 °C for 300 s. The resulting samples had a maximum solder thickness of 0.3 mm at the top of the solder dome, as shown in Fig. 1. For all the alloyed Sn-Bi based solders, 0.023 ± 0.001 g of diced solder pieces were placed on each of the Au/Ni-P pads to prepare the samples with a solder layer approximately 1 mm in maximum thickness. The solder was then covered by a thin layer of flux and also reflowed in air at the peak temperature 220 °C for 300 s. It should be pointed out that a stronger liquid flux was necessary to achieve good adhesion between the Sn56.8Bi2Al solder and the substrate. All the samples were finally cleaned using IPA, acetone and deionized water, before being placed into high-temperature storage.

For the Sn-Bi/Ni-P system, high-temperature storage of the samples was carried out in air at temperatures of 200 °C, 220 °C, and 240 °C for periods ranging from 1 to 96 h. Most of the Sn-Bi-X/Ni-P systems were stored at 200 °C and 240 °C for 48, 96, or 120 h. The Sn56.8Bi1Cu/Ni-P samples (hereafter referred to as SnBi1Cu/Ni-P) having the slowest consumption rate of Ni-P were also stored at 220 °C and for a greater range of times to obtain detailed kinetics of IMC growth. After high-temperature storage, the samples were potted and polished to obtain the metallographic cross sections. Scanning electron microscopy (SEM), together with an EDX spectrometer, was employed to characterize the interfacial structures and IMCs formed between the solder and substrate. The thicknesses of both the formed IMCs and the residual Ni-P layers were measured from the SEM

Fig. 3. SEM images of the polished cross sections for the Sn-Bi/Ni-P samples using the Ni-P pads on the commercial PCB boards: (a) as-reflowed; (b) 200 °C, 4 h; (c) 240 °C, 4 h; (d) 240 °C, 16 h; (e) 200 °C, 48 h; (f) 240 °C, 48 h. Note that the open arrows in (b) and (c) point to local micro-cracks and Sn penetration into the electroless Ni-P layer. The solid arrows in (e) and (f) indicate Sn locally penetrating through the grain boundaries towards the underlying Cu metallization.

images using an image analysis method following manual enhancement [17]. The latter was accomplished by brushing the interfaces between layers with highlighted colours. For each sample, two images were used to obtain a total of 2048 thickness measurement for each data point.

In addition, in order to explore the effect of Ni-P coating quality on the interfacial reaction, Ni-P substrate pads with the geometric dimensions shown in Fig. 2 were also prepared with the chemical content of the Ni-P coating in these lab-manufactured substrate pads similar to that of the Ni-P pads on the commercial PCB boards. Then these lab-manufactured Ni-P substrate pads were used to produce Sn-Bi/Ni-P samples with a maximum solder thickness of 1 mm, and the samples were put into high-temperature storage at both 220 °C and 240 °C for 0.5, 1, 2, 4, and 24 h.

III. RESULTS

A. Interfacial Reaction in Sn-Bi/Ni-P System

Using the Ni-P pads on the commercial PCB boards as the substrate, no Au IMC was detected at the interface of the as-reflowed samples [Fig. 3(a)] as expected, since the original Au layer dissolves rapidly into the solder during the reflow process. EDX analysis confirms that the IMC that forms is Ni_3Sn_4 . As shown in Fig. 3, the interface between the IMC and the solder are somewhat wavy. The Ni_3Sn_4 grows as faceted grains, rather than the scallops of Cu_6Sn_5 [18]. A layer of porous Ni_3P was produced between the formed Ni_3Sn_4 and the residual Ni-P.

Micro-cracks were found to occur at the surface of the Ni-P layer, resulting in Sn penetration locally into the residual Ni-P layer. This occurred for most of the samples even though their residual Ni-P layers were still rather thick after short periods of

high-temperature storage [Fig. 3(b)–(d)]. However, in the as-reflowed sample and one of the two samples stored at 240 °C for 16 h, no such micro-cracks were observed [Fig. 3(a) and (d)].

During high-temperature storage, the Ni-P layer begins to fail at around 48 h, with Sn locally penetrating through the grain boundaries and/or the micro-cracks towards the underlying Cu metallization. This means that channels exist through which the molten solder can penetrate both the formed Ni_3Sn_4 and Ni_3P layers. It was also observed that at the base of the Au/Ni/Cu pads, the Ni layer sometimes failed much earlier than elsewhere, allowing the solder to form IMCs with the underlying Cu [Fig. 3(f)]. Between 200 °C and 240 °C, there is no significant difference in the interfacial reaction, except that the growth rate of IMCs formed between the solder and the underlying Cu, once the Ni barrier has failed, is much faster at 240 °C. This compares with the observation that in the Sn-Bi/Cu system, a layer of $\sim 6 \mu\text{m}$ thick sputtered Cu can survive for 48 h at 200 °C, but only 24 h at 240 °C [16].

Fig. 4 shows the thickness of the residual Ni-P and the formed Ni_3P and Ni_3Sn_4 layers as well as the total thickness of Ni-P plus Ni_3P as a function of storage time, at all the three experimental temperatures. It should be noted that in Fig. 4, and also in what follows, the error bars stand for the 95% confidence intervals of the measured mean thicknesses, while the arrows in (d) point at the data for the samples whose total thicknesses of Ni-P plus Ni_3P are clearly lower than those for the other samples.

Excluding the experimental points for one of the two samples stored at 240 °C for 16 h, from which no micro-crack was observed [Fig. 3(d)], the average thickness of residual Ni-P layer decreased and those of both Ni_3P and Ni_3Sn_4 increased with increase in the storage time before the Ni-P layer began to fail

Fig. 4. Thickness of the residual Ni-P and the formed Ni₃P and Ni₃Sn₄ as well as the total thickness of Ni-P plus Ni₃P for the Sn-Bi/Ni-P system using the Ni-P pads on the commercial PCB boards as a function of storage time.

(48 h), at all three temperatures. However, there is no clear correlation observed between the growth rates of IMCs and the storage temperature.

Once the electroless Ni-P layer began to fail after storage for about 48 h, the average thicknesses for all the residual Ni-P and the formed Ni₃P and Ni₃Sn₄ seems unchanged with further increases in the storage time up to 96 h. This can be readily understood because the IMCs then mainly grew around the underlying Cu layer and this type of IMC was not included in Fig. 4.

Using the lab-manufactured Ni-P substrate pads, the interfacial reaction products were the same as those in the samples using the Ni-P pads on the commercial PCB boards. However, no apparent pores were found to form within the Ni₃P layer, and no micro-cracks were observed at the surface of the Ni-P layer, as shown in Fig. 5. Note that the Cu layers in Fig. 5(c) and (d) detached from the samples during the cutting and polishing process. Although the average thickness of both Ni₃P and Ni₃Sn₄ are larger than those in the samples using the Ni-P pads on the commercial PCB boards, they clearly increased with increase in the storage temperature and the reaction time, if the reaction time is shorter than 24 h (Fig. 6).

B. Interfacial Reactions in Sn-Bi-X/Ni-P Systems

Among the investigated additional elements, Al, Zn, Ru, Ti, Au, Cr, Nb, Si, and Pt were not obviously effective in reducing the IMC growth rates at both 200 °C and 240 °C. After high-temperature storage for periods between 48-120 h,

the Ni-P layers had failed, with Sn locally penetrating through the grain boundaries towards the underlying Cu metallization (Figs. 7–9). Of these, Al apparently accelerated the consumption rates of both the original Ni-P layer and the formed Ni₃P layer [Fig. 7(a)]. Further observation and examination using EDX revealed that Al accumulated and oxidized at the surface of the Sn-56.8Bi-2Al solder during the high-temperature storage [Fig. 7(a)]. Zn also accumulated and oxidized at the surface of the Sn-56.8Bi-1Zn solder [Fig. 7(b)], but had no appreciable effect on the interfacial microstructure between the solder and the Ni-P substrate.

With additions of 2wt.% Ru and Ti into the basic Sn-58Bi solder, (Ru,Ni)₃Sn₇ and Ti₆Sn₅ IMCs [19], [20] were found to form and migrate towards the surfaces of the solders [Fig. 8(a) and (b)], while the addition of 1wt.% Au resulted in the formation of AuSn₄ throughout the solder [Fig. 8(c)]. In each of these cases, the additional elements did not participate in the interfacial reaction, and the interfacial microstructure was essentially the same as in the Sn-Bi/Ni-P system, as shown in Fig. 3(e) and (f).

Cr and Si slightly reduced the consumption rate of the Ni-P and the growth rate of the IMC, with some residual Ni-P left after the high-temperature storage for 48–120 h [Fig. 9(a) and (b)]. Nb and Pt did not affect the interfacial reaction between molten solder and Ni-P appreciably [Fig. 9(c) and (d)]. No Cr, Si, Nb or Pt were detected using EDX from the corresponding samples after high-temperature

Fig. 5. SEM images of the polished cross sections for the Sn-Bi/Ni-P samples using the lab-manufactured Ni-P pads: (a) as-reflowed; (b) 220 °C, 0.5 h; (c) 220 °C, 24 h; and (d) 240 °C, 24 h.

Fig. 6. Thickness of the formed Ni₃P and Ni₃Sn₄ for the Sn-Bi/Ni-P system using the lab-manufactured Ni-P pads as a function of storage temperature and time.

Fig. 7. SEM images of the polished cross sections for: (a) Sn-56.8Bi-2Al/Ni-P and (b) Sn-57.4Bi-1Zn/Ni-P.

Fig. 8. SEM images of the polished cross sections for: (a) Sn-56.8Bi-2Ru/ Ni-P; (b) Sn-56.8Bi-2Ti/ Ni-P; and (c) Sn-57.4Bi-1Au/ Ni-P.

Fig. 9. SEM images of the polished cross sections for: (a) Sn-56.8Bi-2Cr/ Ni-P; (b) Sn-57.4Bi-2Si/ Ni-P; (c) Sn-56.8Bi-1Nb/ Ni-P; and (d) Sn-57.4Bi-1Pt/ Ni-P.

storage. This may be due to the Cr, Si and Nb having extremely low solubility in the basic Sn-58Bi solder, and hence precipitating out; however, it is not clear where the Pt went. In addition, an extremely large Bi particle was found to precipitate out of the Sn-56.8Bi-2Si solder, one of the three custom prepared solders [Fig. 9(b)].

Ag was found to reduce the consumption rate of the Ni-P, but the effect was still small [Figs. 10(a) and 11]. A small quantity of additional Ag-Sn IMC, in the form of nanoparticles, was observed in the vicinity of the Ni_3Sn_4 IMC grain boundaries [Fig. 10(c)].

In contrast, addition of Cu was found to be effective in modifying the IMC formed at the interface (Fig. 12). The mechanism is similar to the reaction between molten Sn-3.5Ag solder saturated with Cu and electroless Ni-P [21]. Cu in the molten SnBiCu solder precipitated out as a layer of Cu-Ni-Sn IMC, instead of the Ni_3Sn_4 IMC formed with the molten Sn-58Bi solder. The IMC formed at all three temperatures was identified

as $(\text{Cu},\text{Ni})_6\text{Sn}_5$ from EDX analysis. This layer of $(\text{Cu},\text{Ni})_6\text{Sn}_5$ IMC acts as a reaction barrier and significantly reduced the consumption rate of the Ni-P substrate during high-temperature storage (Figs. 4 and 13). Only a few locations were converted to porous Ni_3P with limited size and thickness. The majority of the Ni-P metallization remained intact following contact with the molten Sn-57.4Bi-1Cu solder for all samples stored at 200 °C, 220 °C, and 240 °C for storage periods less than 432 h [Figs. 12(e)–(g)]. When the storage time was increased to 716 h, the Ni-P layers were entirely converted to porous Ni_3P , through which Sn can penetrate to react with the underlying Cu metallization to form Cu_3Sn [see the solid arrow in Fig. 12(h)].

Micro-cracks were observed in all samples, including the as-reflowed sample, except for the three samples stored at 220 °C for 25, 48, and 240 h and one sample at 240 °C for 240 h. The locations of the micro-cracks are shown by the open arrows in Fig. 12(a)–(f). In particular, it was observed that of the two samples stored at 220 °C for 25 h, one of them

Fig. 10. SEM images of the Sn-57.4Bi-1Ag/Ni-P samples: (a) polished cross section, 200 °C, 48 h; (b) polished cross section, 240 °C, 48 h; (c) etched top, 200 °C, 96 h.

Fig. 11. Comparison of thickness of Ni-P, Ni₃P and Ni₃Sn₄ for the Ni-P substrate in contact with the Sn-57.4Bi-1Ag solder and the basic Sn-58Bi solder.

contained micro-cracks in the Ni-P layer [Fig. 12(c) and (d)] but the other did not. As in the Sn-Bi/Ni-P system, the total thickness of the residual Ni-P layer plus the formed Ni₃P layer for all the four samples without such micro-cracks were clearly thinner than those for the other Sn-57.4Bi-1Cu/Ni-P samples, as shown in Fig. 13(d), where the arrows point at the data for the samples whose thickness addition of Ni-P and Ni₃P are clearly lower than those for the other samples.

In general, the thickness of the residual Ni-P layer decreased, and the thicknesses of both the formed Ni₃P layer and the (Cu,Ni)₆Sn₅ layer increased with increasing storage time, as shown in Fig. 13(a)–(c). However, the fluctuations of the thicknesses of the different layers with respect to both storage temperature and time are more significant than those in the Sn-Bi/Ni-P system (Fig. 4), and the correlation between the growth rates of IMCs and the storage temperature cannot be evaluated.

IV. DISCUSSION

A. Interfacial Reaction in Sn-Bi/Ni-P System

The interfacial reaction products are in agreement with those reported for reactions of liquid Sn-37Pb, Sn-3.5Ag and also

Sn-58Bi solders with similar electroless Ni-P substrates for reaction times from 5 s to 5 h [12], [15], [22]. In the present work where the samples were prepared using the Ni-P pads on commercial PCB boards and stored at high-temperature for longer reaction times, the interfaces between the IMC and the solder are wavier, and the pores in the Ni₃P layers are significantly larger than the previously reported Kirkendall voids [15]. These wavier interfaces could be ascribed to the continuous development and the non-conservative nature of the coarsening process, i.e., the number of Ni₃Sn₄ grains decreased, while their volume fraction increased due to interfacial reaction, as suggested by Ghosh [11]. In investigation of the coarsening kinetics of Ni₃Sn₄, scallops formed during the early stages (up to 600 s) of interfacial reactions between liquid Sn-3.5Ag, Sn-57Bi and Sn-38Pb solders and electroplated Ni substrate [11]. Ghosh suggested that the non-conservative nature of the coarsening process could account for the observed increase in the standard deviation of the size distribution of the Ni₃Sn₄ scallops with reaction time. Meanwhile, several mechanisms, including anisotropic interfacial energy, interparticle diffusional interactions and the classical interparticle contact stress, could cause faceting to become very prominent as the Ni₃Sn₄ scallops coarsened [11]. Therefore, applied to the present interfacial reaction in the Sn-Bi/Ni-P system for longer timescales, these mechanisms led to the wavier interfaces and the faceted Ni₃Sn₄ grains because the increase in size variations of the Ni₃Sn₄ scallops, and also the faceting, continuously develop with the reaction time. The pores in the Ni₃P layers may result from the coalescence of Kirkendall voids.

Fig. 14 shows that the thicknesses of the Ni-P layers in the as-received substrate pads fluctuated significantly, in the range of 3.0 to 4.5 μm. Micro-cracks, allowing the immersion gold to penetrate, were observed in thicker Ni-P layer, while no micro cracks were observed in the thinner Ni-P layer pads. Therefore, the micro-cracks observed in Fig. 3(b)–(d) already existed before soldering and their occurrence was probably associated with the levels of intrinsic stresses produced during the electroless plating process [23], [24], as this explains the correlation between layer thickness and occurrence of microcracks. As disordered crack systems, the densities of microcracks varied among the as-received Ni-P pads and had somewhat changed after the soldering process. Therefore, despite the fact that the microcracks and pores affected the IMC growth, it is difficult

Fig. 12. SEM images of the polished cross sections for the Sn-57.4Bi-1Cu/Ni-P samples: (a) as-reflowed; (b) 200 °C, 25 h; (c) 220 °C, 25 h; (d) 220 °C, 25 h, another sample; (e) 240 °C, 25 h; (f) 220 °C, 120 h; (g) 220 °C, 240 h; (h) 200 °C, 716 h; and (i) 240 °C, 716 h.

to establish a quantitative relationship between the densities of microcracks in the original pads, and subsequent IMC thickness. This can be further confirmed by Fig. 15 showing the plots of Ni_3Sn_4 thickness versus density of crack for the three storage temperatures. Here the densities of cracks were measured from the SEM images of the samples after the high-temperature storage and expressed as the numbers of the microcracks divided by the cross-sectional lengths.

Unlike the results from the Sn-Bi/Cu system in which the IMC growth appeared to be diffusion controlled and the Arrhenius relationship could be applied to model the variation in the growth rate constants with temperature [16], there is no clear correlation observed between the growth rates of IMCs and the storage temperature. This is very similar to the result reported by Prakash *et al.* [13] for the interfacial reaction between the molten Sn-Pb solders and Cu substrate. The latter was thought to be related to effects of temperature on both dissolution and growth rates of IMCs. In the present case, it can be reasonably attributed to the highly scattered micro-cracks and pores within the Ni_3P layer, which have

been described in detail elsewhere [25]. As shown in Fig. 3, the pores are not uniformly distributed and their sizes are highly scattered within the formed Ni_3P layers. Despite the fact that other mechanisms, such as grain coarsening and grain grooving [11], [14], [15], might be involved, both grain boundary diffusion and bulk diffusion of atoms through the porous Ni_3P layer are important mechanisms for the present interfacial reaction and IMC growth. The highly scattered micro-cracks and pores within the Ni_3P layers are hence likely to have caused fluctuations in the rates of interfacial reactions and therefore of the thicknesses of the different layers. This can be further confirmed by the results of the Sn-Bi/Ni-P samples using the lab-manufactured Ni-P pads, as shown in Figs. 5 and 6. In the latter case, high-temperature storage was carried out for relatively shorter times, and no apparent pores and micro-cracks were observed in any of the samples. The thickness of both Ni_3P and Ni_3Sn_4 fluctuated less significantly and appeared to increase with increasing the reaction temperature and time. As also described in detail elsewhere [25], as an average for the three reaction temperatures, a temporal law with time expo-

Fig. 13. Thickness of the residual Ni-P and the formed Ni₃P and Ni₃Sn₄ as well as the total thickness of Ni-P plus Ni₃P for the Sn-57.4Bi-1Cu/Ni-P system as a function of storage time.

Fig. 14. SEM images taken from the polished cross sections of the as-received Au/Ni-P pads: (a) the micro-cracks observed in thicker Ni-P layer and (b) no micro-crack existing in thinner Ni-P layer.

ment, $1/n$ where n is greater than 3 can be applied to predict the thickening kinetics of the IMC Ni₃Sn₄ shown in Fig. 4, which can be attributed to the radial growth kinetics of the Ni₃Sn₄ grains and grain boundary diffusion due to the existence of molten channels between the previously formed Ni₃Sn₄ grains.

B. Interfacial Reactions in Sn-Bi-X/Ni-P Systems

Zn, Ti, Au, and Ru appear to have had no effect on the interfacial microstructure between the solder and Ni-P substrate when

compared to the Sn-Bi/Ni-P system. Al appears to have accelerated consumption of the Ni-P and Ni₃P layers but was also not detected at the solder-substrate interface, and the observed effect could have been due to poor quality substrate pads.

The nanometer-sized Ag-Sn IMC particles formed in the Sn57.4Bi1Ag/Ni-P system are similar to Ag₃Sn precipitated on the IMC surfaces in the as-soldered Sn-3.5Ag/Cu and Sn-3.5Ag/Ni samples [26]. In the latter instance, the precipitation of the nanometer-sized Ag₃Sn grains was believed to

Fig. 15. Plots of Ni_3Sn_4 thickness versus density of crack for the three storage temperatures.

be the reason for the relatively thinner IMC layer formed in Sn-3.5Ag/Cu system when compared with that of the Sn/Cu system. This suggests that “ Ag_3Sn ” groups were probably formed and captured at the surfaces of the main IMC grains since they reduced the interfacial energy, causing the growth of the main IMCs to slow down to some extent. After the solders cooled down, these “ Ag_3Sn ” groups were precipitated out as nanometer-sized Ag_3Sn particles [26], as shown in Fig. 10(c) where these Ag_3Sn particles can be estimated smaller than 50 nm in size. However, because they cannot be clearly observed in Fig. 10(a) and (b), it is difficult to estimate their volume percent.

The formation of $(\text{Cu},\text{Ni})_6\text{Sn}_5$, rather than Ni_3Sn_4 , between the SnBi1Cu solder and Ni-P substrate is because the formation and growth of the former is more thermodynamically favorable [21], [27], [28]. The structure of the $(\text{Cu},\text{Ni})_6\text{Sn}_5$ IMC formed in the present SnBi1Cu/Ni-P system was somewhat different from those at the Ni-P/Au/SnAgCu interface [28], which mainly consisted of $(\text{Cu},\text{Ni})_6\text{Sn}_5$, but also contained some Ni_3Sn_4 . Unlike the In-Sn/Nb system where the formation of NbSn_2 results in an excellent diffusion barrier protecting the substrate for over a year, the 4- μm -thick Ni-P layer in the SnBi1Cu/Ni-P system failed after a reaction time of about one month. This may be attributed to both the relatively porous nature of the $(\text{Cu},\text{Ni})_6\text{Sn}_5$ IMC and higher diffusion coefficients of atoms through the $(\text{Cu},\text{Ni})_6\text{Sn}_5$ IMC layer.

The total thickness of the residual Ni-P layers plus the formed Ni_3P layers for the SnBi1Cu/Ni-P system without the micro-cracks is less than those with micro-cracks, just as in the Sn-Bi/Ni-P system. Again, the micro-cracks observed in these SnBi1Cu/Ni-P samples already exist in the as-received Au/Ni-P pads before the application of the SnBi1Cu solder and were probably due to the intrinsic stresses produced during the electroless plating process.

The fluctuations of the thicknesses of the different layers in the SnBi1Cu/Ni-P system with respect to both storage temperature and time were more pronounced than those in the Sn-Bi/Ni-P system. This should be expected as the reaction times in the SnBi1Cu/Ni-P system are longer than those in the Sn-Bi/Ni-P system, and the fluctuations continually developed with increasing reaction time. Consequently the effect of

temperature on the IMC growth could not be evaluated, and the existing models of IMC growth [11], [13], [15], [18], [22] could not be applied to predict the IMC growth behavior in the SnBi1Cu/Ni-P system. Nonetheless, the results obtained here show the possibility of modification and limitation of IMC formation at the interface between molten solder and the substrate for extended periods, by adding a small quantity of an additional element.

V. CONCLUSION

The interfacial reaction products formed between the molten eutectic Sn-58Bi solder and electroless Ni-P include the IMCs Ni_3Sn_4 and porous Ni_3P , where the pores in the latter might result from the coalescence of Kirkendall voids formed during early stages of the interfacial reaction. The interfaces between the IMC and the solder were relatively wavier in the present studies than in comparable studies at shorter timescales.

Micro-cracks were found to occur at the surfaces of both the as-received Ni-P layers and the residual Ni-P layers for most samples. This was probably associated with the levels of tensile intrinsic stresses produced during the electroless plating process. The original $\sim 4 \mu\text{m}$ thick Ni-P layers began to fail at about 48 h at both 200 °C and 240 °C.

Among the additional elements, only Cu modified the interfacial IMC growth, by replacing Ni_3Sn_4 by $(\text{Cu},\text{Ni})_6\text{Sn}_5$, resulting in significantly decreased growth rates for both Ni_3Sn_4 and Ni_3P formation between the molten solder and the Ni-P substrate. Accordingly, the $\sim 4 \mu\text{m}$ thick Ni-P layers in contact with the molten Sn-Bi based solder alloyed with 1 wt.% addition of Cu could survive for at least 430 h at temperatures between 200 °C and 240 °C, but not for longer than 716 h.

The thickness of the residual Ni-P layer decreased, and the thicknesses of both the formed Ni_3P layer and the IMC Ni_3Sn_4 or $(\text{Cu},\text{Ni})_6\text{Sn}_5$ layer increased with increasing storage time. However, as a result of the large fluctuations of the thicknesses, the effect of temperature on the IMC growth could not be evaluated, and existing models could not be applied to predict the IMC growth behavior. This can be reasonably attributed to the highly scattered micro-cracks in the as-received Ni-P layer and the pores within the formed Ni_3P layer.

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