Electrical Analysis of High Dielectric Constant Insulator and Metal Gate Metal Oxide Semiconductor Capacitors on Flexible Bulk Mono-Crystalline Silicon

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***Abstract*—We report on the electrical study of high dielectric constant insulator and metal gate metal oxide semiconductor capacitors (MOSCAPs) on a flexible ultra-thin ($25\ \mu\mathrm{m}$) silicon fabric which is peeled off using a CMOS compatible process from a standard bulk mono-crystalline silicon substrate. A lifetime projection is extracted using statistical analysis of the ramping voltage ($\mathrm{V_{ramp}}$) breakdown and time dependent dielectric breakdown data. The obtained flexible MOSCAPs operational voltages satisfying the 10 years lifetime benchmark are compared to those of the control MOSCAPs, which are not peeled off from the silicon wafer.**

***Index Terms*—Flexible, lifetime projection, metal oxide semiconductor capacitors, time dependent dielectric breakdown, voltage breakdown, Weibull distribution.**

ABBREVIATIONS AND ACRONYMS:

MOSCAP	metal oxide semiconductor capacitor
TDDB	time dependent dielectric breakdown
C-V	capacitance-voltage
AC	alternating current

NOTATION:

κ	dielectric constant
$\mathrm{D_{it}}$	interface defect density
R_{series}	Series resistance
$\mathrm{V_{bd}}$	breakdown voltage
$\mathrm{V_{ramp}}$	ramping voltage used in accelerated tests
$\mathrm{t_{bd}}$	time to breakdown

Manuscript received March 12, 2014; revised June 30, 2014, September 22, 2014, October 19, 2014, and November 08, 2014; accepted November 09, 2014. Date of publication November 26, 2014; date of current version June 01, 2015. This work was supported by KAUST Office of Competitive Research Fund (OCRF) Competitive Research Grant CRG-1-2012-HUS-008. Associate Editor: S. Bae.

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Digital Object Identifier 10.1109/TR.2014.2371054

I. INTRODUCTION

RECENT advancements in flexible electronics have created opportunities for consumer electronics, bio-integrated electronics, and energy applications [1]–[9]. Starting with the seminal paper on flexible inorganic electronics [9], several demonstrations have provided various options for fabricating flexible inorganic devices with applications ranging from thin film to logic transistors [10]–[14]. To complement the present trend of exploring multifaceted applications using flexible electronics, we have investigated the reliability of flexible devices fabricated using a promising process where high dielectric constant (κ) insulator and metal gate metal oxide semiconductor capacitors (MOSCAPs) are first fabricated on a bulk mono-crystalline silicon, and then the top portion of the silicon substrate with the already fabricated MOSCAPs as a flexible silicon platform is released [15]. Flexibility comes from the ultra-thin nature of the released silicon top layer, which is also semi-transparent due to the presence of trench holes. We have conducted electrical characterization of both released flexible and unreleased inflexible devices. Our reliability analysis includes the standard ramping voltage ($\mathrm{V_{ramp}}$) breakdown analysis to extract the breakdown voltage ($\mathrm{V_{bd}}$), the time dependent dielectric breakdown (TDDB) analysis, and finally the lifetime projection.

II. DEVICE FABRICATION

Our process is standard complementary metal oxide semiconductor (CMOS) compatible and generic to any pre-fabricated as well as post-fabricated devices [15]–[23]. Three uniquely distinguishable features of this process are (i) usage of the most conventional and commercially widely available low-cost bulk mono-crystalline silicon substrate, (ii) ultra-large-scale-integration density and high thermal budget compatibility, and (iii) cost effectiveness including recyclability of the same wafer for multiple production cycles. Although the process and its effectiveness to transform varieties of silicon electronics (metal-oxide-semiconductor capacitors and transistors, thermoelectric generators, micro-lithium ion battery, laterally actuated micro-electro-mechanical systems based thermal actuator, etc.) into a flexible, semi-transparent one have been chronicled in various publications in the past, just a brief introduction is presented here. We start with any substrate or chip where the devices are

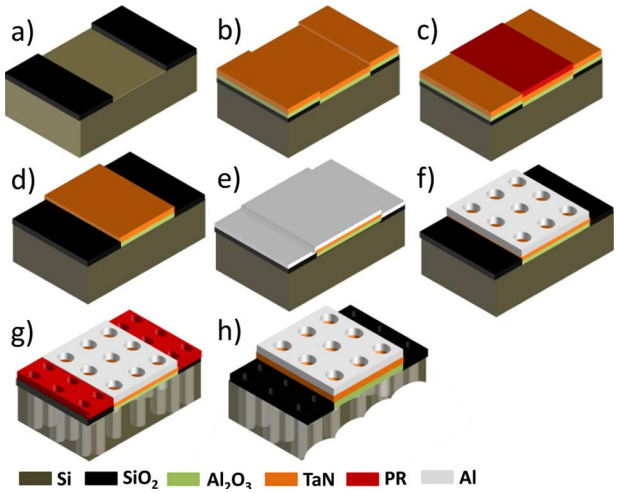

Fig. 1. Fabrication process of flexible MOSCAPs.

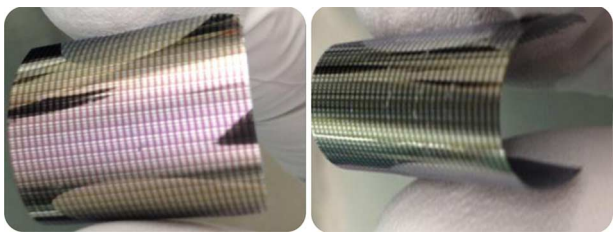

Fig. 2. Digital photo of the actual fabricated MOSCAPs on flexible ultra-thin Si fabric.

already fabricated retaining the intended performance-energy-cost effectiveness, ultra-large scale-integration density, and high thermal budget processes as required. The p-type, 4-inch silicon substrate used in this work is lightly doped with boron. The gate stacks in the MOSCAPs are deposited with an atomic layer deposited (ALD) 10 nm aluminum oxide (Al_2O_3) high-κ dielectric, and a 20 nm tantalum nitride (TaN) metal gate. Aluminum (Al) is used as a contact metal (Fig. 1 parts a through f). Then, we lithographically pattern the resist to expose the areas where the release holes are to be formed. With reactive ion etching (RIE), we make trenches through the interlayer dielectric (ILD) layers to expose the silicon substrate. Next, we perform a selective (to oxide or other insulating layers used in ILD) deep reactive ion etching (DRIE) to make trenches in the silicon (Fig. 1(g)). Subsequently, we form a vertical sidewall to especially cover the silicon sidewalls (of the trenches). Next, we use a xenon di-fluoride (XeF_2) based isotropic etching process to form caves inside the silicon. When the wall between adjacent caves is etched, the top portion of the silicon substrate with the pre-fabricated devices detaches, releasing a flexible silicon fabric (Fig. 1(h)). In the present experiment, the fabric is 25 μm thick and has an area of 6 cm^2 (Fig. 2).

III. Device Characterization

Fabricated MOSCAPs were characterized using capacitance voltage (C-V) measurements at low and high frequencies. We also extracted the parasitic capacitances. The C-V curves were

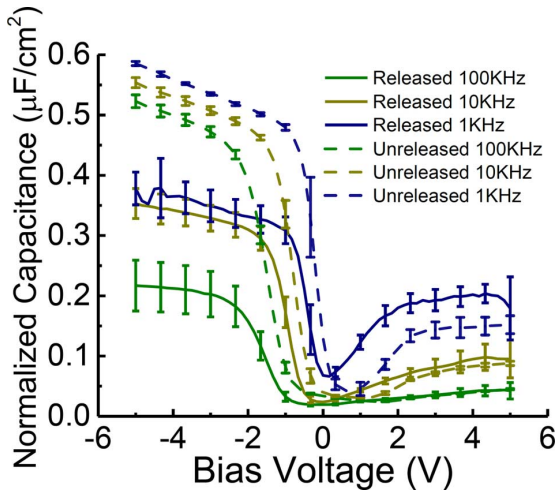

Fig. 3. Normalized C-V curves for flexible and inflexible MOSCAPs at different frequencies.

collected using an E4980A Precision LCR Meter (Agilent Technologies), with a 30 mV small AC signal superimposed on a direct current (DC) voltage bias. Fig. 3 shows the normalized capacitance of the flexible and inflexible devices, with flexible devices having a smaller effective area as there are 25 holes of the radius of 5 μm (i.e., 80% of total area) through the gate stack of each flexible device. The figure shows common C-V behavior in terms of accumulation $(< -2\text{ V})$, depletion $(-2\text{ V} \rightarrow +2\text{ V})$, and inversion $(> +2\text{ V})$ regions, as well as a reduction in inversion capacitance due to the minority carriers' inability to follow the AC signal at higher frequencies.

Although the frequency response in both types of devices is similar, the features in accumulation differ due to a difference in the properties of the inflexible silicon bulk and the ultra-thin fabric of the released flexible silicon. We can infer that, due to a poor contact between the bottom chuck and thin silicon fabric, the released device is more sensitive to the C-V frequency. There is an overall degradation in the normalized capacitance ranging from 30% at 1 KHz to 50% at 100 KHz, and a failure to operate at 1 MHz. It is also observable that, whereas the accumulation (below ~ -2 V) charge of flexible devices has a lower value, and is more dispersed relative to bulk devices, the behavior is reversed in the inversion region (above $\sim +2$ V) where the capacitance values of flexible devices are slightly higher than their bulk counterparts. This result implies that the generated traps and defects due to the release trenches have a net negative polarity. This negative polarity imposes a frequency limitation on our flexible devices associated with the drop in capacitance value as frequency increases. This result can be explained by the difference in the nature of our flexible silicon fabric compared to that of bulk silicon. The substrate is lightly doped, i.e., its resistivity is $11 - 20\ \Omega$.cm, and a limited number of free carriers are available. In the inversion region, because of the limited amount of free charges in the lightly doped substrate and its relatively high resistivity, the ability of charges to follow-up the fast changing voltage decreases. This inability of charges to respond is evident in the C-V curves from the drop in inversion capacitance maximum as the frequency of the voltage signal increases. In flexible silicon, the available

carriers are not only limited by the light doping level but also the limited supply of free carriers at the poor contact between the bottom chuck and the silicon fabric. This limitation amplifies the drop in capacitance phenomenon, that the accumulation mode maximum capacitance is also degraded as voltage signal frequency increases. The relative drop between flexible and inflexible capacitance is 30% at 1 KHz, and 50% at 100 KHz. This poor contact can be attributed to the non-planar bottom of the silicon fabric resulting from the isotropic etching release step (Fig. 4). Still, this limitation can be overcome by using a silicon-on-insulator (SOI) type substrate where the non-planar bottom formation will be inhibited by the presence of a ceiling buried oxide (BOX) layer, or an all front contact scheme can eliminate the problem but at the cost of more real estate. The frequency dispersion can also result from high interface defect density ($\mathrm{D_{it}}$). Equation (1) shows how $\mathrm{D_{it}}$ is calculated.

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{C_{lf}}{C_{ox-Clf}} - \frac{C_{hf}}{C_{ox}-C_{hf}}\right). \tag{1}$$

Using the oxide capacitance in the accumulation region (C_{ox}) and the capacitances in the inversion region at the lowest and highest available frequencies (C_{lf} and C_{hf}, respectively), we find that D_{it} for flexible devices is $3.8 \times 10^{11}\ \mathrm{cm^{-2}\ eV^{-1}}$. For bulk inflexible devices, D_{it} is $1.6 \times 10^{11}\ \mathrm{cm^{-2}eV^{-1}}$. Therefore, the interface defects density for flexible devices is $\sim 137\%$ higher than that of the inflexible ones. This result can be attributed to the structural features associated with the presence of a network of release holes.

To solve this dilemma, capacitance was corrected for series resistance (R_{series}). The plot in Fig. 3 is for capacitance measurement using the parallel equivalent circuit model ($\mathrm{C_p}$) with a dissipation factor (D). The conductance ($\mathrm{G_p}$) is calculated using (2), and (R_{series}) is calculated using (3) [24].

$$G_p = D\omega C_p \tag{2}$$

$$R_{series} = \frac{\left[\frac{G_p}{\omega C_p}\right]^2}{\left[1+\left[\frac{G_p}{\omega C_p}\right]^2\right] G_p}. \tag{3}$$

R_{series} was calculated using (3) at different frequencies ($\omega = 2\pi f$). The results of R_{series} at -5 V (deep accumulation) are shown in Table I. The higher values of R_{series} for flexible devices is attributed to the non-planar bottom shown in Fig. 4. Fig. 5 shows the modified version of the C-V plot after accounting for series resistance. Although there is observable improvement in the frequency dispersion, it can be deduced that the remaining dispersion is due to intrinsic properties of the high-κ $\mathrm{Al_2O_3}$ rather than extrinsic factors.

Dummy MOSCAPs with 300 nm thermal $\mathrm{SiO_2}$ dielectric are used to extract parasitic capacitance (capacitance due to the external cables and connections that does not pertain to the actual device). If we examine dummy MOSCAPs fabricated on the same wafer with released and unreleased devices (Fig. 6, corrected for series resistance), we observe that there is almost no frequency dispersion in the unreleased dummy MOSCAPs. The $\mathrm{Si-SiO_2}$ interface has very low defect density for thermal oxide, and as a result, there is no frequency dispersion. On the other hand, we notice that the released dummy devices exhibit frequency dispersion. Excluding the series resistance effect and the $\mathrm{SiO_2}$ interfacial defects (based on the non-dispersed unreleased dummy devices), we can attribute this dispersion to the etching holes covered with $\mathrm{Al_2O_3}$ sidewalls in the active area of the devices leading to the introduction of significant defects in the oxide. Therefore the high-κ $\mathrm{Al_2O_3}$ has a high defect density, leading to mild dispersion in unreleased actual MOSCAPs as shown in Fig. 5, and calculated in previous $\mathrm{D_{it}}$

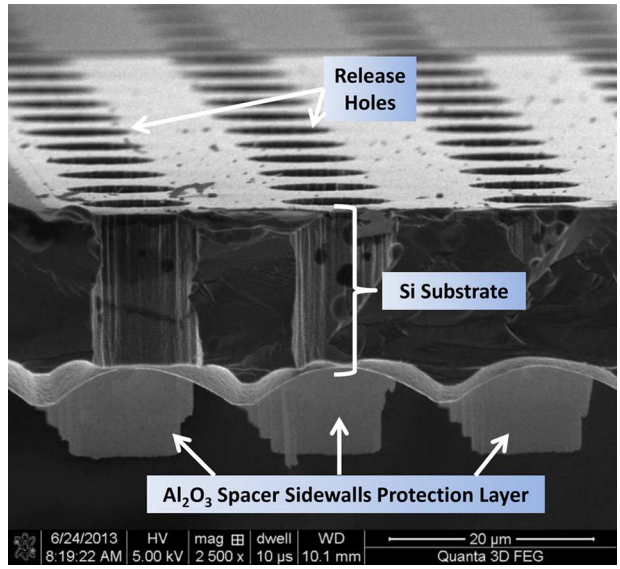

Fig. 4. The scanning electron microscope image of the thin silicon fabric showing the scallops at the bottom of the structures, which might be caused by the release processing step.

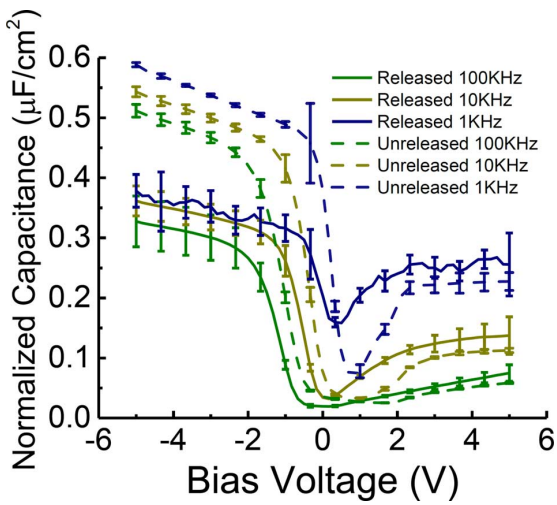

Fig. 5. Normalized C-V curves for flexible and inflexible devices corrected for series resistance.

TABLE I
SERIES RESISTANCE VALUES FOR RELEASED AND BULK DEVICES AT DIFFERENT SMALL SIGNAL EXCITATION FREQUENCIES

Frequency	1 kHz	10 kHz	100 kHz	1 MHz
R_{series} (released)	321 kΩ	57 kΩ	37 kΩ	26 kΩ
R_{series} (bulk)	91 kΩ	16 kΩ	2 kΩ	1 kΩ

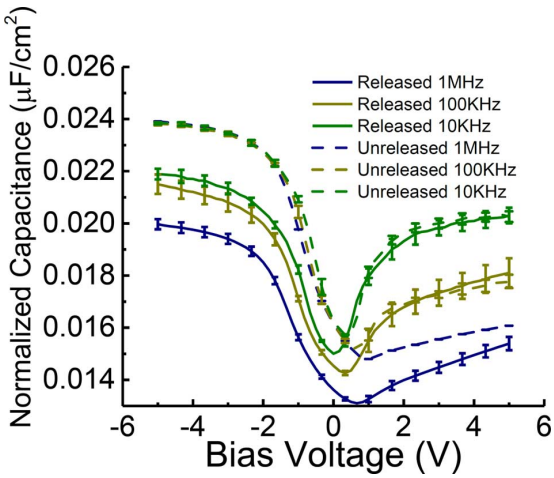

Fig. 6. Normalized C-V curves for flexible and inflexible dummy MOSCAPs at different frequencies.

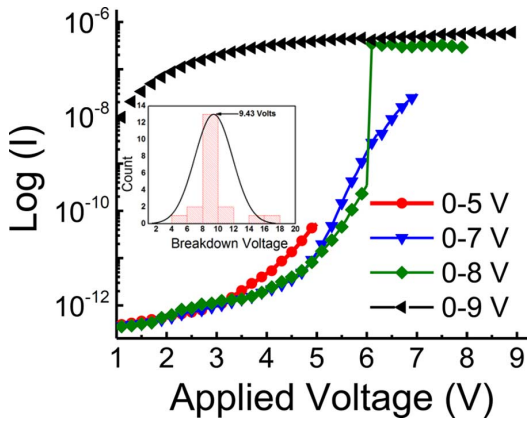

Fig. 7. The current-voltage dependencies for the subsequent applied Vramp measurements with a 1V increment. Inset: the histogram of V_{bd} values obtained on tested devices.

calculations, while the presence of release holes and Al_2O_3 spacers introduces significant defects in dummy MOSCAPs (Fig. 6). Finally, both the defective high-κ Al_2O_3 and the release holes introduced defects lead to severer dispersion, as shown in released MOSCAPs (Fig. 5) and D_{it} calculations. However, today's technology might be more forgiving on this shortcoming thanks to today's 10s or 100s of nanometers technology nodes, as then the release trenches do not need to go through the active areas. Hence, these results can be more of a guideline for our release process than a frequency imposed limitation because, without holes in active areas, D_{it} is only mandated by the material system and fabrication processes which can be optimized without interfering with our release process.

IV. Reliability Analysis

Reliability analysis was done by executing the V_{ramp} test on 20 devices with 200 mV increments. V_{bd} was then determined as the median value which coincided with the value of most occurrences. After determining V_{bd}, TDDB measurements were done at 3 different stress voltages ($\pm$200 mV incremented to 85% of V_{bd}). However, using 85% of V_{bd} for flexible devices resulted in immediate breakdown in 10s of seconds; hence, the values have been reduced to 72% for flexible devices. Each constant stress voltage was applied to 10 devices to construct a single line on a Weibull distribution ($ln(-ln(1-F))$ versus time plot, where F is the fraction of the device number, arranged in ascending order with respect to time-to-breakdown (t_{bd}), divided by the total number of measured devices at the same stress voltage. From the Weibull plot, the value of t_{bd} corresponding to $F = 0.63$ ($ln(-ln(1-F)) = 0$) is extracted for lifetime projections.

In the V_{ramp} breakdown measurements, devices were subjected to incremental increases in gate voltage until the dielectric breakdown (determined as greater than an order of magnitude leakage current increase) occurs (Fig. 7). The inset shows a histogram for extracting the average value of most occurrences. This value is carried forward to be used as a stress voltage in the constant voltage stress (CVS) measurements in the TDDB study. The actual voltage drop across the gate dielectric is actually lower than the applied voltage because some voltage is dropped across the bottom chuck and lightly doped p-type substrate. To quantify this drop for the purpose of obtaining accurate reliability projections, we calculate the built-in voltage drop (V_{bi}).

$$V_{bi} = \varphi_m - \varphi_{p-si}. \tag{4}$$

φ_m is the work function of the metal-stainless steel in volts ($\sim$ 4.7 V [25]), and φ_{p-si} is the work function of the p-type silicon in volts (2.194 V), calculated using (5), and (6).

$$E_{FV,p-si} = -K_B T\, x\, \ln(\frac{p}{N_v}) \tag{5}$$

$$q\varphi_{p-si} = q\chi_{si} + E_{g,si} - E_{FV,p-si}. \tag{6}$$

The difference between the Fermi level energy and the valence band energy of p-type silicon ($E_{FV,p-si} \sim 0.296$ eV) is calculated using the background thermal energy ($K_B T \sim 0.026$ eV at 300 k), the Boron doping concentration ($p \sim 2.2\times10^{14}$ cm^{-3} [26]), and the valence band effective density of states ($N_v \sim 3.1\times10^{19}$ cm^{-3}[27]). The work function of the p-doped silicon then reduces to simple addition between the electron affinity of Si ($qXsi \sim 1.39$ eV), the forbidden band gap of Si (($E_{g,si} \sim 1.1$ eV), and $E_{FV,p-si}$ calculated in (5). Using (6) to calculate φ_{p-si}, and plugging the result into (4), gives V_{bi} of $\sim$ 2.5 V. In Fig. 7, we observe that, until 0–7 volts, there is no physical damage in the material as evident by all the appended sweeps for 0–3, 0–5, 0–6 volts following the same slope patterns. Then, at the 0–8 volts sweep, we see the wear out phase leading to breakdown characterized by a very steep slope, until reaching a set current compliance limit. The subsequent 0–9 volt sweep confirms that the material was indeed permanently damaged (hard breakdown) because the initial current value at 0.1V is very high while the current exhibits Ohmic-like behavior.

Under a continuous stress, a random creation of defects contributing to the electron transport through the dielectric occurs, culminating in the run-away defect generation process [28]. At this stage, a permanent conductive path between the top electrode and bottom semiconductor through the dielectric is formed. The average applied voltage at which breakdown

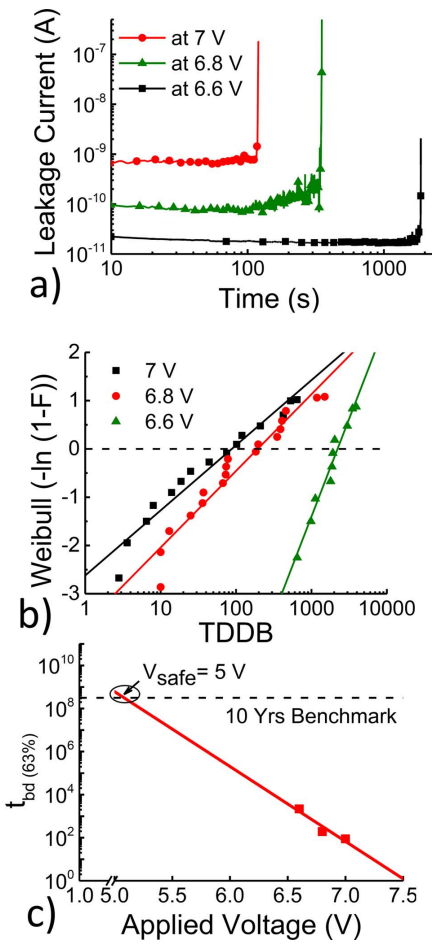

Fig. 8. (a) Sample constant stress voltages (CVS) measurements performed on flexible devices, (b) corresponding Weibull distributions, and (c) lifetime projection plot.

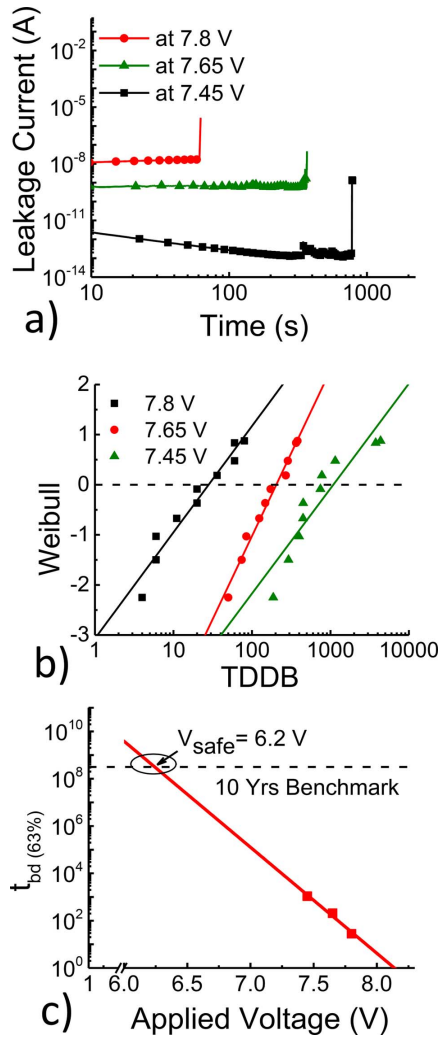

Fig. 9. (a) Constant stress voltages (CVS) measurements on unreleased inflexible devices, (b) corresponding Weibull distributions, and (c) lifetime projections plot.

occurs is 9.43 V for released devices compared to 9 V for unreleased (corresponding to an effective E-filed of 6.93 MV/cm, and 6.50 MV/cm on the dielectric in released, and unreleased devices, respectively after deducting V_{bi} at the backside contact).

TDDB and lifetime projections are then carried out. Fig. 8(a) shows TDDB data for flexible devices at different CVS values. Clearly, as the stress voltage increases, the initial leakage current increases, and t_{bd} decreases significantly. The observed decrease in the leakage current during the initial stress time period is due to the continuous trapping of injected electrons in the high-κ film [29].

Similar measurements have been performed on 10 released devices, and the Weibull distribution plot [Fig. 8(b)] was constructed to extract the 63% t_{bd} value to be used in lifetime projections [Fig. 8(c)]. From the linear fit (based on the electric field driven primary degradation mode) in Fig. 8(b), the safe operating voltage (V_{Safe}) for released devices would be < 5 V, which is acceptable for most integrated circuits as technology scaling is heading in the direction of reducing supply voltages to 1 V and lower. Similarly, Fig. 9 parts (a) through (c) represent an example of (a) the TDDB plot for the unreleased devices stressed at 7.8 V, 7.65 V, and 7.45 V; (b) the corresponding Weibull distribution plot for the t_{bd} extraction; and (c) lifetime projections.

These plots show that the unreleased devices pass the 10 years benchmark at < 6 V (exceeding the released devices by 1V). However, the lightly doped wafer had a resistivity in the range of $11 - 20\ \Omega$.cm. Because the devices are back gated, there is a voltage drop across the Si bulk. This lost voltage is 20 times higher for the unreleased devices compared to the released ones because the bulk silicon is 500 μm thick compared to 25 μm of the released fabric. Hence, although the stress voltage is higher for unreleased devices, a higher portion of the applied voltage drops in the silicon bulk, resulting in a much lower stress voltage applied to the gate stack (see calculations in Section V). Overall, the actual voltage stressing the dielectric in the released device case is higher than that for unreleased counterparts due to the larger voltage drop across the lightly doped Si bulk. Moreover, the employed extrapolation model for lifetime projection uses a conservative linear on a semi-log scale fitting, comparing to the power-law model (lifetime $\alpha\ V^{-n}$) fitting which would lead to a significantly higher lifetime for the same operational voltage [30]. Note that, in both cases, the range of the used stressing

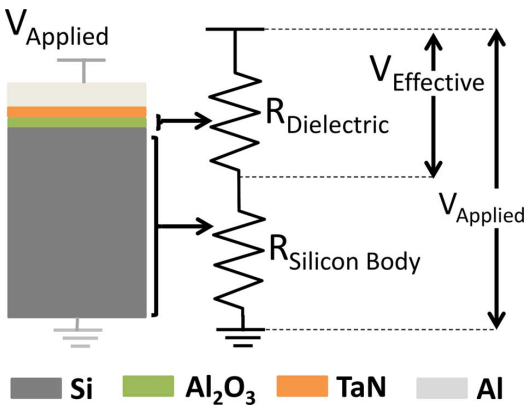

Fig. 10. Modelling of back gated MOSCAPs in terms of series resistances.

voltage values might be too narrow comparing to the intercept at the 10 years benchmark voltage value [30]–[33]. The selection of stress voltages is done based on practical considerations; they are chosen to result in a breakdown around a few thousand seconds, then further readings at ± 200 mV increments are taken.

V. Discussion

Although the above reliability analysis allows us to make certain conclusions regarding the difference between the flexible and inflexible MOSCAPs, a closer look at the dielectric reliability irrespective of the probing setup would enable discerning the variation in the dielectric physical properties due to the flexing process. To achieve that result, we define the effective voltage (V_{eff}) as the voltage across the dielectric, which can be calculated using a simple voltage divider (7), while the MOSCAP can be modelled as in Fig. 10.

$$V_{eff} = (V_{app} - V_{bi}) x \frac{R_{Dielectric}}{R_{Dielectric} + R_{Silicon\ Body}} \quad (7)$$

where V_{app} is the actual applied back gate voltage, V_{bi} is the built-in voltage drop at the metal chuck and the p-type Si interface due to the difference between the work function of the metal and the electron affinity of the p-type Si, $R_{Dielectric}$ is the resistance of the dielectric, and $R_{Silicin\ Body}$ is the resistance of the Si bulk.

$$R_{Dielectric} = \rho_{Dielectric}\ x\ \frac{t_{Dielectric}}{A_{Device}} \quad (8)$$

$$R_{Silicon\ Body} = \rho_{Silicon\ Body}\ x\ \frac{t_{Silicon\ Body}}{A_{Device}} \quad (9)$$

where ρ and t are the resistivity in Ω.cm, and thickness of the corresponding materials, respectively. $\rho Dielecric \sim 10^{14}$ Ω.cm for Al_2O_3, $\rho_{Silicon\ Body} \sim 15.5\Omega$.cm for lightly doped p-type Si, A_{Decice} is device area (which does not contribute in effective voltage calculation), $t_{Dielectric} = 10$ nm, and $t_{Silicon\ Body} = 500\ \mu$m and 25μm for the inflexible and flexible MOSCAPs, respectively. Plugging these values into (7) through (9), we find that the effective voltage across the flexible and inflexible devices is 99.99% of the applied voltage. This happens because of the negligible resistance of the Si body compared to that of the much higher dielectric resistance. Therefore, the series resistance effect due to changes in the Si thickness can be safely neglected.

VI. Conclusion

In this paper, we report the electrical analysis of flexible MOSCAPs on 25 μm thick flexible silicon fabric. The released devices show acceptable operational voltages below 5 V compared to 6.2 V for bulk unreleased devices (degradation of $\sim 19\%$). However, such magnitude of the operational voltage makes the degradation non-significant as today integrated circuits pursue operation voltages of around 1V to minimize power consumption. Moreover, calculations performed to assess the series resistance, due to substrate thickness differences between flexible (25 μm) and bulk (500 μm) stacks for back gated MOSCAPs, show negligible difference. Finally, the frequency response degradation of the flexible MOSCAPs is attributed to both a poor contact between the scalloped silicon fabric and the bottom electrode, and higher defects at the interface between holes and device active area hindering the ability of carriers to respond at higher frequencies.

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